VPR-3

Training Manual
Vol. I

AMPEX

VPR-3

Training Manual
Vol. I

10017

VIDEO HEAD MOUNTING SHOE

USED IN

A. VIDEO ERASE HEADS
B. VIDEO RECORD/PLAY HEADS
C. VIDEO DUMMY HEADS (VPR-80)

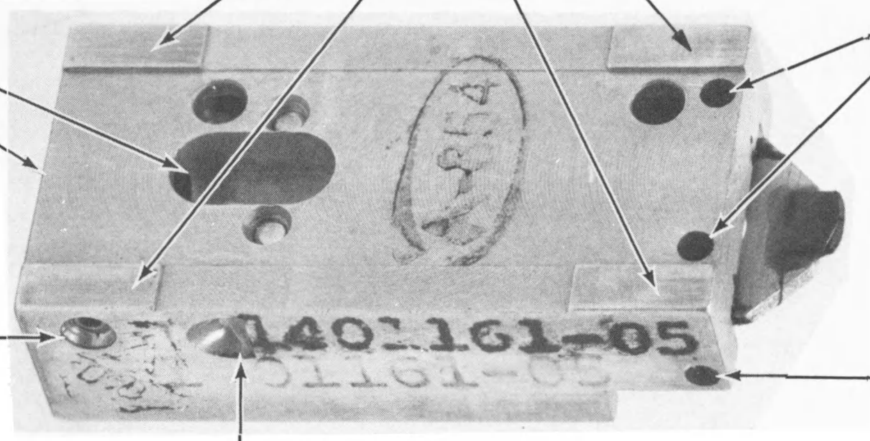
THESE FOUR MOUNTING FEET REST ON THE SCANNER BASE AND ESTABLISH HEAD HEIGHT WITH RESPECT TO THE TAPE.

FACTORY FIXTURE ALIGNED TIP PROJECTION SET SCREW.

THESE TWO FACTORY FIXTURE ALIGNED SET SCREWS ESTABLISH

1. HEAD HEIGHT WITHIN SHOE.
2. HEAD AZIMUTH.

TIP PROJECTION LOCKING SET SCREW.



THIS SET SCREW IS FACTORY FIXTURE ALIGNED TO ESTABLISH THE RELATIONSHIP OF THIS HEAD TO ALL OTHERS WITHIN THE SCANNER SEE FIG. 2

FIG. 1

SCANNER HEAD MOUNTING REGISTRATION PIN SEAT.

HEAD CONNECTOR PINS.

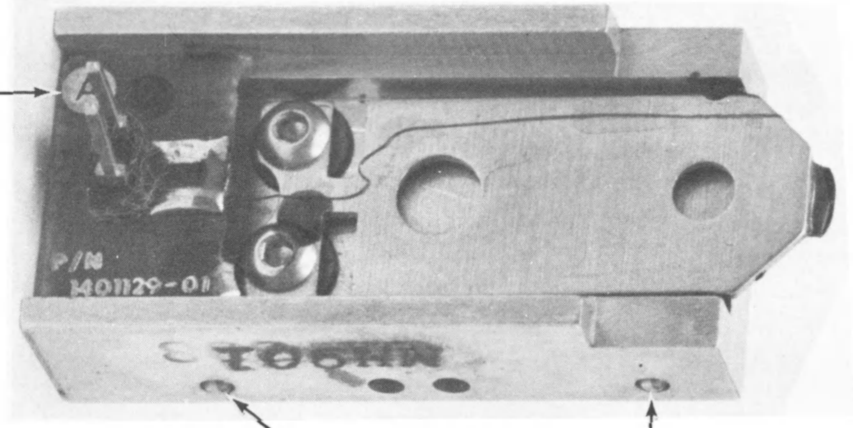


FIG. 2

THESE FACTORY PRESSED IN BALL BEARINGS MATE TO HARDENED INSERTS WITHIN THE SCANNER HEAD MOUNTING SYSTEM. THIS ESTABLISHES THE RELATIONSHIP OF THIS VIDEO HEAD TIP GAP TO ALL OTHERS WITHIN THE SCANNER SEE FIG. 1.

AST HEAD MOUNTING SHOE

USED IN

A. AST/PLAY HEADS
B. RECORD/AST PLAY HEADS (VPT (VPR-80)

SEE FIG. 1

SEE FIG. 1

SEE FIG. 1

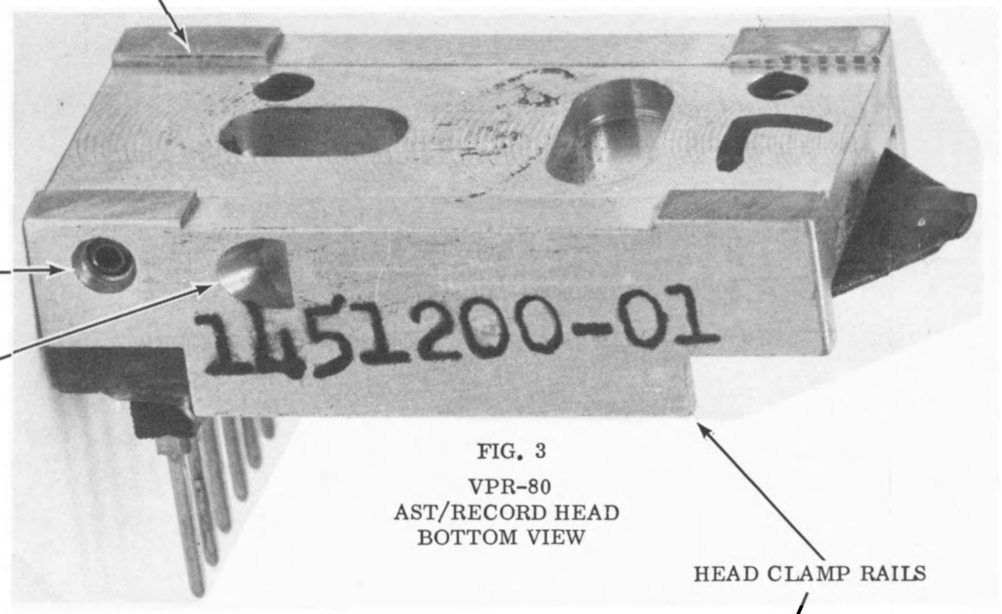


FIG. 3
VPR-80
AST/RECORD HEAD
BOTTOM VIEW

HEAD CLAMP RAILS

HEAD CONNECTOR PINS

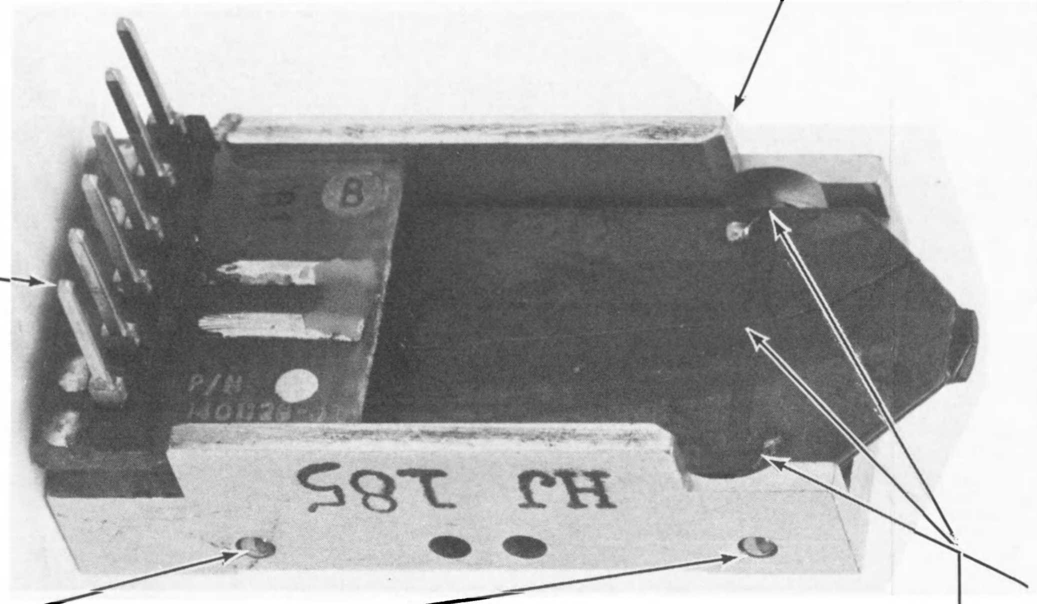
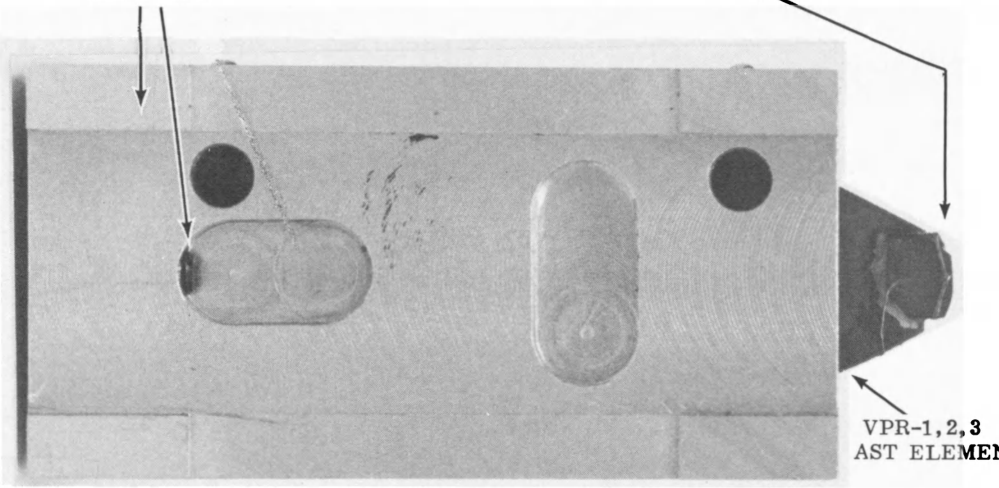


FIG. 4
VPR-80
RECORD/AST HEAD
TOP VIEW

HEAD JUMPER WIRES AND INSULATING STRIP WHICH ALLOW THE ELEMENT TO ARTICULATE IN AN S CURVE AS IT DEFLECTS PROVIDING OPTIMUM HEAD TO TAPE CONTACT IN SLO-MO.

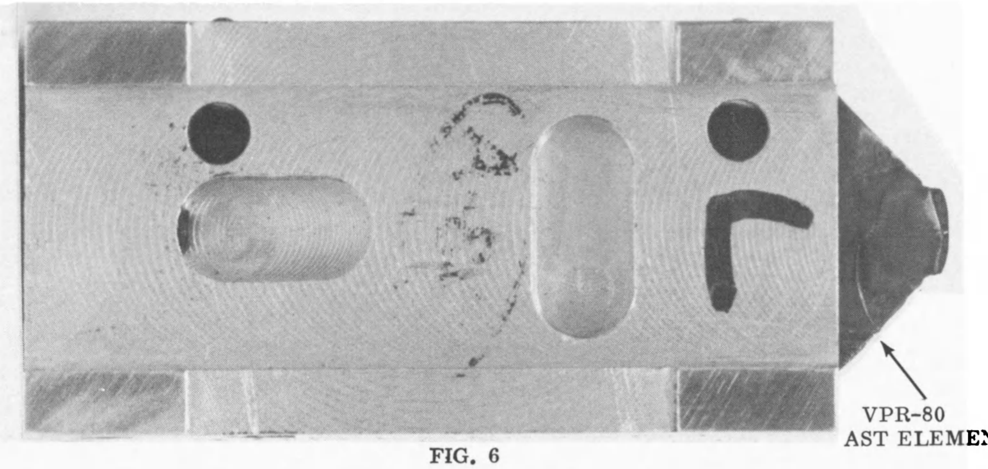
NOTE:
THE MISSING PORTION OF THIS BROKEN HEAD TIP BY COMPARISION WITH THE GOOD TIP BELOW SEE FIG. 6,9,10.

SEE FIG. 1



VPR-1,2,3
AST ELEMENT

FIG. 5
VPR-1, VPR-2, AND VPR-3 AST/PLAYBACK HEAD



VPR-80
AST ELEMENT

FIG. 6
VPR-80
RECORD/AST PLAYBACK HEAD

NOTE:

TWO TYPES OF AST ELEMENTS ARE CURRENTLY IN USE, AND ARE NOT INTERCHANGABLE. THE TWO HEAD TYPES CAN BE DISTINGUISHED BY,

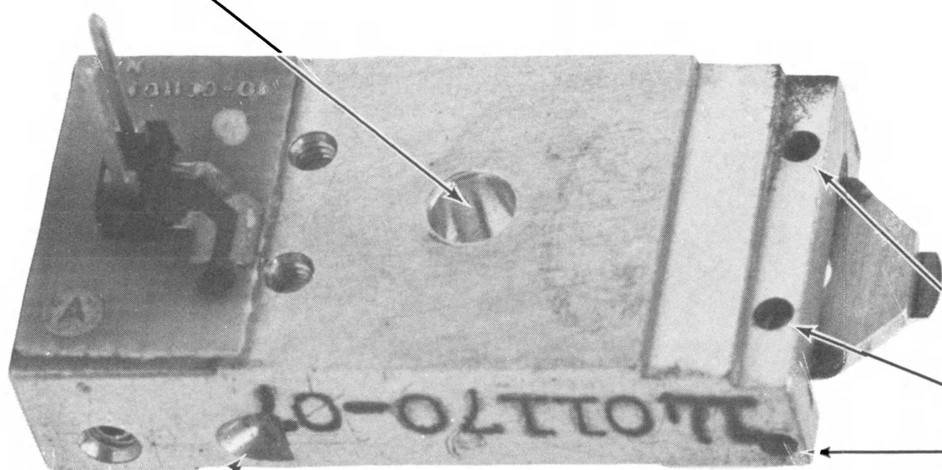
1. PART NUMBER
2. ELEMENT SHAPE AS VIDEO HEAD TIP.

1" VTR
SCANNER HEADS

SYNC HEAD MOUNTING SHOE

USED IN
A. SYNC RECORD/PLAY HEADS
B. SYNC DUMMY HEADS

MOUNTING SCREW HOLE



DUMMY HEAD TIP
NOTE ABSENCE
OF HEAD WINDINGS.

SEE FIG. 1

SEE FIG. 1

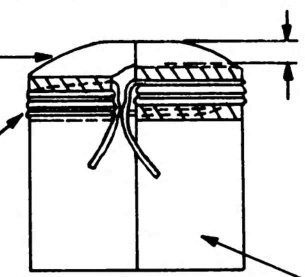
FIG. 7

GENERAL HEAD TIP CONSTRUCTION (CORE)

HEAD TIP IS CONTOURED TO MATCH SCANNER SURFACE CONTOUR

HEAD GAP DEPTH (LIFE) (.0013 TYPICAL)

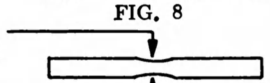
HEAD WINDINGS



HEAD TIP CORE

FIG. 8

HEAD NOTCH TO ESTABLISH ERASED OR RECORED TRACK WIDTH.



HEAD GAP
THE CAP IS FILLED WITH GLASS TO ADD STRENGTH AND PREVENT ENTRY OF FOREIGN MATERIAL.

HEAD PART NUMBERS

1400627-02	AUTOMATIC SCAN TRACKING HEAD, 50 Hz	A VIDEO RECORD/PLAY HEAD IS USED IN NON AST SYSTEMS.
1400626-02	AUTOMATIC SCAN TRACKING HEAD, 60 Hz	
1401166-05	VIDEO RECORD/PLAY HEAD, 50 Hz	
1401161-05	VIDEO RECORD/PLAY HEAD, 60 Hz	
1401165-06	VIDEO ERASE HEAD, 50 Hz	
1401160-06	VIDEO ERASE HEAD, 60 Hz	
1401169-06	SYNC RECORD/PLAY HEAD, 50 Hz	
1401164-06	SYNC RECORD/PLAY HEAD, 60 Hz	
1401168-06	SYNC ERASE HEAD, 50 Hz	
1401163-06	SYNC ERASE HEAD, 60 Hz	
1401170-07	SYNC DUMMY HEAD & (THREE HEADS USED IN NON-SYNC VTR'S).	
1451210	VIDEO DUMMY HEAD (VTR-80) (INSTALLED IN THE PLAY HEAD POSITION ONLY).	
1451200	AUTOMATIC SCAN TRACKING HEAD 60 Hz (VTR-80).	A VIDEO RECORD/PLAY HEAD CAN BE USED IF CORRECT HEAD IS NOT AVAILABLE. TURN OFF AST USE THE CENTER TWO PINS OF THE HEAD CONNECTOR.
1451220	AUTOMATIC SCAN TRACKING HEAD 50 Hz (VPR-80).	

A PORTION OF THIS HEAD TIP IS BROKEN AND MISSING

HEAD BONDING IS FRACTURED.

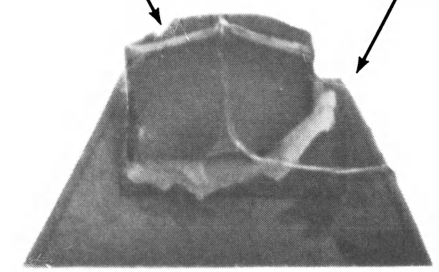
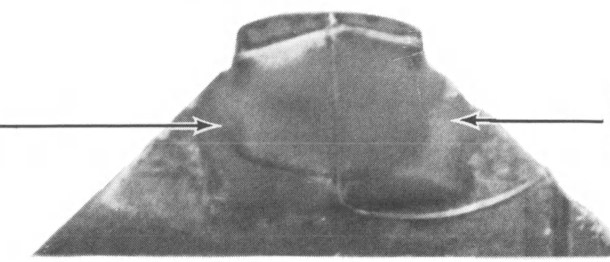


FIG. 9

DAMAGED VIDEO HEAD TIP (ALSO SEE FIG. 5)

VIDEO HEAD TIP IS BONDED TO TIP SUPPORT. IN THIS CASE THE AST ELEMENT.



EPOXY IS USED TO SECURE AND PROTECT THE HEAD WINDINGS. THE EPOXY DOES NOT EXTEND TO THE HEAD TIP.

FIG. 10

GOOD VPR-80 RECORD/AST HEAD TIP

VIDEO HEAD TIP CLEANING

1. MOISTEN A COTTON SWAB WITH AMPEX HEAD CLEANER AMPEX PART # 087-007.
2. GENTLY RUB THE HEAD TIP IN THE DIRECTION THE HEAD TIP CONTACTS THE TAPE IN NORMAL OPERATION.
3. AMPEX HEAD CLEANER IS PRIMARILY XYLENE WHICH WILL AGGRESSIVELY DESOLVE THE TAPE POLYESTER BACK FILM AND THE BINDER SYSTEM.

NOTE:

1. THE FOUR VIDEO HEAD MOUNTING FEET AND THEIR COMPANION SURFACES WITHIN THE SCANNER MUST BE THOROUGHLY CLEANED WHENEVER A HEAD IS REMOVED OR REPLACED SEE FIG. 1, 5, 6.

HOW NOT TO BE FRIGHTENED BY MICROPROCESSORS

by

E.S. BUSBY

It might help to explain the title if I told you that I once debated against the premise that "all fear stems from ignorance". I lost, convinced that at least we are much more comfortable about things we know about. This paper is not very technical, and is intended to be of help to those who know what an oscilloscope is, but don't know where to stick the probe. Relax, this won't hurt.

Since a microprocessor is not a computer, I won't talk about computers but about the use of a microprocessor to perform machine control logic, in, for example, a video recorder. In the simple days of video recording, most logic inputs came via the human finger, and the controlled devices, brakes, motors, and the like were slow. Control logic was performed by switch contacts and relays. It was slow by today's standards, but fast enough.

Relays were supplanted by digital logic, AND gates, OR gates, and other functions. They were embarrassingly fast. With all that time at hand, it is more efficient to share time on a single logic device and create any kind of gate or counter you need. Such is a microprocessor.

Most logic chips used today come in four-packs. Whatever it does, it does to four wires at once. Most of the microprocessors you will find in video recorders treat eight wires at once. If the state of each wire is called a binary BIT, then a collection of eight of them is called a BYTE, 16 of them a WORD, and four, a NIBBLE. Inside our device exists at least one eight-bit storage register which can be told to be an eight-wide AND, OR, COUNTER, SHIFT REGISTER, LATCH, or ADDER. It is called an ACCUMULATOR, and associated with it is a very important register called the STATUS REGISTER whose bits tell you whether the last thing the accumulator did resulted in all zeros or not, was negative or not, or resulted in a carry or a borrow. There is at least one 16-bit counter and usually a small collection of handy eight-bit storage registers as well. There are eight pins on the device through which it is told what to do, what to do it to, and on which appear the results. These eight pins are called the DATA BUS, which is bi-directional, that is, the device can listen to these pins or talk to them.

To explain the rest of the wires, I invite you to imagine a little scenario. You have an office. Outside is a waiting room. Inside, by the door, are a red light, a shrill doorbell which you can't turn off, and a pleasand one which you can. These connect to buttons outside. The one connected to the red light is labelled "RESET". The one for the shrill bell is labelled "UNMASKABLE INTERRUPT". The one for the nice bell is labelled "MASKABLE INTERRUPT".

There is a clock on the wall. Normally, every time it ticks, you do something. You have a desk. On it is a blotter where you do most of your work, along with several paper baskets which hold one sheet each. You have a counter on your desk. Outside, but connected to your desk, is a file cabinet. In that cabinet are up to 256 file folders, numbered 0 through 255. In each folder are 256 sheets of paper, also numbered 0 through 255. On each sheet are eight marks, which may be any combination of ones or zeros. You are never allowed to remove anything from the cabinet. You can make all the copies you want, however, and in part of the cabinet are some file folders that you can write on once you've read them.

These writable sheets comprise a random access memory, or RAM. The copy-only sheets are read-only memory, or ROM. Eight wires connect the cabinet to your desk for the purpose of copying sheets, one for each mark. 16 wires connect the cabinet to your desk counter. Eight of them define one folder, and the other eight pick out one sheet in that folder. These wires are controlled by you alone. You either talk on them or stay silent, but you never listen to them. At least one small part of your cabinet contains no paper. Instead, some ordinary logic attached to your 16 counter wires, called the ADDRESS BUS, recognizes when you access the empty locations, and either remembers what you said, if you were talking, or sends you eight bits of something if you were listening. This is the way you communicate with the outside world. A small number of your writable sheets are reserved for temporary storage of sheets (scratchpad) which would otherwise clutter your desk. A cluttered desk is forbidden.

Now let's start a day's work. You enter your office. It is dark and cold. The electrician comes, turns on your heat, and pushes the reset button. Your clock starts ticking, and the red light goes on. You have a blind, instinctive urge to go to your desk counter and put the number in it that you inherited from your maker and wait for the red light to go out. When it does, you copy the sheet from the cabinet pointed to by your counter. It is your first instruction of the day. It is and must be an instruction, for the only way to tell which addresses are instructions, is to make sure the first address always is one. Almost invariably, this is an instruction to read the next two sheets in the cabinet, form a 16 bit word from them, and stuff it into your desk counter, thereby pointing to a different part of the cabinet. This location is where the first instruction of the main program resides. It is in the ROM.

The next few instructions cause you to make your area safe and orderly. Turn on the brakes, turn off all motors and lights, and erase any confusing contents from your writable sheets. You then ask the outside world to send you the state of any jumper-selected options, for example 525 or 625 lines, SECAM or PAL, and ask if the tape is moving. This last may seem absurd, but consider that you might be waking up after a short power dip during rewind.

So far, you have used only one means of communication. The second one is about to happen. A man in a hurry named "frame pulse" rings your shrill doorbell. I must now introduce a second desk counter. You set it while you were tidying up, and it points to a small part of the writable sheets. It is an automatic counter. After you write something on one of those sheets to which it points, it decreases one. When you want to copy from there, it advances one, and lets you copy. Thus this part of the cabinet appears as if it were a stack of sheets on your desk, with the most recent copy stacked on top. It is, in fact, called a STACK, and the counter that points to it is called the STACK POINTER.

When you finish the one step you are doing, you become aware of the shrill bell. Automatically, you store away your desk counter's two bytes onto the stack. You now set your desk counter to another built-in number which you inherited. Just as in the case of waking up, you go there to find out not WHAT to do, but rather WHERE to go to find out what to do next. This is called a VECTOR, in this case an INTERRUPT VECTOR since you were interrupted by the doorbell. There is a separate vector for the pleasant bell.

The job you were doing before the doorbell rang is called the BACKGROUND TASK. Now, as a result of the frame pulse interrupt, you are doing an INTERRUPT SERVICE ROUTINE, perhaps updating the time code generator. If more than one person knows where the doorbell button is, you must ask: "who's there" when it rings. This is easy enough, since there is another means of talking and listening to the world outside.

So your day goes, listening to buttons, sensors, and time code readers...answering the door to handle time related tasks...sensibly waking up and going to sleep. You who know better might notice that I have not included two tasks for which microprocessors are not well adapted. These are: doing anything really fast, and marking time. Marking time means watching the clock and counting ticks. It leaves too little time for proper work.

For these tasks, we hire underlings who sit in the waiting room and do specific not-so-smart tasks. They are called PERIPHERALS. One is a set of eight-bit input/output ports. They connect to the outside world and are programmable only to the extent that they can be told to talk or listen. Another will accept a byte and send it out one bit at a time in teletype format and will accept serial data and tell when it has a byte-full. Another is a timer chip which has several fairly large counters, which, given a number, can act as a digital one-shot, or supply low-frequency square waves derived from the same clock as the one on your wall. It can be used to measure the time between pulses, as in the case of determining tape speed by looking at tachometer pulses.

There is even a chip which will generate sync pulses, blanking, and legible characters on a raster-scan TV. It communicates with you in a way I haven't mentioned before, equivalent to an intelligent secretary who manages your file cabinet. She is a direct memory access controller, or MDA. You send her to a starting place in the file cabinet and tell her how many sheets to copy and send. She then politely asks you to shut up while she does her job. You, if you agree, wave OK (on a special pin), and shut down your address bus so the DMA device can riffle through your file cabinet, copying at about one microsecond per sheet. This represents the only case where you pass control of your file cabinet to anyone else.

There are three classes of things you have to do. The simplest are those you can do right on your desk. Move something from a basket to the blotter in front of you, or add something to what's in front of you, or compare something in a basket to what's in front of you. These tasks require only one byte of instruction. Others require two byes; what to do, and something to do it TO that still lives in the cabinet. A third class takes three bytes...what to do, and WHERE to GO to do it. The major decision-making power of the device is the ability to leave the normal sequence of instructions, and JUMP to a new set elsewhere in the cabinet.

When your boss says: "come to the front office", that is an UNCONDITIONAL jump. If he says: "come when you have a minute", that is a CONDITIONAL jump. If he says "show this visitor around like you've done before, then get back to work", that is a SUBROUTINE jump, or subroutine CALL. The difference is in whether you bother to remember what you were doing and where you were doing it. Jumps and calls can be based on the status register on your blotter. Jump if the answer were true, or if false. Jump if the result were too big or too small...the list is long. In this ability lies the greatest power of a microprocessor.

There may come the day when you get sick, or someone fouls up your file cabinet or someone outside lies to you, or thinks that you are lying to him, and the doctor is called. You are now that doctor, probably unable to even converse with your patient. Here's what you do with your stethoscope:

First.....Is the patient warm?...check the power and ground pins.

Second.....Is his heart beating?...check the clock.

Third.....Is anyone leaning on the reset or interrupt buttons?

Fourth.....Check the data bus. All line should be wiggling.

Fifth.....Check the address bus....most of them should be wiggling.

Sixth.....Check the input ports....is someone out there lying?

Seventh.....Check the output ports...are they speaking?

Major components of the system are often mounted in sockets. Pry them out and reinsert them to assure good contact. If you are lucky, the system includes a self-diagnostic program which can further isolate the problem. About the worst that can happen is that someone has messed up the file cabinet. Most of the ROM memories used in the systems familiar to us are the ultraviolet eraseable types, programmed by the machine's designer. When programmed, the programming device calculates a check sum of its contents. If you have a programmer like his, ask for the sum, and check your memory. If not, compare your suspect memory against one from an identical machine. Use a ROM programmer, or simply swap them.

If you are adept at programming, it is tempting to insist that the manufacturer suppy you with a copy of his SOURCE LISTING, an annotated list of each step of the program with comments as to what the programmer intended, usually with the thought of modifying it to tailor it to your particular needs. You will find him reluctant to do so. He put in several man/years generating it, and de-bugging it. He swears by it and will support it. He fears that it will fall into the hands of competitors, and the last thing he wants is several versions of it out in the field, each with its own set of problems which require the attention of his technical support.

If you feel the need to be sufficiently knowledgeable so those who already know about these things can't snow you under, I have this advice: buy yourself a home computer. It will probably wake up speaking a language called BASIC. Learn it...it doesn't take long, but do buy an ASSEMBLER for it, a program which puts you in more intimate touch with the innards of the device, and start writing some simple programs in the machine's own language. Don't worry that it uses a different microprocessor than the one used in your equipment at work. Broadly speaking, if you've seen one, you've seen them all. Alternatively, buy or borrow a microprocessor training course which includes at least a processor and numberic keyboard. It's like learning to bake bread. Books are not enough; you must get your hands in it.

SUMMARY OF VPR-3 FIELD ENGINEERING BULLETINS

1. OBTAINING FEB'S

If your facility is not receiving Field Engineering Bulletins applicable to your equipment contact the nearest AMPEX field office, or write to:

AMPEX CORPORATION
Video Technical Support Group
401 Broadway
Redwood City, California 94063-3199 USA
M.S. 3-46

Include system name, model number, serial number, date of purchase, name and address of your organization. Include the job function to which communication should be addressed.

2. COST

AMPEX Corporation provides product improvement and update information through Field Engineering Bulletins for all Audio-Video Products to its customers worldwide. This service reflects AMPEX's policy of after sales support to insure that maximum performance and reliability is realized by our users. In supplying this information, AMPEX Corporation assumes no obligation or responsibility to supply parts or perform the modifications. Parts may be purchased through AMPEX, and installation assistance can be obtained through your local AMPEX regional office at current AMPEX Field Engineering rates.

3. APPLICABILITY AND RECORDS

Some bulletins provide improved performance, others are applicable only for particular equipment applications. Read the entire FEB before starting any work, and check schematics and parts lists.

4. SUMMARIES

These summaries prepared by the training department are not intended to be used in perfoming the modifications. They summarize the bulletin and provide information on the necessity for the modification, serial or assembly number applicability, and circuit effects.

5. FEB 60929 (8403-01) MODULATOR CLAMP MODIFICATION

1. Applicable to Modulator, PWA 1, p/n 1467010-01(NTSC) and p/n 1467013-01(PAL).
2. The modification prevents possible mis-function of the input clamp.
3. On all VPR-3's shipped before February 1 1984, verify that PWA Pin 89 is disconnected from ground. Verify that PWA Pin 80 is isolated. Leave pin 70 connected to R 319.

6. FEB 60941 (8405-03) PLAYBACK SYNC PWA PROM CHANGE

1. Applicable to Playback Sync PWA 6, p/n 1467060-01 through -03.
2. A new control prom, p/n 1467400-04 (U46) contains timing information to ensure proper playback phasing in Edit mode.

7. FEB 60942 (8405-04) CONTROL TRACK AND CAPSTAN SERVO PWA ADJUSTMENT

1. This procedure applies to all 525 Line Standard Control Track and Capstan Servo PWA 15, p/n 1467150.
2. Mis-adjustment of the control track slicers can cause improper operation of the tape timer or time code reader.
3. With PWA 15 on an extender, and the VPR-3 in STOP, not READY (capstan not servoed), adjust R 107 for -25 mV at TP 4, and R 108 for + 25 mV at TP 1. Return PWA 15 to the card slot and verify proper operation of tape timer and time code reader.

8. FEB 60943 (8405-05) TAPE REMAINING PWA MODIFICATION

1. Applicable to Tape Remaining PWA 19, p/n 1467223-01 through -04.
2. To improve the sensitivity of the line voltage indication, replace 1 k ohm resistors R17 and R21 with two 21 k, 1/8 W, 1% MF resistors, Ampex p/n 062-559.

9. FEB 60944 (8405-06) INPUT VIDEO CLAMP IMPROVEMENT

1. See FEB 60929

10. FEB 60945 (8405-07) AUDIO FREQUENCY RESPONSE IMPROVEMENT

1. Applicable to Audio PWA p/n 1467080-01
2. The following component values are changed to improve the audio response to 18 kHz:
   - C128 and C112 to 680 pf, 300 volt mica, p/n 034-677
   - R259 and R328 to 3.92 kOhm 1/8 W, 1%, p/n 062-961
   - R294 to 100 Ohms, 1/4 W, 5%, p/n 066-812

11. FEB 60946 (8405-08) VIDEO ERASE IMPROVEMENT

1. Applicable to Audio Control PWA 12, p/n 1467120-01 through -05
2. The circuit changes provide increased video erase margin:
   - Replace C72 with a 0.1 uF, 50v, 20% cer. capacitor, p/n 064-653
   - Replace R43 and R148 with 10 kOhm, 1/4 W, 5%, p/n 066-830
   - Cut the trace connecting R111 to R110, and add a wire from the free end of R111 (100 kOhm) to the junction of C42 and U28.

12. FEB 60947 (8405-09) AUDIO 3 TIME CODE IMPROVEMENT

1. Applicable to Audio 3 PWA p/n 1467106-01 and -02
2. To improve the reading of time code at shuttle speeds, remove and discard C69 (51 pF) and C168 (560 pF), and replace R104 with a 10 kOhm. 1/8 W, 1%, p/n 062-983.

13. FEB 60948 (8405-10)(REPLACED BY FEB 60970) AST/24 VOLT POWER SUPPLY RELIABILITY IMPROVEMENT

1. Applicable to AST/24V SUPPLY PWA p/n 1467320-01
2. Circuit changes are made to increase immunity to transients on the +13 volts during power up.

14. FEB 60949 (8405-11) REFERENCE GENERATOR 625 TIMING MODIFICATION

1. Applicable to Reference Generator PWA 16, p/n 1467217-01 through -03.
2. Wiring changes are made to eliminate a timing error caused by improper artwork.

15. FEB 60950 (8405-12) PLAYBACK SYNC PROM CHANGE (PAL)

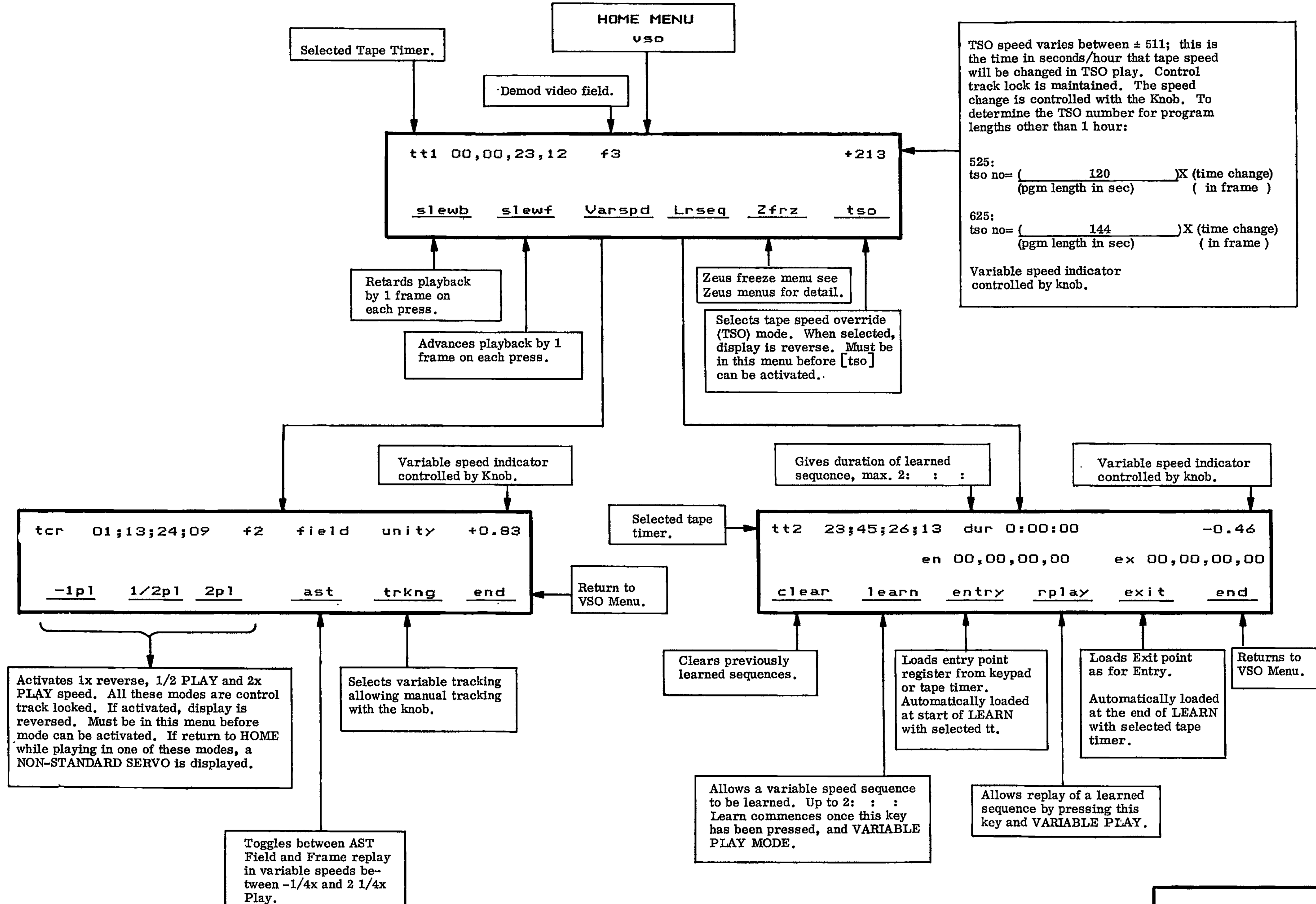
1. Applicable to PAL System Playback Sync PWA 6 p/n 1467050-05
2. Vertical Prom U22 is replaced with p/n 1467404-02 to improve vertical servo performance.

16. FEB 60951 (8405-13) MOTHER BOARD WIRING ERROR

1. Applicable to electronics mother board assembly PWA p/n 1467420-01 through -03.
2. To eliminate a possible wiring error and allow the VITC accessory to receive the blanking command, verify that there is no connection between XA1-80 and XA18-10, and remove if necessary. Verify that there is a connection from XA1-80 to XA18-70.

17. FEB 60952 (8405-14) MONITOR AUDIO CROSSTALK REDUCTION

1. Applicable to Audio Control PWA 12, p/n 1467120-01 through -07.
2. The changes will reduce the audio crosstalk from the monitor head.



VPR-3
OPERATIONS
OPS 4
VSO MENU

18. FEB 60954 (8405-16) CONTROL TRACK/CAPSTAN SERVO MODIFICATION

1. Applicable to Control Track/Capstan Servo. PWA 15, 525 p/n 1467150-01 through -05, 625 p/n 1467153-01 through -05.
2. Implementing the recommended circuit changes eliminates the need to select components when replacing IC's U45 and U52.

19. FEB 60961 (8406-19) AST PROM CHANGE

1. Applicable to AST Servo PWA 7, p/n 1467070-01 through -03.
2. The change allows the AST head to be servo controlled while the VPR-3 is in Record Mode to prevent the possibility of an occasional off-track condition, which could appear as a loss of RF.
3. The following Proms are changed:
   - U 18 to a 1467412-02
   - U 27 to a 1467413-02
   - U 86 to a 1467416-02

20. FEB 60962 (8407-02) TIME CODE READER/GENERATOR MODIFICATION -05

1. Applicable to Time Code Reader/generator PWA 18, p/n 1367180-01 through -04.
2. Circuit changes improve the recorded time code waveform and prevent high frequency oscillation in character generator video.

21. FEB 60963 98407-20 (8407-20) TIME CODE READER MODIFICATION -06

1. Applicable to Time Code Reader/generator PWA 18 p/n 1467180-01 through -05.
2. Replacing U47, PROM, TC Reader, Program, with p/n 1467457-02 improves drop frame/full frame operation.
3. FEB 60964 replaces U47 with a -03 version.

22. FEB 60964 (8407-21) TIME CODE READER/GENERATOR MODIFICATION

1. Applicable to Time Code Reader/generator PWA 18 p/n 1467180-01 through -06.
2. This change corrects character irregularities and compensates for noise on the reset line.
3. Add a capacitor, 0.1 microfarad, 50 V, 20%, Mono, p/n 064-653, from ground to the junction of U74 pin 8 and R103. The capacitor is designated C 88.
4. Replace U 24, PROM, TC Reader, Font, with p/n 1467455-02.
5. Replace U 47, PROM, TC Reader, Program, with p/n 1467457-03.

23. FEB 60969 (8408-22) AST/24 V SUPPLY POWER FAIL MODIFICATIONS.

1. Applicable to AST/24 V Regulator PWA p/n 1467320-01, 02
2. The modification ensures a power fail command if the vacuum compressor stalls due to low voltage, It also ensures a CPU reset after a power failure.

24. FEB 60970 (8405-10B) AST/24 V SUPPLY RELIABILITY IMPROVEMENT (REPLACES FEB 609480

1. Applicable to AST/24 V Supply PWA p/n 1467320-01
2. The modification increases immunity to noise on the + 13 V line, and increases reliability during power-up.

25. FEB 60975 (8409-23) RECOMMENDED AIR SYSTEM MAINTENANCE - VPR-3

1. Applicable to all VPR-3
2. The air system of the VPR-3 is equipped with two five micron air filters. Under normal conditions they should be replaced at least every 500 hours.

26. FEB 60977 (8410-26) AUDIO CHANGES TO AUDIO PWA 3

1. Applicable to Audio 3 PWA (slot 10) p/n 1467080-01. It should be remarked p/n 1467106-06.
2. The modification creates an Audio 3 PWA for primary use with the Time Code Generator/Reader. It provides reliable reading of time code at shuttle speeds, resonates and widens the range of a transformer, and improves high frequency equalization.

27. FEB 60980 (8410-24) C. T. AND CAPSTAN SERVO COUNTER MOD (625)

1. Applicable to Control Track and Capstan Servo PWA 1467156-01 through -04 (625).
2. The modification prevents an erroneous loss of control track pulses which can cause the TBC to switch to the Color Processor momentarily (the VPR-3 generates a VARIABLE command).
3. The preload of counter U 49 is modified. Cut traces at U49-4 and U49-5 to isolate these pins from ground, and connect the two pins to + 5 V. Cut the trace to U49-6 to isolate it from + 5V, and connect U49-6 to ground.

28. FEB 60981 (8410-25) COLOR FRAMING AND SERVO IMPROVEMENT (525)

1. Applicable to Control Track and Capstan Servo PWA 1467150-01 through -08 (NTSC). See FEB 61050 for added information.
2. A small change is made to insure proper color frame start (AST normal) and improve capstan servo response in slow acceleration.
   - Remove capacitor C118.
   - Cut the trace from U44-3, isolating pin 3.
   - Add a 220 K, 5%, ¼ W resistor, AMPEX p/n 066-913, from U44-3 to the trace which was cut. The trace goes to U79-9 and U45-6.

29. FEB 60986 (8411-27) PREVENTION OF DEMOD WHITE FLASHES.

1. Applicable to Demodulator PWA 1467020-01,02 (NTSC) and PWA 1467023-01 through 03 (625). Replaced by FEB 61095.
2. The demodulator clamp circuit is improved to prevent white flashes during playback. Adjustment range of the video level meter is also improved.

30. FEB 60987 (8411-28) TIME CODE READING IMPROVEMENT.

1. Applicable to Audio PWA 1467083-01 through -09.
2. To improve the recovery of time code in fast wind modes, three component values are changed. **R 387** (10 K) is replaced with a 47 ohm, ¼ W, C.F., 5% Resistor, Ampex p/n 066-938. **C 135** (200 pf) is replaced by a capacitor, Cer. mono, 270 pf, 50 V, 1%, Ampex p/n 064-726. **C 166** (680 pf) is replaced with capacitor, Cer., mono, 150 pf, 50 V, 1%, Ampex p/n 064-686.

31. FEB 60988 (8411-29) SYNC EDIT ERASE MODIFICATION

1. Applicable to Edit Erase PWA, p/n 1467630-01.
2. To prevent the possibility of Sync Head Edit Erase command not working, remove CR 3 on the Edit Erase PWA (the PWA is located on the transport, near the scanner. Add a jumper wire in place of the diode.

32. FEB 60989 (8411-30) REFERENCE GENERATOR MODIFICATION (625)

1. Applicable to 625 Reference Generator, PWA 16, p/n 1467217-01 through -03.
2. To improve timing, cut the trace at U 83-6 and U 72-4. Add a jumper wire from U 83-7 to U72-3. Add a jumper wire from U 72-4 to U 83-9.

33. FEB 60990 (8411-32) AUDIO MONITOR CROSSTALK REDUCTION

1. Applicable to Audio Control PWA 12, p/n 1467120-01 through -07.
2. Component changes are made to reduce the monitor gain to reduce audio crosstalk into the monitor.

34. FEB 60992 (8411-31) AUDIO HARMONIC DISTORTION IMPROVEMENT.

1. Applicable to AUDIO PWA, p/n 1467083-01 through -05.
2. Performance of the FEB results in a slight improvement in second harmonic distortion.

35. FEB 60996 (8412-32) PRE-PROC MODE SYNC CHANNEL IMPROVEMENT.

1. Applicable to VPR-3 with Sync Processor PWA 1467063-01.
2. Minor circuit changes are made to improve sync channel operation in pre-processing mode. Small hook-up wire is all that is needed.

36. FEB 60993 (8412-34) AUDIO CONTROL PWA MODIFICATION.

1. Applicable to VPR-3 with Audio Control PWA 1467120-01 through -08.

2. To improve ramping of erase current, prevent possible reset latch up, and to eliminate negative voltage at the A/D converter, components are added and changed.

37. FEB 60995 (8501-37) VACUUM PUMP VANE CHECK

1. Applicable to all VPR-3's through serial number 550.

2. It has been found that carbon vanes on GAST vacuum pumps with serial numbers 08/83, 09/83, 10/83, 04/84, 05/84, and 06/84 may be too soft, resulting in premature failure of the vanes, or clogging of the filter. a replacement kit is available from AMPEX.

3. **NOTE:** In all cases, new vanes will wear rapidly during the first 50-100 hours until they are properly seated. During this time, it may be necessary to replace the output filter. The filter should be inspected frequently during this time.

38. FEB 60997 (8501-35) CONTROL PANEL MODIFICATION

1. Applicable to Control Panel Input/Output PWA 1467570-01 and -02.

2. A ground wire added between two traces reduces audio noise pick-up.

39. FEB 60979 (8501-36) AUDIO 4 TO C. T. CROSSTALK IMPROVEMENT.

1. Applicable to 625 C. T./Capstan Servo PWA 1467156-01.

2. Component changes are made which allow better adjustment for minimum audio 4 to control track crosstalk.

40. FEB 60999 (8501-33) USER SETUP LEARN INFORMATION

1. Applicable to VPR-3's with expanded diagnostics 4.0 software installed.

2. User setup learn mode allows programming a number of soft key modes, then being able to select this operating mode with a single key. The FEB provides information pending an instruction manual update.

41. FEB 61005 (8502-38) REEL/SCANNER SERVO MODIFICATION

1. Applicable to Reel/Scanner Servo PWA 1467140-01 through -05 (NTSC) and 1467143-01 through -05 (PAL).

2. This modification was included in the 3.0 software kit. It reduces tension until the scanner is up to speed to reduce the possibility of head clogs.

3. On both versions, replace C16 (0.22) with a 0.33 UF capacitor, AMPEX P/N 064-797. On PWA 1467140 (NTSC), replace R100 (39 k) with a 23.7 K, 1/8 W, 1% resistor AMPEX p/n 066-003. On PWA 1467143 (PAL), replace R 100 (39 K) with a 28.7 K, 1/8 W, 1% resistor.

42. FEB 61012 (8503-42) AUDIO PWA MODIFICATION

1. Applicable to VPR-3 with AUDIO PWA 1467083-09 through -12.
2. To improve low frequency response below 200 Hz C180, C182, R409, and R410 are added to the network between U62-7 and U34-7.

43. FEB 61013 (8503-43) AUDIO CONTROL PWA MODIFICATION

1. Applicable to VPR-3 with AUDIO CONTROL PWA 1467120-01 through -09.
2. To eliminate monitor amplifier oscillation, capacitor C138, AMPEX p/n 064-684, 100 pF, 50 V, ceramic, is added from U13-16 to ground.

44. FEB 61014 (8503-41) AUTOCHROMA PWA MODIFICATION

1. Applicable to VPR-3 with AUTO CHROMA PWA 1467040-01 and -02.
2. To increase the range of autochroma for operation with sync channel, R48 is changed from 5.1 kOhm to 200K, 1/4 watt, 5%, AMPEX p/n 066-853.

45. FEB 61020 (8502-39) VPR-3 MENU TREE

1. Applicable to all VPR-3 with version P4.0 software.
2. A menu tree offers a clear view of the software menus, included those added by P4.0, such as animate and user set-up.

46. FEB 61021 (8504-46) PRE-PROC KIT (PLAYBACK SYNC PWA).

1. Applicable to VPR-3 with Playback Sync PWA 1467060 (all dash numbers).
2. A kit, P/B sync with pre-processing, AMPEX p/n 1467261-01, allows proper gating of various signals during the pre-processing mode of the VPR-3. Pre-processing (Video SET-UP menu) provides time base correction of signals prior to recording.

47. FEB 61022 (8503-44) MODULATOR IC CHANGE

1. Applicable to VPR-3 525 Modulator PWA 1467010-01, 02, and 625 Modulator PWA 1467013-01, 02, and 03.
2. IC U50 has been changed because of a marginal high level input on pins 2, 3 of some IC's. It should not be necessary to perform this modification unless U50 is changed.
3. Replace U50 (MC 14456B or CD 4556B) with a 74HCT139, AMPEX p/n 003-237.

48. FEB 61023 (8506-49) CAPSTAN/SCANNER MDA MODIFICATION.

1. Applicable to VPR-3 with CAPSTAN/SCANNER MDA 1467340-01 throught -05.
2. The -13 volt connection to U13 is changed to a "cleaner" power source to prevent possible crosstalk which may cause the scanner to rephase during shuttle mode.
3. Cut the trace at U13-4 on the component side of the board between the two feed through holes to the left of TP-11. On the bottom of the PWA add a small wire from the feed-thru hole still connected to U13-4 to the negative lead of C29.

49. FEB 61026 (8503-45) REGULATOR PWA RESISTOR CHANGE

1. Applicable to VPR-3's with REGULATOR PWA 1467310-01 through -03.
2. To increase the current output of the +5 volt supply before current limiting occurs, replace R52 and R54 (249K ohms) with Resistor, 205K ohm, 1%, 1/8 W, AMPEX p/n 066-154.

50. FEB 61029 (8504-47) REGULATOR PWA INDUCTOR CHECK

1. Applicable to all VPR-3's with REGULATOR PWA 1467310 shipped before 1 April 1985.
2. Insulating washers and standoffs have been added to the inductors on the REGULATOR PWA to prevent the possibility of the inductors shorting to the PWA. All of these PWA's should be inspected per the procedures in the FEB.
3. VPR-3's manufactured after 1 April 1985 will have a yellow dot above L6 to indicate that the Regulator PWA has been inspected.

51. FEB 61030 (G-8504-1) STATIC ELECTRICITY INFORMATION

1. Applicable to all equipment with static sensitive components.
2. AMPEX is strongly recommending a comprehensive program of properly handling and servicing static sensitive components. The information in the FIELD ENGINEERING BULLETIN is based on vendor recommendations and exhaustive testing conducted by AMPEX. All solid state devices, and especially FET and CMOS devices, can be damaged by static electricity. Precision metal film resistors can also be damaged. The power MOSFETS used in the VPR-3 motor MDA's are susceptible, and must be handled properly to avoid catastrophic failure. Devices can be damaged in such a way that they will fail within a short time.

52. FEB 61032 (8507-51) SYNC EQUALIZER PWA MODIFICATION.

1. Applicable to 525 Sync Equalizer PWA 1467030-01, -02; and 625 Sync equalizer PWA 1467033-01, 02.
2. To improve head switching of the sync channel during variable speed operation, C144 (0.01 microfarad) is replaced with a capacitor, 1.0 microfarad, 50 volt, AMPEX p/n 064-314.

53. FEB 61034 (8507-50) LOW SERVO GAIN KIT

1. Applicable to all VPR3's with 4.0 and above software, and REEL AND SCANNER PWA, NTSC 1467140, PAL 1467143, all dash numbers.
2. The kit, p/n 1467782-01, allows reducing the reel acceleration via a soft key to better handle tapes which have edge damage or other defects which result in a loose tape pack.

54. FEB 61035 (8504-48) CONTROL PWA 1467203 SCHEMATICS AND PARTS LIST

1. Applicable to all VPR-3's with expanded diagnostics (4.0 Software).
2. The FEB provides a schematic (1467205) and LM for the new control PWA 1467203, which is not included in Parts List and Schematics Manual 1809608.

55. FEB 61041 (8506-17B*) A1-A2 MIX MODIFICATION

1. Applicable to all VPR-3's with AUDIO PWA 1467080-01 through -03.
2. Recommended circuit changes provide balanced A1-A2 mix performance.

56. FEB 61050 (8508-25B*) COLOR FRAMING AND SERVO IMPROVEMENT

1. Applicable to all VPR-3's with NTSC Control Track and Capstan Servo PWA 1467150-01 through -08. Adds information to FEB 60981.
2. A small change is made to insure proper color frame start (AST normal) and improve capstan servo response in slow acceleration.
   - Remove capacitor C118.
   - Cut the trace from U44-3, isolating pin 3.
   - Add a 220 K, 5%, ¼ W resistor, AMPEX p/n 066-913, from U44-3 to the trace which was cut. The trace goes to U79-9 and U45-6.
   - Replace R45 (56.2 K) with 100 K, 1/4 W, 1% MF resistor, Ampex p/n 062-601.
   - Replace R44 (1 K) with 3.01 K, 1/4 W, 1% MF resistor, Ampex p/n 062-639.

57. FEB 61054 (BP-8511-52) VPR-3 MODULATOR PWA 525/625

1. Applicable to VPR-3's with Modulator PWA 1467010-01 through -04 for 525 and 1467013-01 through -05 for 625.
2. Circuit changes are made to eliminate the need for selecting IC U27 to ensure proper clamping.
3. Isolate pins 1 and 2 of IC U27. Add a wire to connect U27-1 to U27-5. Connect U27-2 to +5 Volts.

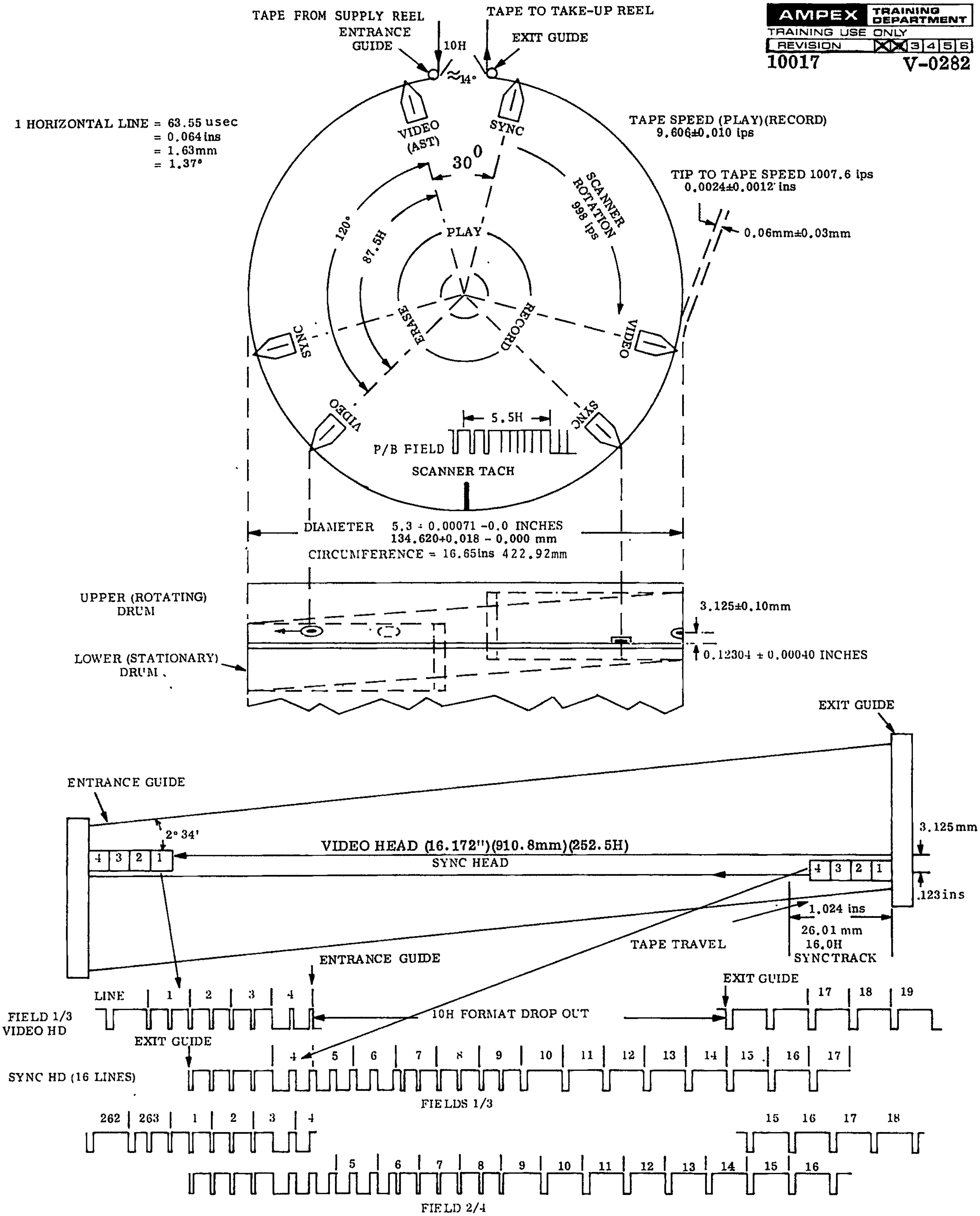
58. FEB 61095 (BP-8411-27B) PREVENTION OF DEMOD WHITE FLASHES

1. Applicable to VPR-3's with Demodulator PWA 1467020-01 and -02 (525), and 1467023-01 through -03(625).
2. This FEB replaces FEB 60986 (BP 8411-27), and provides a piggyback to prevent white flashes during playback. It also allows a better range of adjustment for the Video Level Meter.

VPR-3
CUSTOMER OPTION
UPDATE KITS

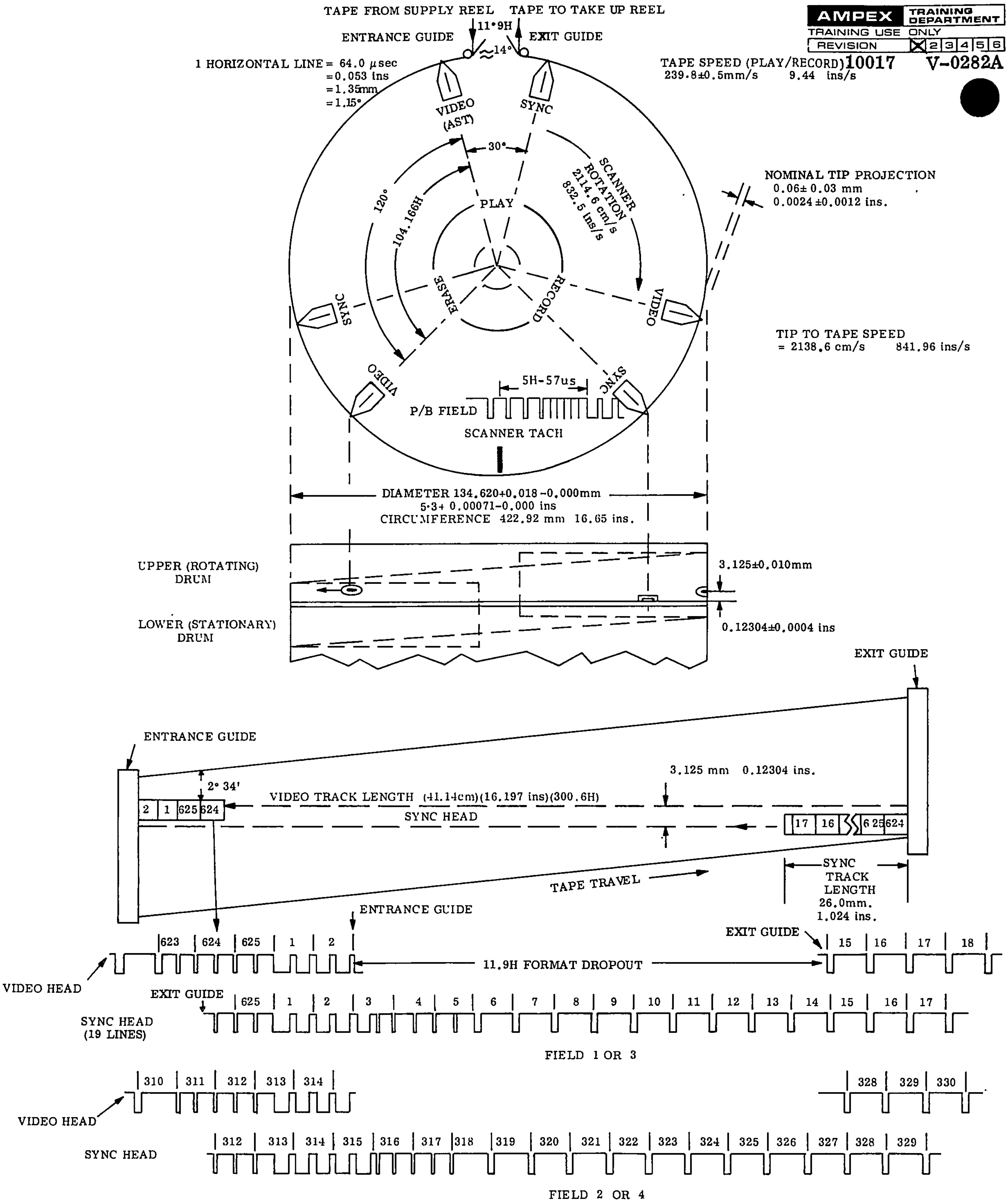
	KIT TITLE, PURPOSE AND PART NUMBER	SYMPTOM	APPLICATION
1.	Kit Demod/Chroma level control 1467097-01	Required where customers prefer chroma level instead of demo level control on the control panel.	All systems except ABC which has this mod already installed.
2.	Speaker collar assembly ABC 1467990-01	All standard ABC consoles have no high fidelity speakers because there is no collar between mon bridge and lowboy.	If collar is required to raise monitor bridge. This assembly includes hi fidelity speakers (no power amplifier included)
3.	Kit, vertical interval time code 1467720-01	If customer chooses to update his time code reader by adding VITC piggyback assembly.	Customer must have kit 1467700 (TC read/gen without VITC).
4.	Kit, update air system 1467765-02	If customer chooses to update air system to include quick mount, extra large filters, and auto flow regulation by adding these components.	All air systems without extra large filters.
5.	Kit, low servo gain 1467782-01	Required where customers need to switch to low reel servo gain because of loose reel tape packs.	All systems if requested by the customer.
6.	Kit, P/B sync with pre processing 1467261-01	Required if customer needs to have pre processing mode activated. Later software made this feature available.	All systems that shipped with version 1467160 P/B sync.
7.	Kit, A3/TCRG auto setup 1467118-01	Allows auto setup with T.C.R. board installed adjust per time code level.	All systems with audio PWA 1467083
8.	Kit, vid/sync rec. cont. switch 1467099-01	Elimates manual optimize switch and allows automatic selection of video/sync record current thru software control.	All systems having modulator 1467010-01 thru -05, or 1467013-01 thru -06 inclusive.

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 3 4 5 6
10017 V-0282



NOMINAL VIDEO RECORDING ON TAPE

C- FORMAT 525


TAPE FROM SUPPLY REEL
TAPE TO TAKE UP REEL
11.9H
ENTRANCE GUIDE
EXIT GUIDE
14°
1 HORIZONTAL LINE = 64.0 μsec
= 0.053 ins
= 1.35mm
= 1.15°
TAPE SPEED (PLAY/RECORD)
239.8±0.5mm/s 9.44 ins/s
VIDEO (AST)
SYNC
30°
120°
104.166H
PLAY
SCANNER ROTATION
2114.6 cm/s
832.5 ins/s
NOMINAL TIP PROJECTION
0.06± 0.03 mm
0.0024 ±0.0012 ins.
ERASE
RECORD
SYNC
VIDEO
VIDEO
SYNC
TIP TO TAPE SPEED
= 2138.6 cm/s 841.96 ins/s
5H-57us
P/B FIELD
SCANNER TACH
DIAMETER 134.620+0.018 -0.000mm
5.3+ 0.00071-0.000 ins
CIRCUMFERENCE 422.92 mm 16.65 ins.
UPPER (ROTATING) DRUM
LOWER (STATIONARY) DRUM
3.125±0.010mm
0.12304±0.0004 ins
EXIT GUIDE
ENTRANCE GUIDE
2° 34'
3.125 mm 0.12304 ins.
VIDEO TRACK LENGTH (41.14cm)(16.197 ins)(300.6H)
SYNC HEAD
2 1 625 624
17 16 6 25 624
SYNC TRACK LENGTH 26.0mm. 1.024 ins.
TAPE TRAVEL
ENTRANCE GUIDE
EXIT GUIDE
623 624 625 1 2
15 16 17 18
11.9H FORMAT DROPOUT
VIDEO HEAD
EXIT GUIDE
625 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
SYNC HEAD (19 LINES)
FIELD 1 OR 3
310 311 312 313 314
328 329 330
VIDEO HEAD
312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329
SYNC HEAD
FIELD 2 OR 4

C FORMAT 625

I. THE SMPTE 525 C FORMAT

1. This is a summary of the C Format specifications covered in the following documents.

   a. AMERICAN NATIONAL STANDARDS

      (1) ANSI C98.18M-1979: Basic system and transport geometry parameter for 1 inch Type C Helical Scan videotape recording, August 9, 1979.

      (2) ANSI C98.19M-1979: Dimensions and location of records for 1 inch Type C Helical Scan videotape recording, August 9, 1979.

      (3) ANSI C98.20M-1979: Frequency response and reference level of recorders and reproducers for audio records for 1 inch Type C Helical Scan videotape recording, August 9, 1979.

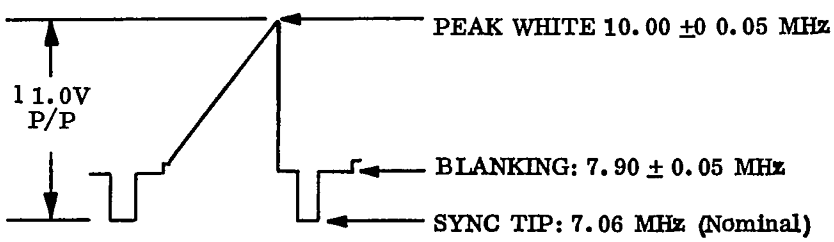
   b. SMPTE RECOMMENDED PRACTICES

      (1) RP 85-1979: Tracking-control Record for 1 inch Type C Helical Scan videotape recording, February 1, 1979.

      (2) RP 86-1979: Video Record Parameters for 1 inch Type C Helical Scan videotape recording, February 1, 1979.

2. Figure 1 is a summary of the track dimensions and locations on the one inch wide magnetic tape used for the C Format.

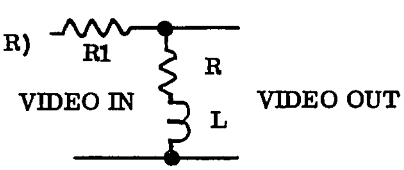
3. As in previous videotape recording systems, the C Format Helical Scan system records frequency modulated (FM) RF signal on the magnetic tape, using a record transducer rotated at high speed across the tape, which is moving at a relatively slow speed. The standard frequencies are similar to those used with high band video recording systems for many years.



   a. Pre-emphasis of the video signal is defined by a network, where

   $t_1 = 240\ \text{ns} = L/(R_1 + R)$

   $t_2 = 600\ \text{ns} = L/R$



   b. The burst has additional pre-emphasis applied, so that the amplitude of the recorded signal during burst time is increased by 6 $\pm$ 0.1 dB (2X), with respect to sync and video, with the phase of burst maintained within $\pm 1^\circ$.

4. Audio tracks 1, 2 and 3 are recorded using bias (anti-hysteresis method).

   a. When the same signal is recorded on Audio #1 and Audio #2 tracks, the tracks are phased to be additive when reproduced by a head wide enough to cover both tracks.

      (1) When separate channels are used for stereo audio, the left channel utilizes Audio 1; the right channel is recorded on Audio 2.

      (2) When the sum and difference method of recording stereo audio is used, left plus right is recorded on Audio 1, and the left minus the right channel on Audio 2.

   b. When Time and Control Code is used, it is recorded on Audio 3.

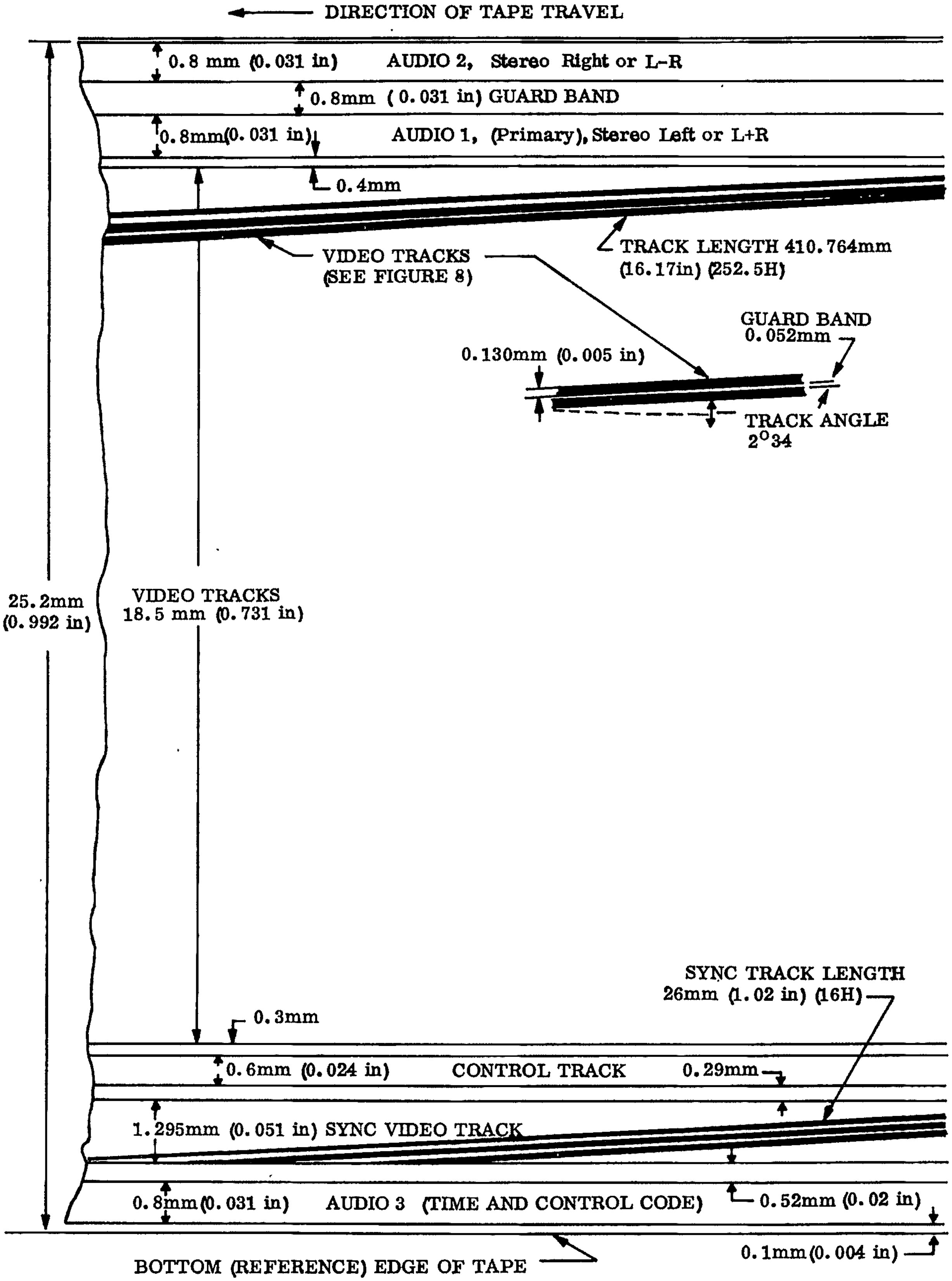


FIGURE 1. RECORD LOCATION, C FORMAT (525/SMPTE)

5. The control track is recorded as a series of constant flux levels alternating in polarity at a field rate, with an extra pair of transitions added on alternate frames. Or, it is a non-biased saturation recording. **The alternate frame identification pulse should identify FIELD I.**

   a. Figure 2 shows the tracking control waveform and timing.

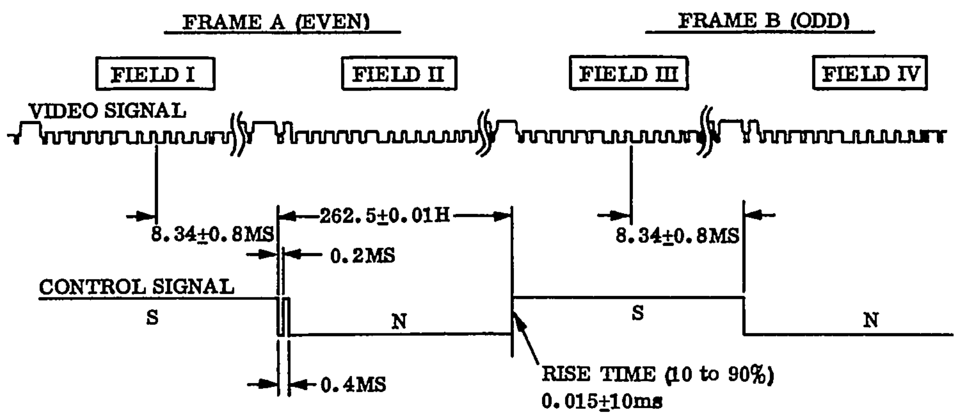
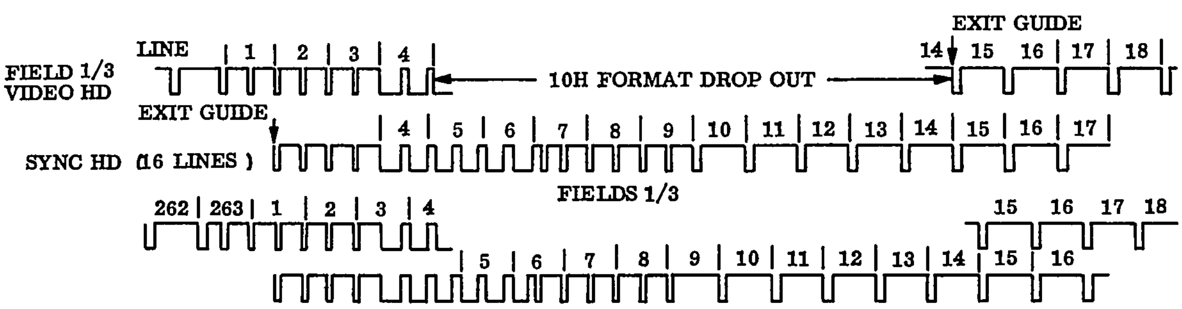


FIGURE 2.TRACKING CONTROL RECORD WAVEFORM

6. In the C Format Helical Scan system, one field of video is recorded during each revolution of the transducer. This video recording contains all active picture information and enough vertical sync information to permit playback synchronization.

   a. Missing information is called the vertical dropout, or sometimes the format dropout. The tape entrance and exit guides are placed to provide a tape wrap around angle so that the dropout is 10 $\pm$ 0.25 horizontal lines, due to the loss of head to tape contact. The dropout is measured between the half amplitude points of the RF envelope recovered from tape.

   b. An optional sync record function can provide all of the information in the vertical interval dropout, including an overlap for playback switching.



FIELD 2/4

FIGURE 3. NOMINAL VIDEO RECORDING ON TAPE

7. The heart of the system is the scanner, a mechanical assembly containing the drums, rotating pole tips, and tape guiding elements used to record and reproduce videotape recordings.

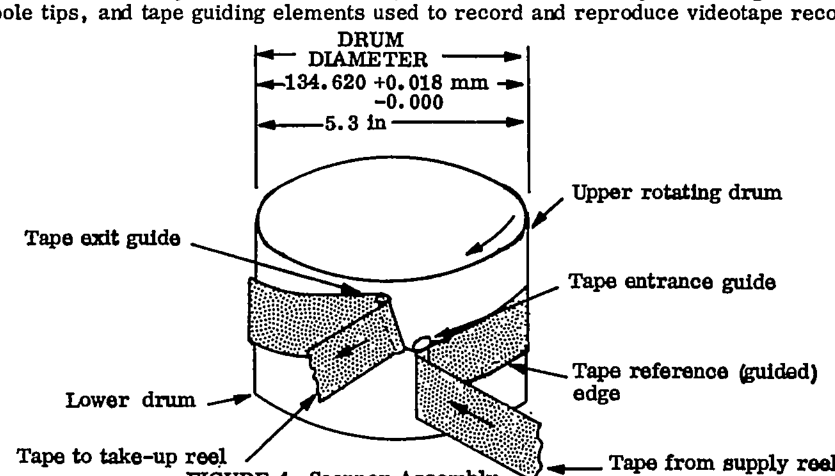


FIGURE 4. Scanner Assembly

a. There is 346° wrap of tape around the scanner. The scanner rotation is tied to vertical - 59.9 Hz. Since the circumference of the drum is 16.65"(423 mm), a tip moves at 998 inches per second (2535 cm/s).

8. The guiding requirements are quite strict. The edge of the video record track must be contained within two parallel straight lines 0.030 mm (0.00118 in.) apart.

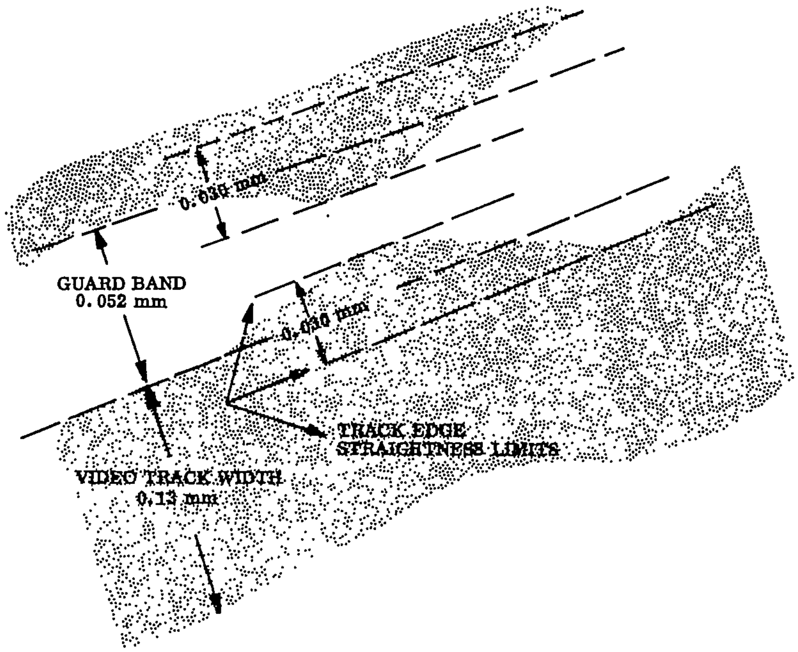


FIGURE 5. Track Straightness

a. Good tape interchange on any VTR is strongly dependent on track straightness, particularly on C Format, where the track is 411 mm (16.17 in.) long. Track straightness is dependent on many factors: entrance and exit guide placement; method of tape guiding around the drum; tension build-up around the drum; tape slitting characteristics.

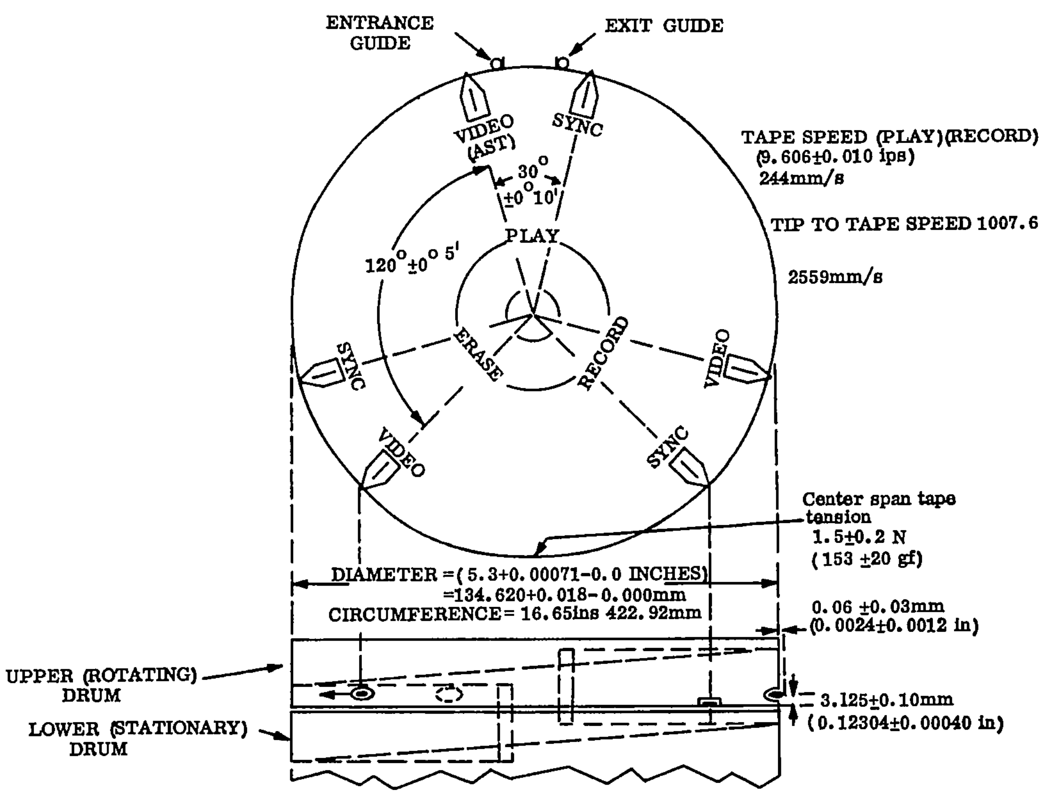


FIGURE 6. TIP LOCATIONS AND DRUM DIMENSIONS

9. Figure 6 shows the tip locations. When an operational pole tip is not required (such as the optional sync heads), a dummy tip is required in that location.

a. Each tip projection shall be 0.06 ± 0.03 mm (0.0024 ± 0.0012 in) measured from the outer surface of the upper drum to the end of the pole tip.

10. The helix angle, 2^{o} 35' 29" $\pm$ 2" is the angle formed between the path of the rotating pole times and the tape reference edge guiding system on the scanner. (Figure 7)

a. The track angle is the angle of video record with respect to the reference edge of the tape, with the tape under normal tension.

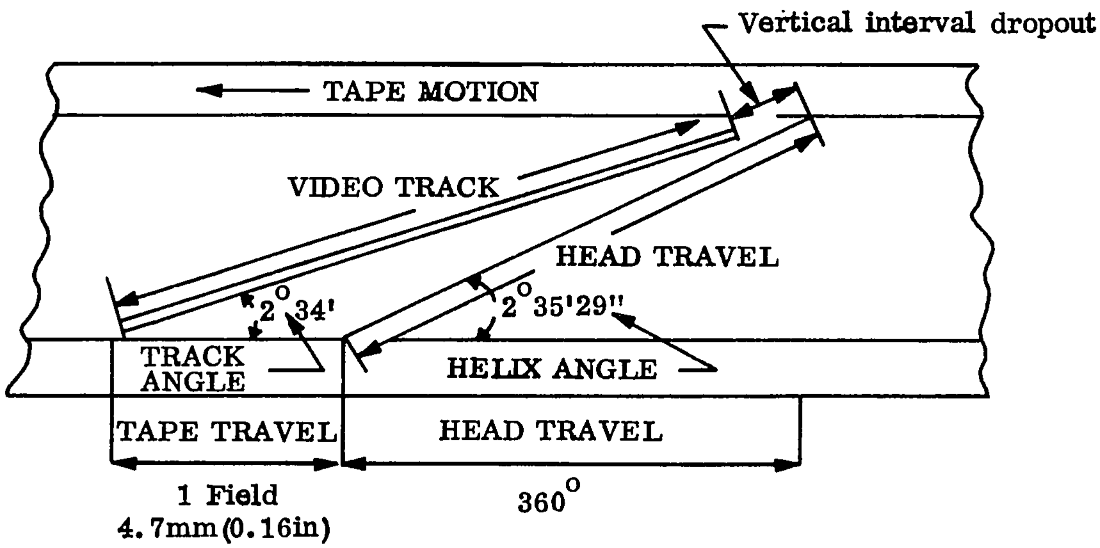


FIGURE 7. Helix angle versus track angle

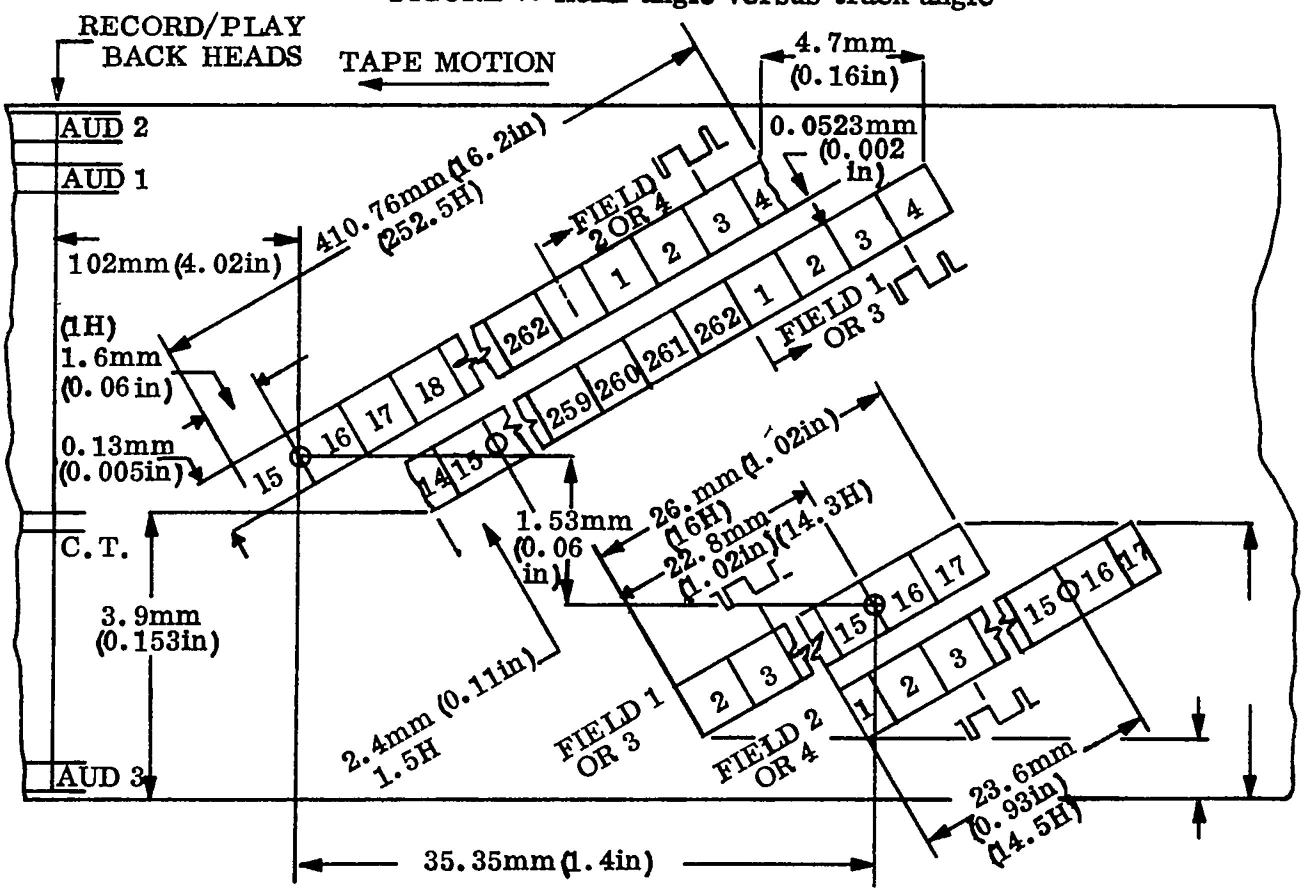


FIGURE 8.
VIDEO AND SYNC RECORD LOCATIONS

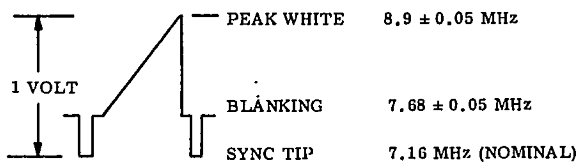
THE EBU 625 PAL/SECAM FORMAT

1. This is a summary of C Format specifications covered by E.B.U. Technical Information Sheet No. 7, "SPECIFICATIONS FOR A HELICAL SCAN NON-SEGMENTED FIELD TELEVISION RECORDING ON 25.4 mm (ONE INCH) TAPE (E.B.U. Format C)".

   a. For the most part, dimensions are given for the center value of the tolerance range.

2. Figure I is a summary of the track dimensions and their location on the 25.4 mm (one inch) wide magnetic tape, including OPTION II, (Sync Track Head), and OPTION III, Audio 4. These are covered in the Appendix to Technical Information Sheet No. 7.

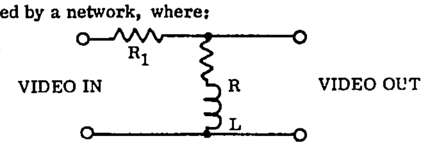
3. As in previous video tape recording systems, the C Format Helical Scan records the video portion of the television signal on magnetic tape as a frequency modulated (FM) Radio Frequency Signal. The record transducer rotates at high speed across the tape, which is moving at a relatively slow speed longitudinally. The standard frequencies are similar to those used with high band video tape recording systems for several years.



   a. Pre-emphasis of the video signal is defined by a network, where:

t_1 = 180 ns = $L/R_1 + R)$

t_2 = 610 ns = L/R



   b. Except in the SECAM system, the burst has additional pre-emphasis applied so that the amplitude of the recorded signal during burst time is increased by 6 ± 0.1 dB (2X) with respect to sync and video. The phase of burst is to be maintained within ± 1°.

4. All audio tracks are identical, and are recorded using bias. The audio leads associated video information by 102.4 mm (4.03inches).

   a. When the same signal is recorded on Audio 1 and Audio 2 tracks, the tracks are phased to be additive when reproduced by a head wide enough to cover both tracks.

   b. Monophonic sound shall be recorded on Audio track 1. Track 2 may carry auxiliary sound.

   c. When seperate channels are used for stereophonic audio, the left channel utilizies Audio 1 track and the right channel is recorded on Audio 2.

   d. When time and control code is used, it is recorded on Audio track 3, using AC bias. Ampex is recommending recording at +3dB over the reference level.

      (1) Tech 3097-E, June 1980 "E.B.U. Time and Control Code for Television Tape-Recordings" covers the characteristics of the code, including the timing relationship between the code and the television signal, particularly with respect to the PAL four and eight field colour.

   e. Option III provides for an additional Audio track 4 instead of the Sync Track (Option II). It is intended that this track shall permit dubbing to and from Audio tracks 1 and 2.

5. The control track is recorded using AC bias.

   a. Figure II shows the tracking control waveform and timing. An edit pulse is included, which defines the PAL eight field colour sequence. The PAL/SECAM four field sequence can be derived from this information.

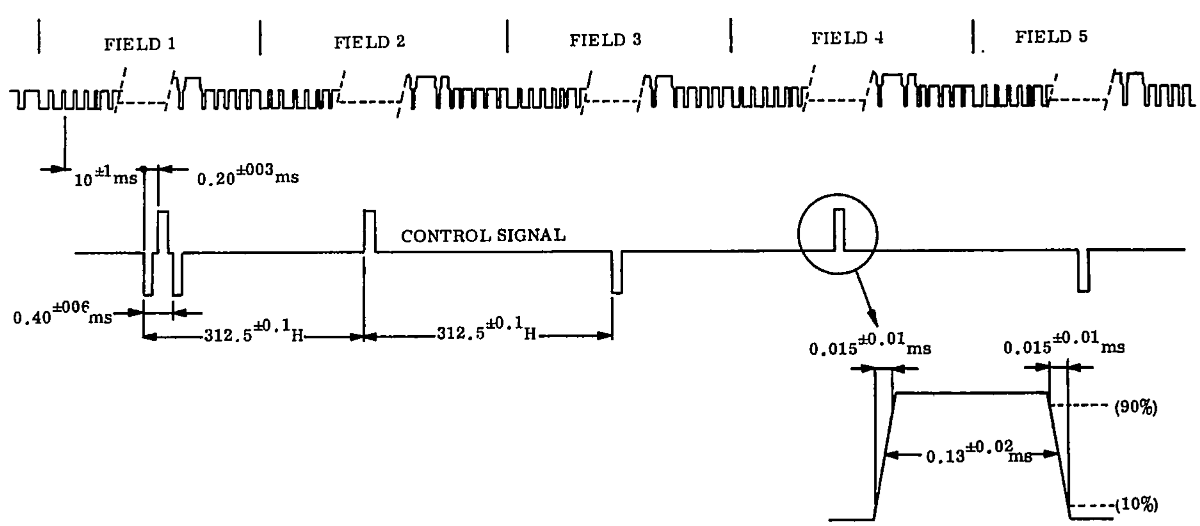


FIGURE II. CONTROL TRACK FORMAT

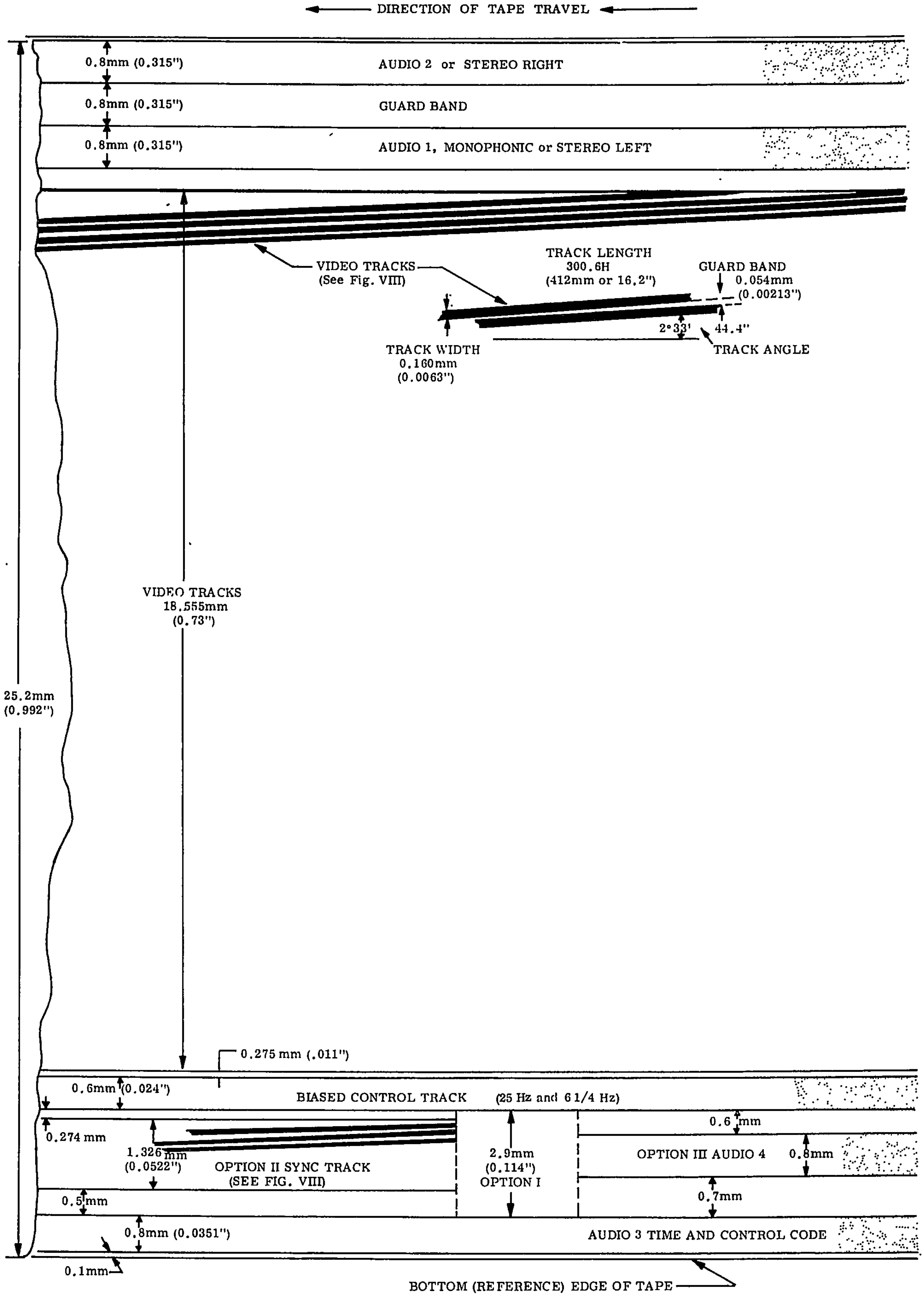


FIGURE I: RECORD LOCATION, EBU C FORMAT (NOT TO SCALE)

In the C Format Helical Scan Systems, one field of video is recorded during each revolution of the video record head. This recording contains all active picture information and enough vertical sync information to permit playback synchronization.

a. Missing information occurs during the vertical interval, and is usually called the format dropout. The tape entrance and exit guides are placed to provide a tape wrap-around angle such that the dropout is a nominal twelve horizontal lines (768 microseconds) due to the loss of head to tape contact. The dropout is measured between the half amplitude points of the RF envelope from the video head. The dropout width will increase in width as the tip wears down.

b. Option II provides for a sync record head. This head will record all the information in the vertical interval gap, including an overlap for playback switching. Figure III shows the dropout with respect to the television signal.

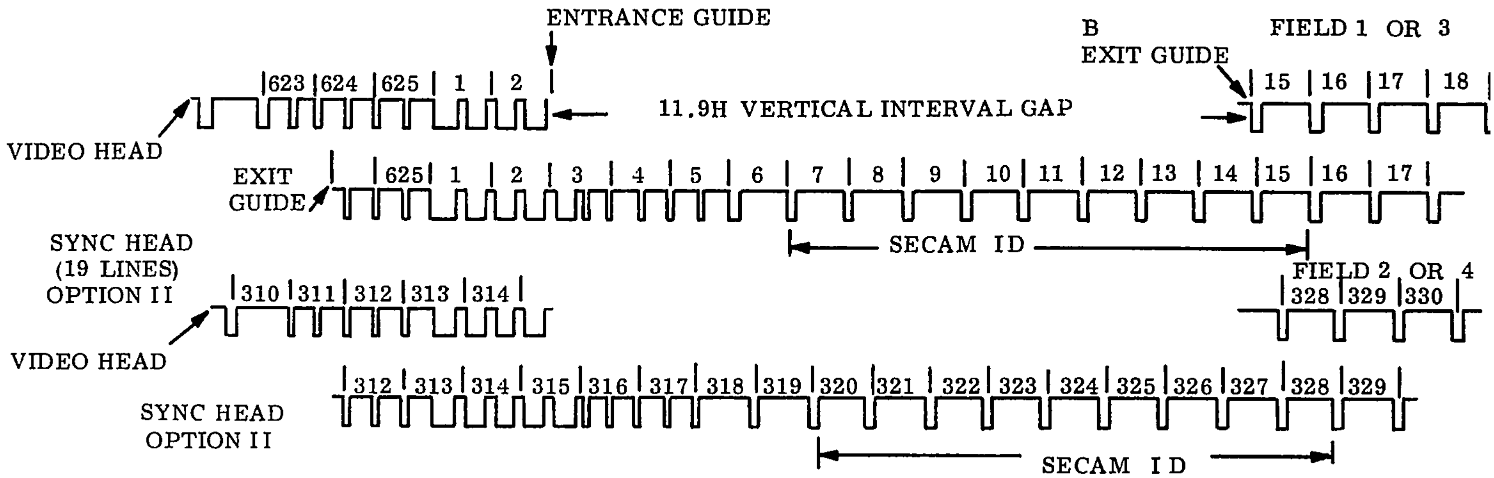


FIGURE III. NOMINAL VIDEO RECORDING ON TAPE

7. The heart of the system is the scanner, a mechanical assembly containing drums, the rotating pole tips, and the tape guiding elements.

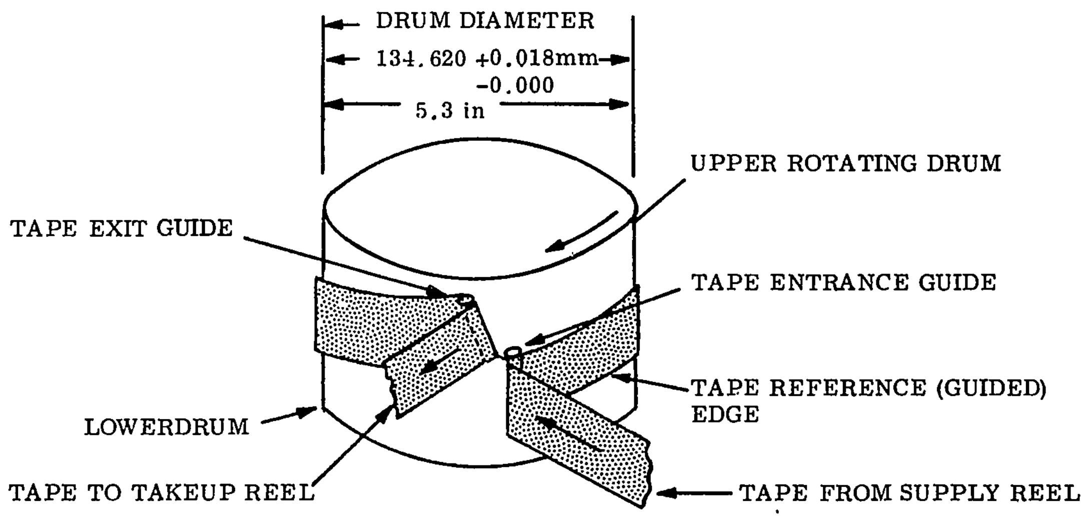


FIGURE IV. SCANNER ASSEMBLY

a. There is a 346° wrap of tape around the scanner. Scanner rotation is tied to the 50 Hz vertical signal. Since the scanner circumference is 422.92 mm (16.65 inches), a tip moves at 2115 cm/s (833.5 ips).

8. The guiding requirements are quite strict. The edge of the recorded track must be contained within two parallel straight lines 0.030 mm apart.

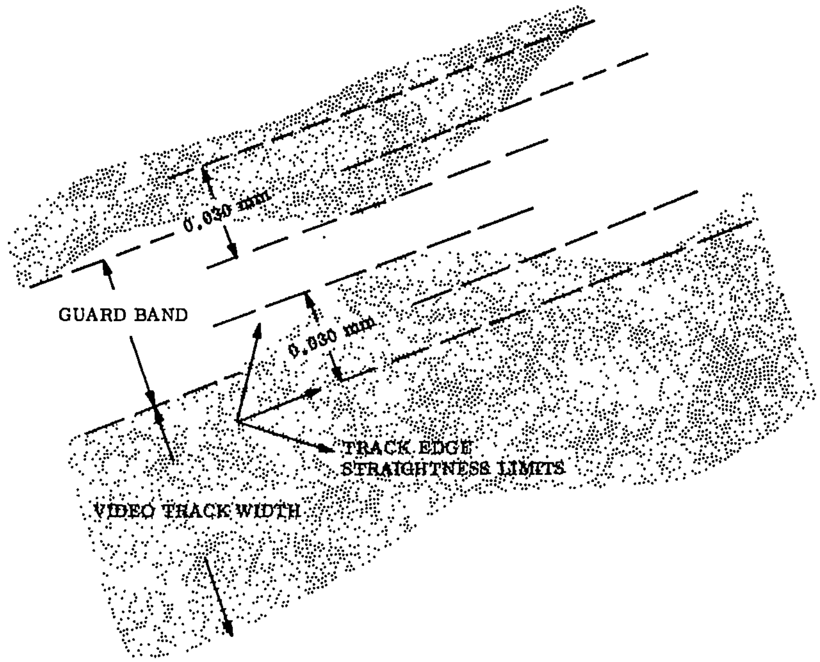


FIGURE V. TRACK STRAIGHTNESS

a. Good tape interchange on any video tape recorder is strongly dependent on track straightness. This is particularly true on the C Format, where the track is about 411 mm (16.2 inches) long. Track straightness is dependent on many factors: entrance and exit guide placements; method of tape guiding around the drum; tension build-up around the drum; tape slitting characteristics.

9. Figure VI shows the tip location. When an operational pole tip is not required (such as the Option II Sync Head), a dummy pole tip is required at that location.

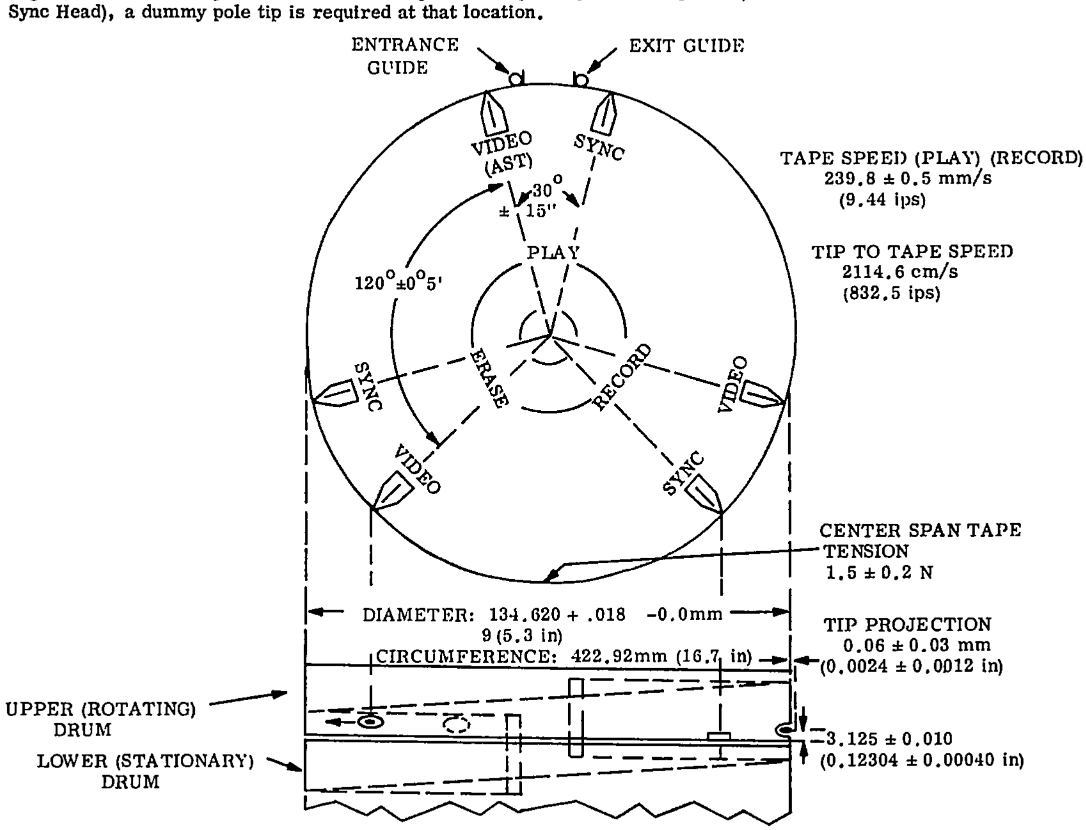


FIGURE VI. TIP LOCATIONS AND DRUM DIMENSIONS.

10. The helix angle, 2° 35' 20", is the angle formed between the path of the rotating poles tips and the tape reference edge guiding system on the scanner, as shown in Figure VII. The track angle is the angle of video record with respect to the reference edge of the tape, while the tape is under normal tension.

a. Calculated tape tension at the center span shall be 1.5 ± 0.2 N. The drum diameter, tape tension, helix angle and tape speed determine the video-track angle. Different methods of design and/or minor variations of some of the parameters shall nevertheless produce equivalent and acceptable recordings for interchange purposes.

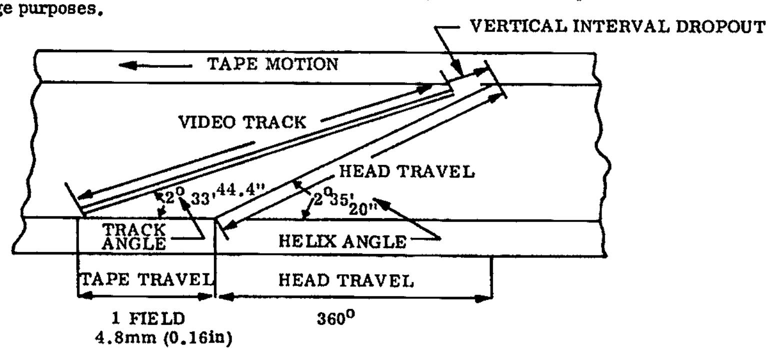


FIGURE VII. HELIX ANGLE VERSUS TRACK ANGLE

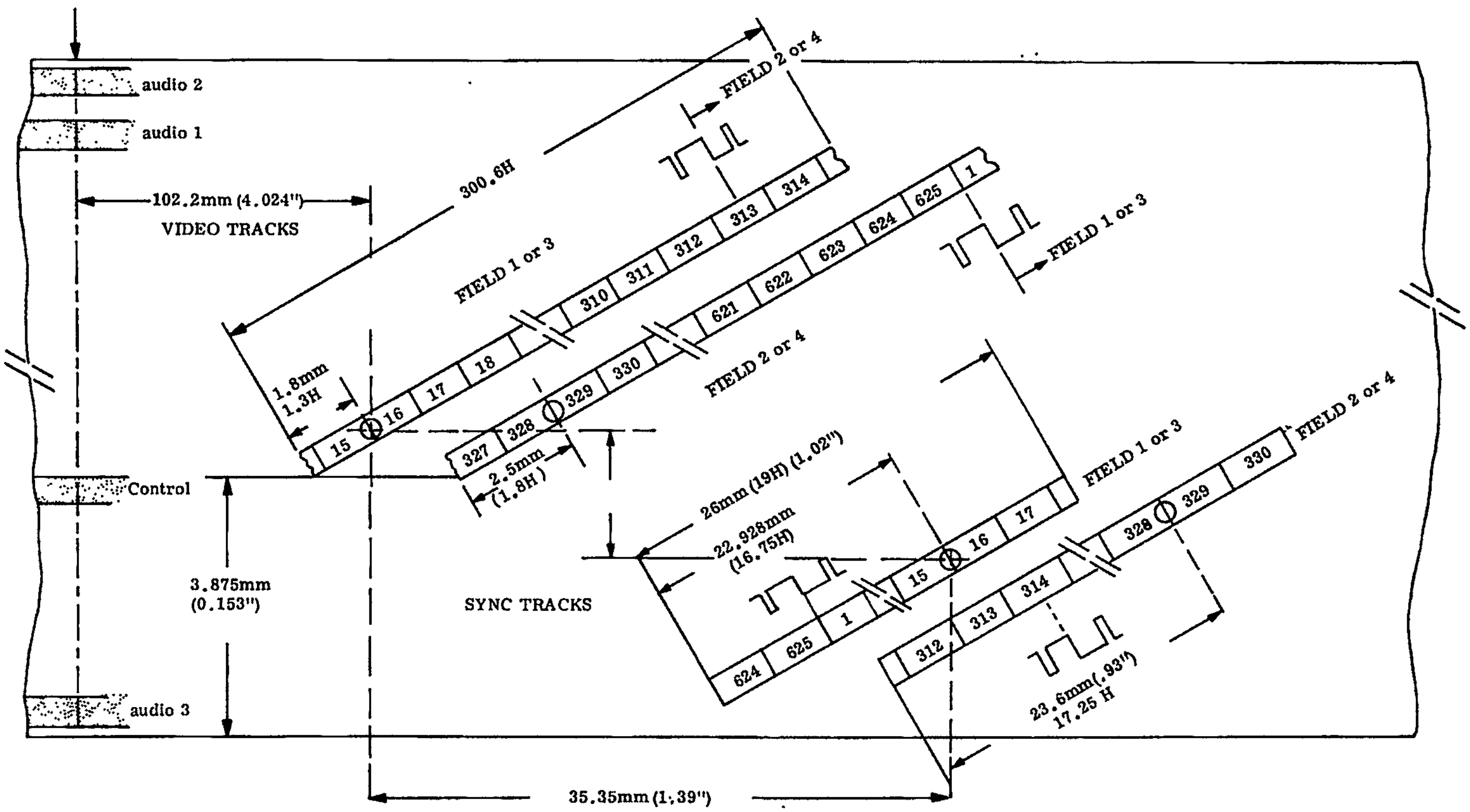
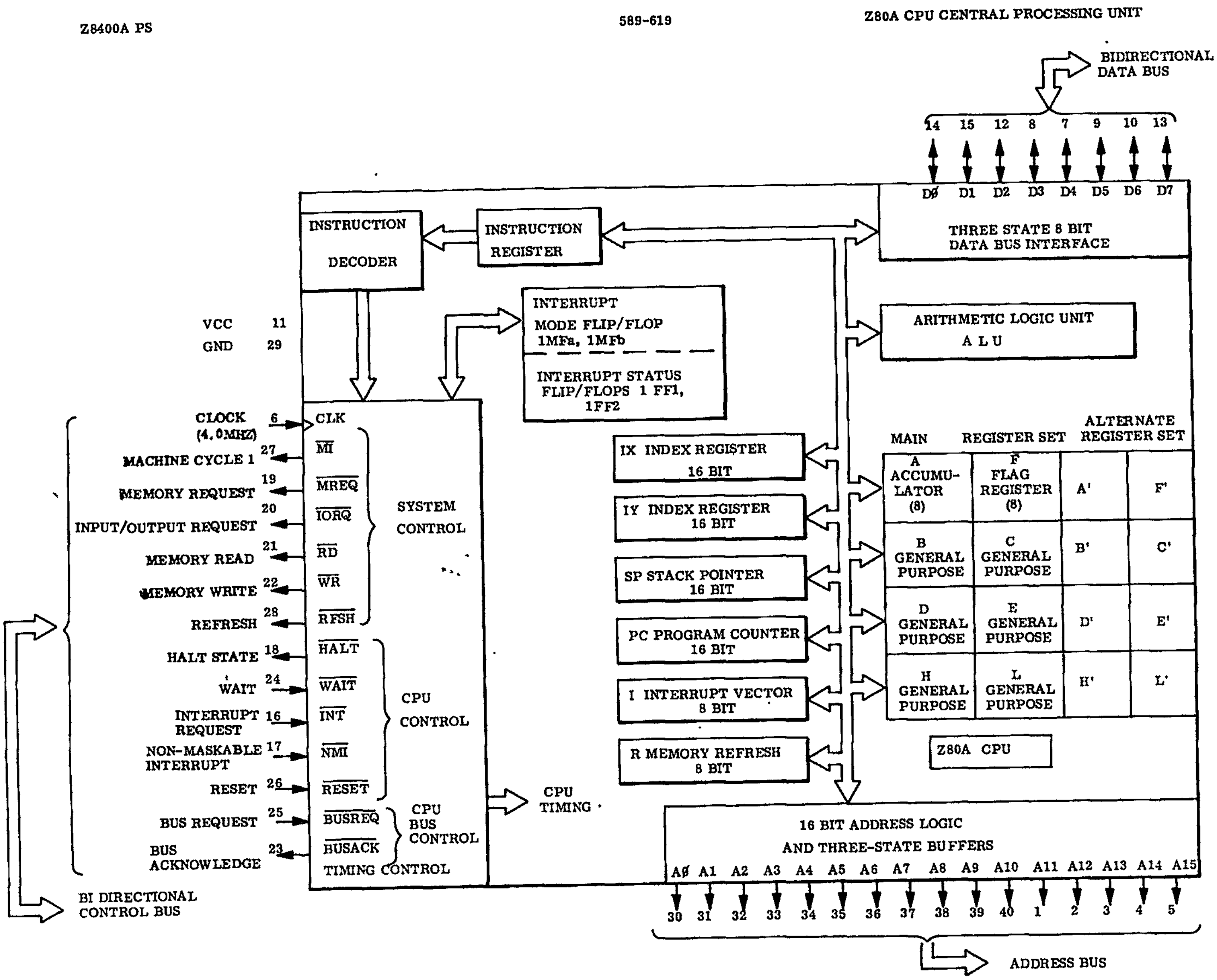


FIGURE VIII. VIDEO AND SYNC RECORD LOCATIONS

The Z80 Central Processing Unit (CPU).

The Z80 microprocessor internal register contains 208 bits of read/write memory accessible to the programmer, including two groups of general purpose registers. These may be used individually as either eight bit registers or as sixteen bit register pairs. There are two sets of accumulator and flag registers. A group of "exchange" instructions makes either set available. The alternate set allows operation in foreground/background mode, or they may be reserved for very fast interrupt response.

The Z80 also has Stack Pointer, Program counter, two Index Registers, a Refresh Register (counter), and an Interrupt Register.



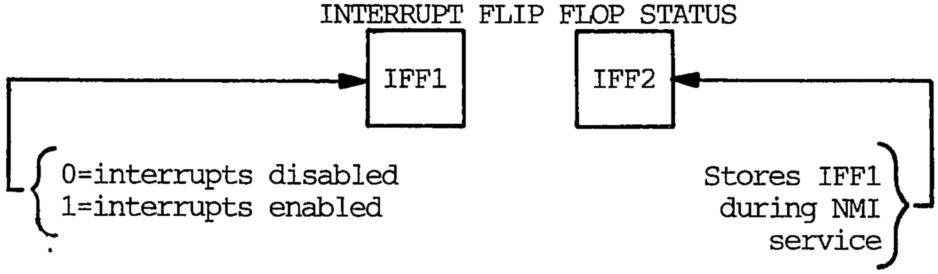
Interrupt Modes

Non-maskable interrupt (NMI) cannot be disabled by program control, but will be accepted at all times by the CPU. It is usually reserved for servicing only the highest priority interrupts, such as shut-down after power failure. If BUSREQ is not active (low), the CPU jumps to restart location 0066H.

Maskable interrupt (INT), when detected, and providing that interrupts are enabled and BUSREQ is not active, generates a special fetch cycle (M1) with IORQ rather than MREQ active.M1 is automatically extended by two WAIT states to allow acknowledgement and to place the interrupt vector on the bus.

1. Interrupt mode flip flops IMFa and IMFb establish the interrupt mode:
   - MODE 0 (IMFA=0, IMFB=0) is compatible with the CPU interrupt service procedures. The interrupting device places an instruction on the data bus, which is then acted upon by the CPU. This is normally a restart instruction, which will initiate an unconditional jump to the selected one of eight restart locations on page zero of memory.
   - MODE 1 (IMFa=1, IMFb=1) is similar to NMI operation. It has only vector address, 0038H.
   - MODE 2 (IMFa=1, IMFb=1) is used with Z80 peripherals. The interrupting peripheral places an eight bit address vector on the data bus during the interrupt acknowledgement cycle. The high order byte is supplied by the Index register.
2. The priority is determined by its physical location in a daisy chain configuration. Each device has an interrupt enable input IEI and an interrupt enable output IEO. IEO is tied to the next lower priority device. The first device in the chain has IEI tied to +5 volts and its IEO output tied to the IEI input of the next higher priority device. The interrupting device disables its IEO output until it has been serviced, and then brings the IEO high to allow lower order peripherals to be serviced.
3. The CPU will nest (queue) pending interrupts, or interrupts received while a selected device is being serviced. Two interrupt flip flops are set or reset to indicate the status.

INTERRUPT FLIP FLOP STATUS



Instruction Set

The Z80 CPU has 158 instructions, a summary of which follows. Details will be found in the Z80 CPU Technical Manual and Assembly Language Programming Manual.

1. Eight bit loads.
2. 16 bit loads.
3. Exchanges, block transfers, and searches.
4. Eight and sixteen bit arithmetic operations.
5. Eight bit logic operations.
6. General purpose arithmetic and CPU control.
7. Rotates and shifts.
8. Bit set, reset, and test operations.
9. Jumps.
10. Calls, returns, and restarts.
11. Input and output operations.

Addressing Modes

A variety of addressing modes are available, including immediate, immediate extend, modified page zero, relative, extended, indexed, register, register indirect, implied, and bit.

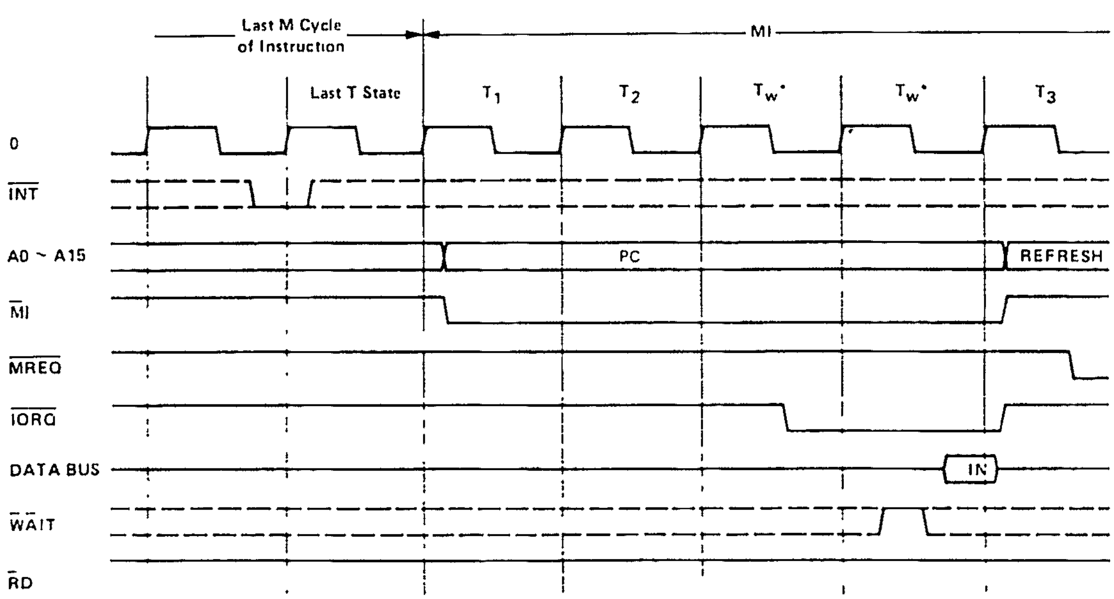
Pin descriptions

- **A0-A15:** Address bus is three state, active high. It provides a 16 bit (high byte, low byte) address for memory and input/output devices.
- **BUSACK(23):** Bus Acknowledge, active low output, indicates to the requesting device that the CPU address bus, data bus, and control signals MREQ, IORQ, RD, and WR are in a high Z state.
- **BUSREQ(25):** Bus Request, active low input, has a higher priority than NMI and is recognized at the end of the current machine cycle. The CPU data and address bus, and control signals MREQ,IORQ, RD, and WR go to high Z. Extended BUSREQ periods due to extended DMA operations can prevent the CPU from properly refreshing dynamic RAMs.
- **D0-D7:** The Data Bus is three state and bi-directional. It is used for data exchanges with memory and I/O.
- **HALT(18):** An active low output indicates that the CPU has executed a Halt instruction, and is waiting for an interrupt before operation can resume. The CPU executes NOPs to maintain memory refresh.
- **INT(16):** Interrupt Request, an active low input, is generated by I/O devices. The request is honored at the end of the current instruction if the internal software controlled flip flop IFF is enabled.

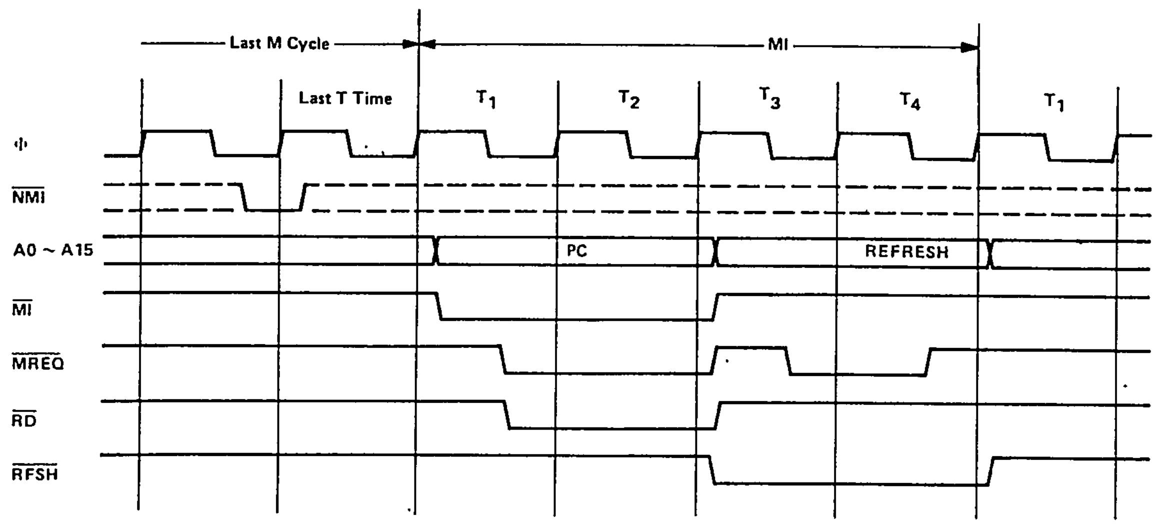
IORQ(20): Input/Output Request, three state, active low, indicates that the lower half of the address bus holds a valid I/O address for a read or write operation. IORQ occurs concurrent with M1 during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

- **M1(27):** Machine Cycle one, active low output, together with MREQ indicates that the current machine cycle is is the opcode fetch cycle of an instruction execution. M1 with IORQ indicates an interrupt acknowledge cycle.
- **MREQ(19):** Memory Request is an active low, three state output. It indicates that there is a valid address on the bus for memory read or write.
- **NMI(17):** Non-maskable Interrupt is an active low input that has a higher priority than INT. It is recognized at the end of the current instruction, and automatically forces the CPU to restart at location 0066H.
- **RD(21):** Memory Read, active low output, three state, indicates that the CPU wants to read data from memory or I/O.
- **RESET(26):** Reset is an active low input that initializes the CPU. It resets the interrupt flip flop, clears the program counter and the interrupt and memory and refresh registers, and sets the interrupt status to mode zero. Address and data bus go to high Z state. All control output signals are inactive. RESET must be active for at least three clock cycles.
- **RFSH(28):** Refresh, active low output, together with MREQ, indicates that the lower seven bits of the address bus can be used as a refresh address to dynamic memories.
- **WAIT(24):** Wait is an active low input. It indicates that the addressed memory or I/O are not ready for a data transfer. Extended WAIT periods can prevent the CPU from properly refreshing dynamic memory.
- **WR(22):** Memory Write is an active low three state output. It indicates that the CPU data bus has valid data to be stored at the addressed memory or I/O.

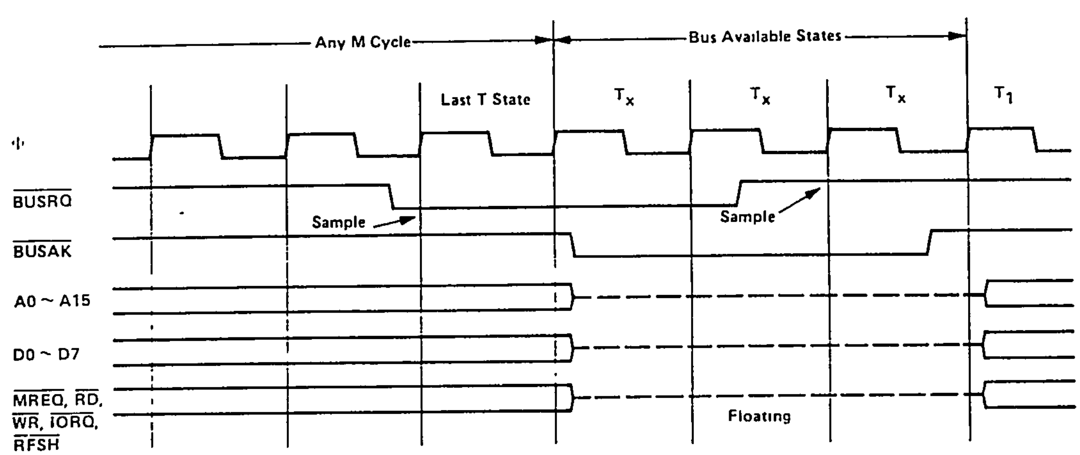
Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction. When the interrupt is accepted, a special M1 cycle is generated, with IORQ active to indicate that the interrupting device can put an eight bit vector on the data bus. The CPU automatically adds two WAIT states to this cycle.



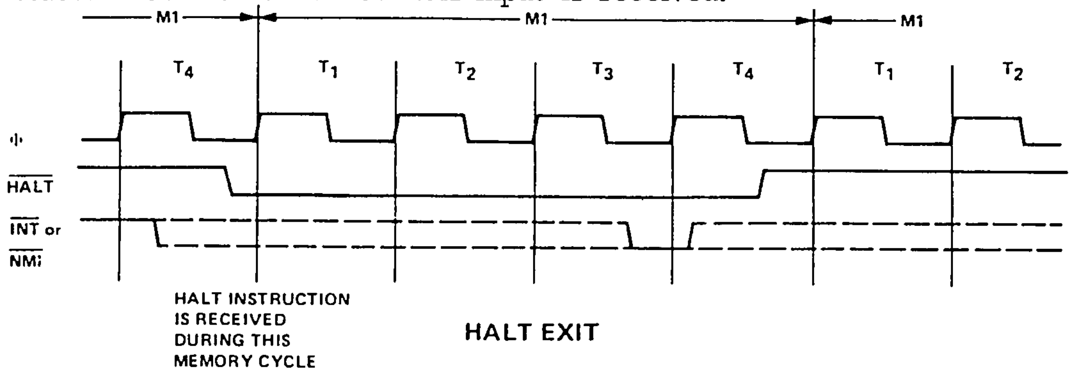
Non-Maskable Interrupt Request Cycle. NMI is sampled at the same time as INT, but has a higher priority and cannot be disabled by software. Timing is similar to normal memory read operation, but any data on the bus is ignored. The CPU executes a restart (RST) and jumps to the NMI service routine at address 0066H.



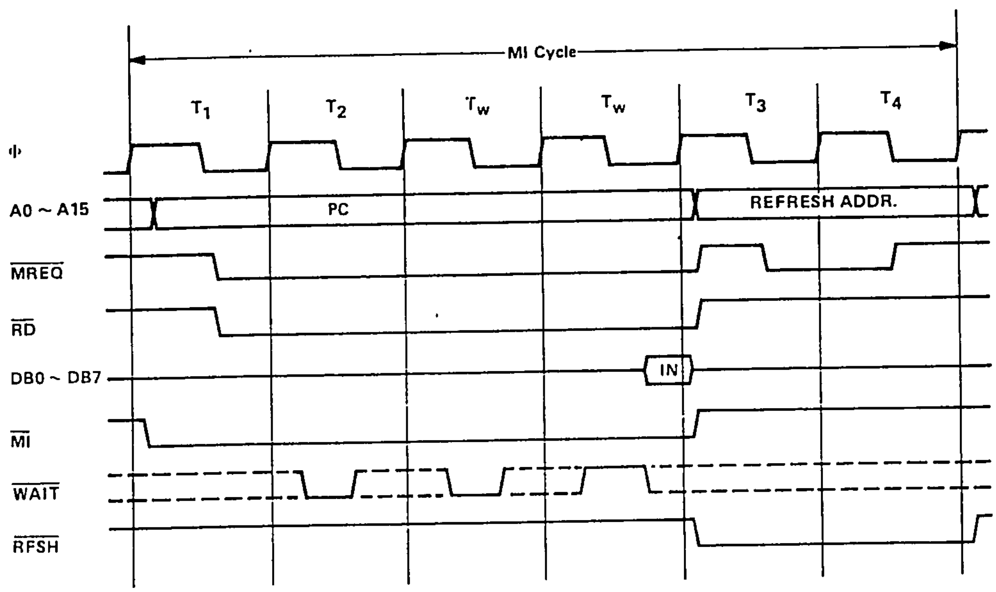
Bus Request/Acknowledge Cycle. The CPU samples BUSREQ with the rising edge of the last clock period of any machine cycle., With BUSREQ active, the CPU sets address, data, and MREQ, IORQ, RD, and WR lines to high Z state with the rising edge of the next clock pulse. Usually used to transfer data between memory and I/O.



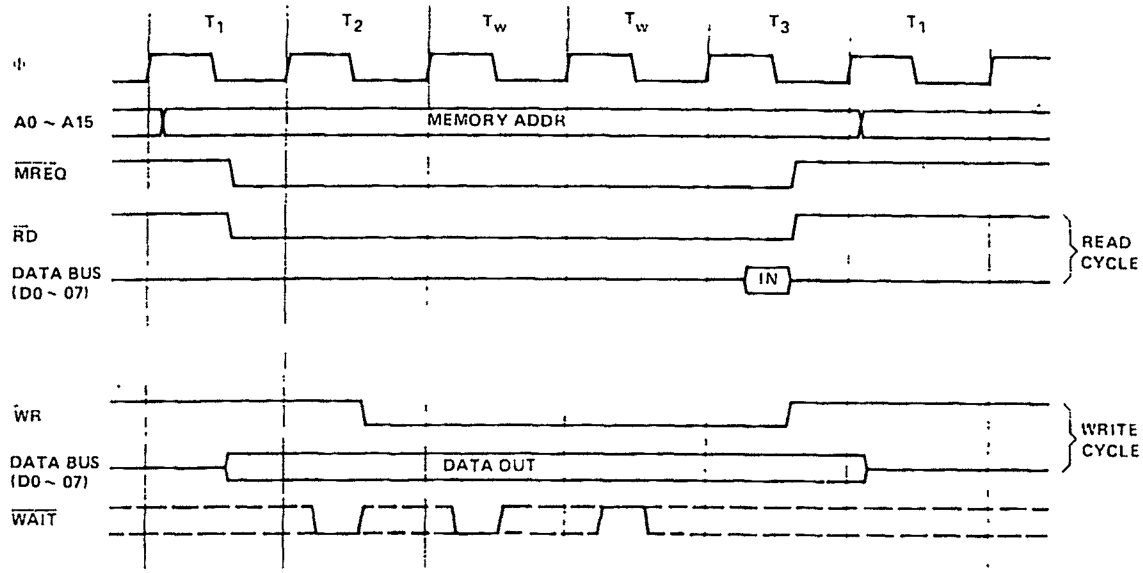
Halt Acknowledge Cycle. When the CPU receives a HALT instruction it executes NOP states until either INT or NMI input is received.



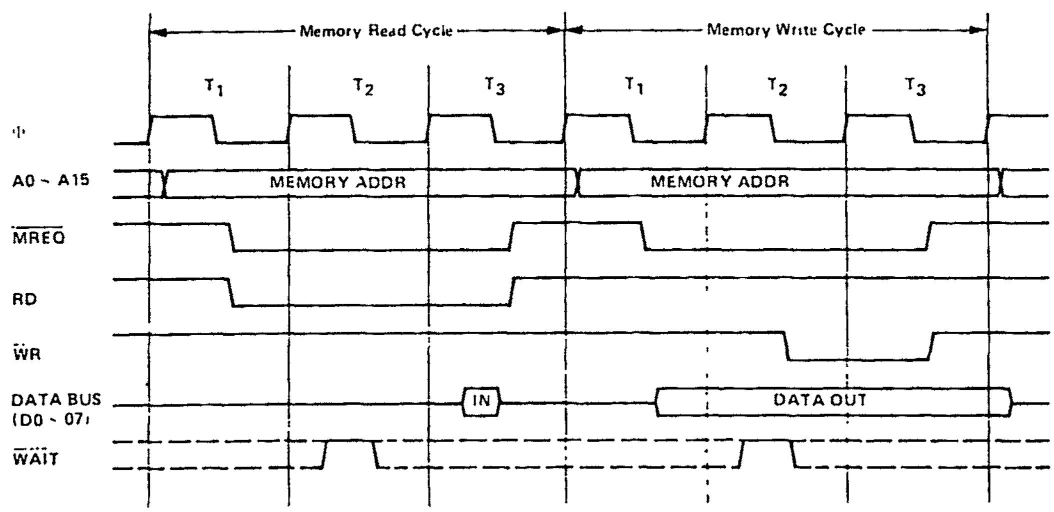
Instruction Op Code Fetch Timing: The CPU places the contents of the program counter on the address bus at the start of the cycle. Approximately one-half clock cycle later, MREQ goes active. The falling edge of MREQ can be used as a chip enable to dynamic memories. When active, RD indicates that memory data can be placed on the data bus. The CPU samples the WAIT input with the rising edge of clock state T3. During T3 and T4 of an M1 cycle, dynamic RAM refresh can occur.



Memory Read/Write Timing: (other than opcode fetch M1). The MREQ and RD signals function in the fetch cycle. In a memory write cycle, MREQ also becomes active when the address bus is stable, so that it can be used as a chip enable. The WR line is active when the data bus is stable, so that it can be used directly as an R/W pulse to most memories.

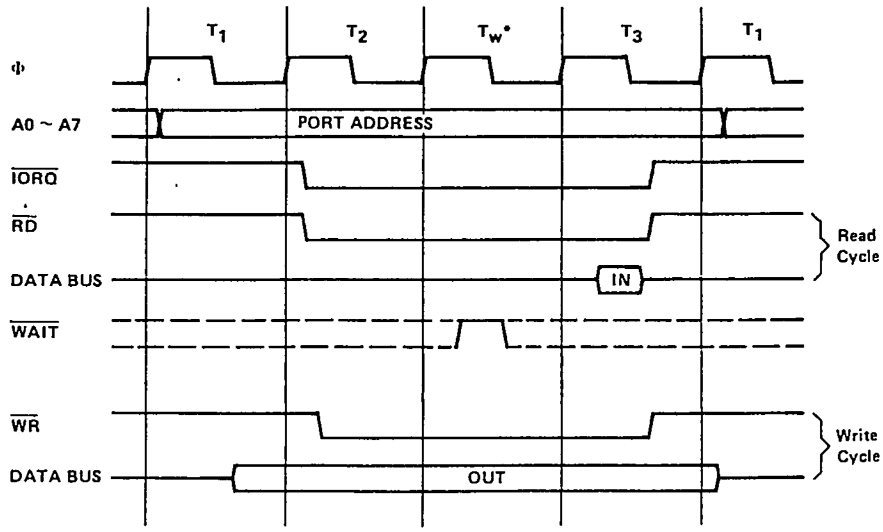


MEMORY READ OR WRITE CYCLES WITH WAIT STATES

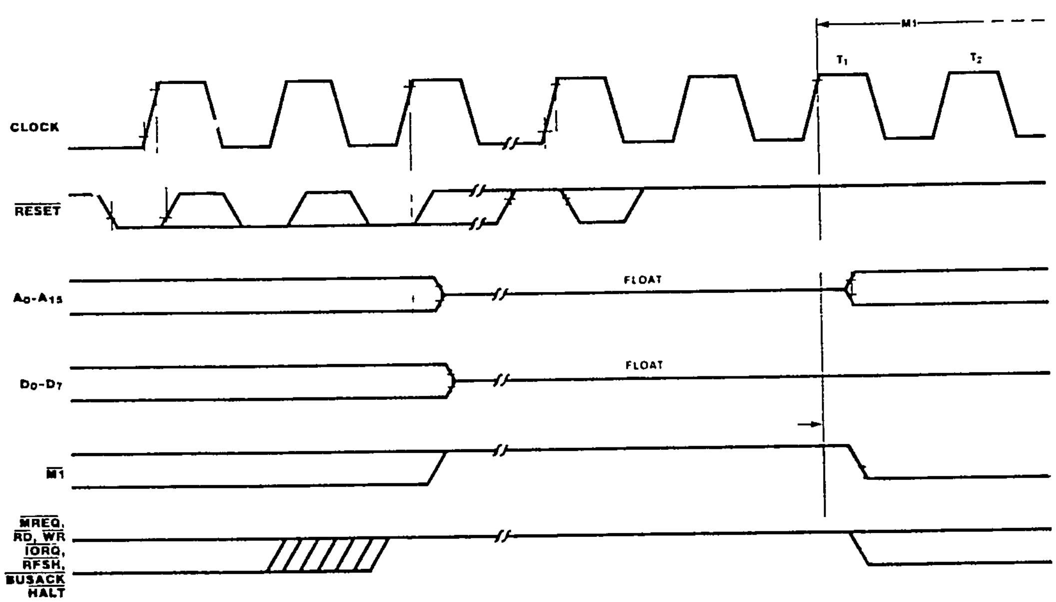


MEMORY READ OR WRITE CYCLES

Input Or Output Timing: During I/O operations, the CPU automatically inserts a single WAIT state (Tw) to allow sufficient time for an I/O port to decode the address and the port address lines.



Reset Cycle: RESET must be active for at least three clock cycles. As long as reset remains active, the address and data buses float, and control outputs are inactive. Once RESET goes inactive, two internal T cycles are used before the CPU starts normal processing. Since RESET clears the program counter, the first opcode fetch will be to location 0000.



Z8470 Z80 DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER

AMPEX P/N 000-012
VPR-80/VPR-3

The Z80 DART provides two independent full duplex channels for use as an asynchronous receiver/transmitter. There can be five to eight bits per word, with optional even or odd parity. The transmitter can supply one, one and a half or two stop bits per character and can provide a break output at any time. The receiver break detection logic interrupts the CPU at the start and the end of a received break.

Symmetrical transmit/receive clocks are not required. Data can be handled at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the clock inputs. If channel B is used, the bit rates for receive and transmit must be the same.

PIN DESCRIPTION

B/$\overline{A}$(34):	Channel A(low) or B(high), defines which channel is accessed during a data transfer between the CPU and the Z80 DART.
C/$\overline{D}$(33):	Control(high) or Data(low) specifies the type of information transferred on the data bus between the CPU and the DART.
$\overline{CE}$(35):	Chip enable, when low, allows the DART to accept commands or data from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.
CLK(20):	System clock input is the standard Z80 single phase system clock to synchronize internal signals.
$\overline{CTSA}$(18), $\overline{CTSB}$(23):	Clear to send when low, enables the respective (A or B) transmitter.
D0-D7:	System data bus (bidirectional, three state) transfers data and commands btween the CPU and the Z80 DART.
$\overline{DCDA}$(19), $\overline{DCDB}$(22):	Data carrier detect inputs, when low, function as receiver enables.
$\overline{DTRA}$(16), $\overline{DTRB}$(25):	Data terminal ready (outputs, active low) follow the state programmed into the DTR bit.
IEI(6):	Interrupt enable input, when high, is used with IEO to form a priority daisy chain when there is more than one interrupt driven device. A high on this input indicates that no other device with a higher priority is using the CPU interrupt.
IEO(7):	Interrupt enable output (output, active high) is high only if IEI is high and the CPU is not servicing an interrupt from this DART. The signal is used to block lower priority devices from interrupting while a higher priority device is being serviced by the CPU.
$\overline{INT}$(5):	Interrupt request (active low) indicates that the DART is requesting an interrupt.

M1(8): Machine cycle one is an active low input from the CPU. When M1 and RD are both low, the CPU is fetching an instruction from memory. If the Z80 Dart is the highest priority device that has interrupted the CPU, the DART accepts M1 and IORQ together active as an acknowledge.

IORQ(36): The active low input from the CPU Input/Output Request is used in conjunction with B/A, C/D, CE, and RD to transfer commands and data between the CPU and the Z80 DART.

1. When CE, RD, and IORQ are all active, the channel selected by B/A transfers data to the CPU .
2. When CE and IORQ are active, but RD is inactive, the channel selected by B/A is written to by the CPU with data or control information as specified by C/D.

RxCA(13); RxCB(27): Input Receive Clocks sample received data on the rising edge of the clock. The clocks may be 1, 16, 32, or 64 times the data rate.

RD(32): The read cycle status is an active low input from the CPU. When RD is active, a memory or I/O read operation is in progress.

RXDA(12); RXDB(28): Receive data, active high inputs.

RESET(21): The active low input RESET disables both receivers and transmitters, forces TXDA and TXDB marking, forces the modem controls high, and disables all interrupts.

RIA(11); RIB(29): Ring indicator (active low inputs), are similar to CTS and DCD. The DART detects both logic transitions and iterrupts the CPU. When not used in switched-line applications, these inputs can be used as general-purpose inputs.

RTSA(17); RTSB(24): When the request to send (active low output) bit is set, this output goes low. When the RTS bit is reset, the output goes high after the transmitter empties.

TxCA(14); TxCB(27): Transmitter clock inputs. (RxCB/TxCB is a common line RxTxCB). The transmitted data TxD changes on the falling edge of the clock. Clocks can be 1, 16,32, or 64 times the data rate; however the clock multiplier for the transmitter and receiver must be the same.

TxDA(15); TxDB(26): Transmit data, active high.

W/RDYA(10); W/RYDB(30):
Wait/Ready:

1. When programmed as WAIT lines that synchronize the CPU to the DART data rate they are open drain outputs.
2. When programmed as READY lines for a DMA controller, they are driven High and Low.
3. The reset state is open drain.

Z8430
Z80® CTC Counter/ Timer Circuit

Features

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.
- Selectable positive or negative trigger initiates timer operation.
- Standard Z-80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.
- Interfaces directly to the Z-80 CPU or—for baud rate generation—to the Z-80 SIO.

General Description

The Z-80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z-80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z-80 CPU and the Z-80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward:

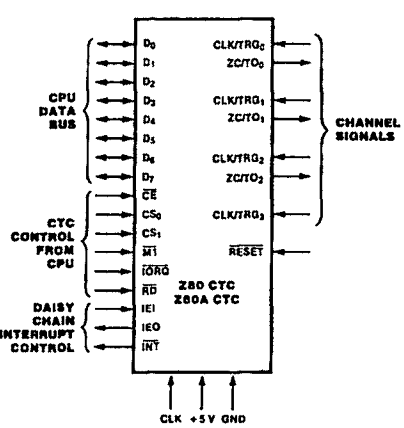


Figure 1. Pin Functions

2041-01

each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, reloads its time constant automatically, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

The Z-80 CTC requires a single +5 V power supply and the standard Z-80 single-phase system clock. It is fabricated with n-channel silicon-gate depletion-load technology, and packaged in a 28-pin plastic or ceramic DIP.

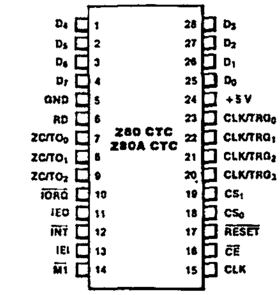


Figure 2. Pin Assignments

Functional Description

The Z-80 CTC has four independent counter/timer channels. Each channel is individually programmed with two words: a control word and a time-constant word. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets a prescaler, which divides the system clock by either 16 or 256. The time-constant word is a value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode operation the counter decrements on each of the CLK/TRG input pulses until zero count is reached. Each decrement is synchronized by the system clock. For counts greater than 256, more than one counter can be cascaded. At zero count, the down-counter is automatically reset with the time constant value.

The timer mode determines time intervals as small as 4 μs (Z-80A) or 6.4 μs (Z-80) without additional logic or software timing loops. Time intervals are generated by dividing the system clock with a prescaler that decrements a preset down-counter.

Thus, the time interval is an integral multiple of the clock period, the prescaler value (16 or 256) and the time constant that is preset in the down-counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

Three channels have two outputs that occur at zero count. The first output is a zero-count/timeout pulse at the ZC/TO output. The fourth channel (Channel 3) does not have a ZC/TO output; interrupt request is the only output available from Channel 3.

The second output is Interrupt Request (INT), which occurs if the channel has its interrupt enabled during programming. When the Z-80 CPU acknowledges Interrupt Request, the Z-80 CTC places an interrupt vector on the data bus.

The four channels of the Z-80 CTC are fully prioritized and fit into four contiguous slots in a standard Z-80 daisy-chain interrupt structure. Channel 0 is the highest priority and Channel 3 the lowest. Interrupts can be individually enabled (or disabled) for each of the four channels.

Architecture The CTC has four major elements, as shown in Figure 3.

- CPU bus I/O
- Channel control logic
- Interrupt logic
- Counter/timer circuits

CPU Bus I/O. The CPU bus I/O circuit decodes the address inputs, and interfaces the CPU data and control signals to the CTC for distribution on the internal bus.

Internal Control Logic. The CTC internal control logic controls overall chip operating functions such as the chip enable, reset, and read/write logic.

Interrupt Logic. The interrupt control logic ensures that the CTC interrupts interface properly with the Z-80 CPU interrupt system. The logic controls the interrupt priority of the CTC as a function of the IEI signal. If IEI is High, the CTC has priority. During interrupt

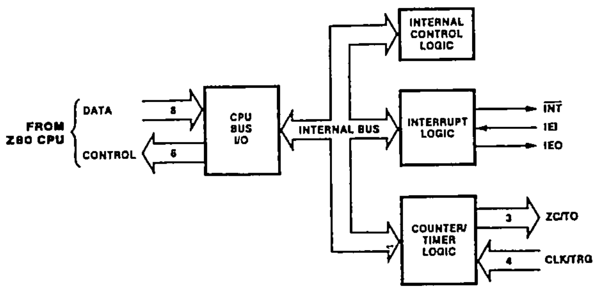


Figure 3. Functional Block Diagram

processing, the interrupt logic holds IEO Low, which inhibits the interrupt operation on lower priority devices. If the IEI input goes Low, priority is relinquished and the interrupt logic drives IEO Low.

If a channel is programmed to request an interrupt, the interrupt logic drives IEO Low at the zero count, and generates an $\overline{INT}$ signal to the Z-80 CPU. When the Z-80 CPU responds with interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$), then the interrupt logic arbitrates the CTC internal priorities, and the interrupt control logic places a unique interrupt vector on the data bus.

If an interrupt is pending, the interrupt logic holds IEO Low. When the Z-80 CPU issues a Return From Interrupt (RETI) instruction, each peripheral device decodes the first byte (ED_{16}). If the device has a pending interrupt, it raises IEO (High) for one $\overline{M1}$ cycle. This ensures that all lower priority devices can decode the entire RETI instruction and reset properly.

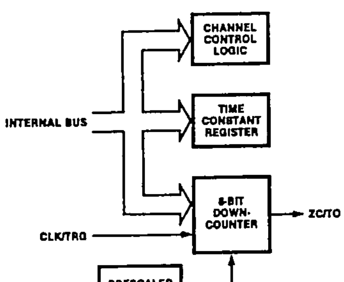


Figure 4. Counter/Timer Block Diagram

Counter/Timer Circuits. The CTC has four independent counter/timer circuits, each containing the logic shown in Figure 4.

Channel Control Logic. The channel control logic receives the 8-bit channel control word when the counter/timer channel is programmed. The channel control logic decodes the control word and sets the following operating conditions:

- Interrupt enable (or disable)
- Operating mode (timer or counter)
- Timer mode prescaler factor (16 or 256)
- Active slope for CLK/TRG input
- Timer mode trigger (automatic or CLK/TRG input)
- Time constant data word to follow
- Software reset

Time Constant Register. When the counter/timer channel is programmed, the time constant register receives and stores an 8-bit time constant value, which can be anywhere from 1 to 256 (0 = 256). This constant is automatically loaded into the down-counter when the counter/timer channel is initialized, and subsequently after each zero count.

Prescaler. The prescaler, which is used only in timer mode, divides the system clock frequency by a factor of either 16 or 256. The prescaler output clocks the down-counter during timer operation. The effect of the prescaler on the down-counter is a multiplication of the system clock period by 16 or 256. The prescaler factor is programmed by bit 5 of the channel control word.

Down-Counter. Prior to each count cycle, the down-counter is loaded with the time constant register contents. The counter is then decremented one of two ways, depending on operating mode:

- By the prescaler output (timer mode)
- By the trigger pulses into the CLK/TRG input (counter mode)

Without disturbing the down-count, the Z-80 CPU can read the count remaining at any time by performing an I/O read operation at the port address assigned to the CTC channel. When the down-counter reaches the zero count, the ZC/TO output generates a positive-going pulse. When the interrupt is enabled, zero count also triggers an interrupt request signal ($\overline{INT}$) from the interrupt logic.

Programming Each Z-80 CTC channel must be programmed prior to operation. Programming consists of writing two words to the I/O port that corresponds to the desired channel. The first word is a control word that selects the operating mode and other parameters; the second word is a time constant, which is a binary data word with a value from 1 to 256. A time constant word must be preceded by a channel control word.

After initialization, channels may be reprogrammed at any time. If updated control and time constant words are written to a channel during the count operation, the count continues to zero before the new time constant is loaded into the counter.

If the interrupt on any Z-80 CTC channel is enabled, the programming procedure should also include an interrupt vector. Only one vector is required for all four channels, because the interrupt logic automatically modifies the vector for the channel requesting service.

A control word is identified by a 1 in bit 0. A 1 in bit 2 indicates a time constant word is to follow. Interrupt vectors are always addressed

Addressing. During programming, channels are addressed with the channel select pins CS_1 and CS_2. A 2-bit binary code selects the appropriate channel as shown in the following table.

Channel	CS_1	CS_0
0	0	0
1	0	1
2	1	0
3	1	1

Reset. The CTC has both hardware and software resets. The hardware reset terminates all down-counts and disables all CTC interrupts by resetting the interrupt bits in the control registers. In addition, the ZC/TO and Interrupt outputs go inactive, IEO reflects IEI, and D_0-D_7 go to the high-impedance state. All channels must be completely reprogrammed after a hardware reset.

The software reset is controlled by bit 1 in the channel control word. When a channel receives a software reset, it stops counting. When a software reset is used, the other bits in the control word also change the contents of the channel control register. After a software reset a new time constant word must be written to the same channel.

If the channel control word has both bits D_1 and D_2 set to 1, the addressed channel stops operating, pending a new time constant word. The channel is ready to resume after the new constant is programmed. In timer mode, if $D_3 = 0$, operation is triggered automatically when the time constant word is loaded.

Channel Control Word Programming. The channel control word is shown in Figure 5. It sets the modes and parameters described below.

Interrupt Enable. D_7 enables the interrupt, so that an interrupt output ($\overline{INT}$) is generated at zero count. Interrupts may be programmed in either mode and may be enabled or disabled at any time.

Operating Mode. D_6 selects either timer or counter mode.

Prescaler Factor. (Timer Mode Only). D_5 selects factor—either 16 or 256.

Trigger Slope. D_4 selects the active edge or slope of the CLK/TRG input pulses. Note that reprogramming the CLK/TRG slope during operation is equivalent to issuing an active edge. If the trigger slope is changed by a control word update while a channel is pending operation in timer mode, the result is the same as a CLK/TRG pulse and the timer starts. Similarly, if the channel is in counter mode, the counter decrements.

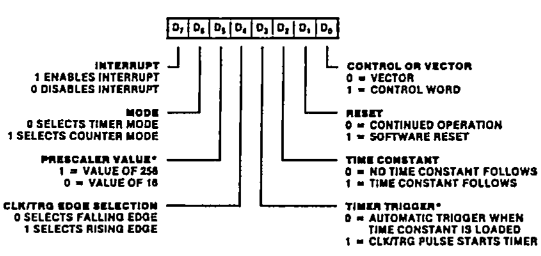


Figure 5. Channel Control Word

Trigger Mode (Timer Mode Only). D_3 selects the trigger mode for timer operation. When D_3 is reset to 0, the timer is triggered automatically. The time constant word is programmed during an I/O write operation, which takes one machine cycle. At the end of the write operation there is a setup delay of one clock period. The timer starts automatically (decrements) on the rising edge of the second clock pulse (T_2) of the machine cycle following the write operation. Once started, the timer runs continuously. At zero count the timer reloads automatically and continues counting without interruption or delay, until stopped by a reset.

When D_3 is set to 1, the timer is triggered externally through the CLK/TRG input. The time constant word is programmed during an I/O write operation, which takes one machine cycle. The timer is ready for operation on the rising edge of the second clock pulse (T_2) of the following machine cycle. Note that the first timer decrement follows the active edge of the CLK/TRG pulse by a delay time of one clock cycle if a minimum setup time to the rising edge of clock is met. If this minimum is not met, the delay is extended by another clock period. Consequently, for immediate triggering, the CLK/TRG input must precede T_2 by one clock cycle plus its minimum setup time. If the minimum time is not met, the timer will start on the third clock cycle (T_3).

Once started the timer operates continuously, without interruption or delay, until stopped by a reset.

Time Constant to Follow. A 1 in D_2 indicates that the next word addressed to the selected channel is a time constant data word for the time constant register. The time constant word may be written at any time.

A 0 in D_2 indicates no time constant word is to follow. This is ordinarily used when the channel is already in operation and the new channel control word is an update. A channel will not operate without a time constant value. The only way to write a time constant value is to write a control word with D_2 set.

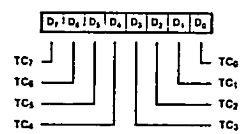


Figure 6. Time Constant Word

Software Reset. Setting D_1 to 1 causes a software reset, which is described in the Reset section.

Control Word. Setting D_0 to 1 identifies the word as a control word.

Time Constant Programming. Before a channel can start counting it must receive a time constant word from the CPU. During programming or reprogramming, a channel control word in which bit 2 is set must precede the time constant word to indicate that the next word is a time constant. The time constant word can be any value from 1 to 256 (Figure 6). Note that 00_{16} is interpreted as 256.

In timer mode, the time interval is controlled by three factors:

- The system clock period (ϕ)
- The prescaler factor (P), which multiplies the interval by either 16 r 256
- The time constant (T), which is programmed into the time constant register

Consequently, the time interval is the product of $\phi \times P \times T$. The minimum timer resolution is $16 \times \phi$ (4 μs with a 4 MHz clock). The maximum timer interval is $256 \times \phi \times 256$ (16.4 ms with a 4 MHz clock). For longer intervals timers may be cascaded.

Interrupt Vector Programming. If the Z-80 CTC has one or more interrupts enabled, it can supply interrupt vectors to the Z-80 CPU. To do so, the Z-80 CTC must be pre-programmed with the most-significant five bits of the interrupt vector. Programming consists of writing a vector word to the I/O port corresponding to the Z-80 CTC Channel 0. Note that D_0 of the vector word is always zero, to distinguish the vector from a channel control word. D_1 and D_2 are not used in programming the vector word. These bits are supplied by the interrupt logic to identify the channel requesting interrupt service with a unique interrupt vector (Figure 7). Channel 0 has the highest priority.

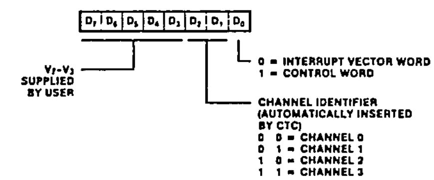


Figure 7. Interrupt Vector Word

Pin Description

$\overline{\textbf{CE}}$. *Chip Enable* (input, active Low). When enabled the CTC accepts control words, interrupt vectors, or time constant data words from the data bus during an I/O write cycle; or transmits the contents of the down-counter to the CPU during an I/O read cycle. In most applications this signal is decoded from the eight least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter-timer channels.

CLK. *System Clock* (input). Standard single-phase Z-80 system clock.

CLK/TRG$_0$-CLK/TRG$_3$. *External Clock/Timer Trigger* (input, user-selectable active High or Low). Four pins corresponding to the four Z-80 CTC channels. In counter mode, every active edge on this pin decrements the down-counter. In timer mode, an active edge starts the timer.

CS$_0$-CS$_1$. *Channel Select* (inputs active High). Two-bit binary address code selects one of the four CTC channels for an I/O write or read (usually connected to A_0 and A_1).

D$_0$-D$_7$. *System Data Bus* (bidirectional, 3-state). Transfers all data and commands between the Z-80 CPU and the Z-80 CTC.

IEI. *Interrupt Enable In* (input, active High). A High indicates that no other interrupting devices of higher priority in the daisy chain are being serviced by the Z-80 CPU.

IEO. *Interrupt Enable Out* (output, active High). High only if IEI is High and the Z-80 CPU is not servicing an interrupt from any Z-80 CTC channel. IEO blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced.

$\overline{\textbf{INT}}$. *Interrupt Request* (output, open drain, active Low). Low when any Z-80 CTC channel that has been programmed to enable interrupts has a zero-count condition in its down-counter.

$\overline{\textbf{IORQ}}$. *Input/Output Request* (input from CPU, active Low). Used with $\overline{CE}$ and $\overline{RD}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC. During a write cycle, $\overline{IORQ}$ and $\overline{CE}$ are active and $\overline{RD}$ inactive. The Z-80 CTC does not receive a specific write signal; rather, it internally generates its own from the inverse of an active $\overline{RD}$ signal. In a read cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ are active; the contents of the down-counter are read by the Z-80 CPU. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest priority interrupting channel places its interrupt vector on the Z-80 data bus.

$\overline{\textbf{M1}}$. *Machine Cycle One* (input from CPU, active Low). When $\overline{M1}$ and $\overline{IORQ}$ are active, the Z-80 CPU is acknowledging an interrupt. The Z-80 CTC then places an interrupt vector on the data bus if it has highest priority, and if a channel has requested an interrupt ($\overline{INT}$).

$\overline{\textbf{RD}}$. *Read Cycle Status* (input, active Low). Used in conjunction with $\overline{IORQ}$ and $\overline{CE}$ to transfer data and channel control words between the Z-80 CPU and the Z-80 CTC.

$\overline{\textbf{RESET}}$. *Reset* (input active Low). Terminates all down-counts and disables all interrupts by resetting the interrupt bits in all control registers; the ZC/TO and the Interrupt outputs go inactive; IEO reflects IEI; D_0-D_7 go to the high-impedance state.

ZC/TO$_0$-ZC/TO$_2$. *Zero Count/Timeout* (output, active High). Three ZC/TO pins corresponding to Z-80 CTC channels 2 through 0 (Channel 3 has no ZC/TO pin). In both counter and timer modes the output is an active High pulse when the down-counter decrements to zero.

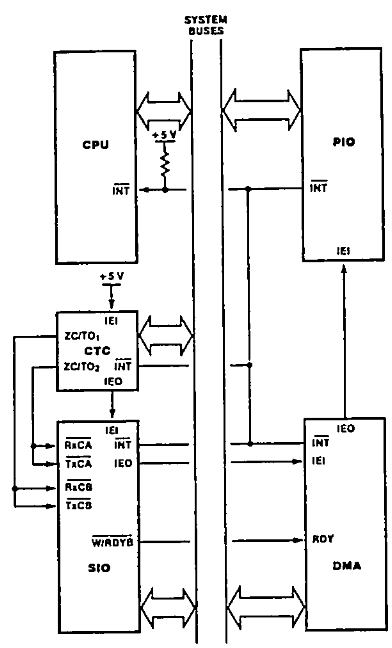


Figure 8. A Typical Z-80 Environment

Timing

Read Cycle Timing. Figure 9 shows read cycle timing. This cycle reads the contents of a down-counter without disturbing the count. During clock cycle T_2, the Z-80 CPU initiates a read cycle by driving the following inputs Low: $\overline{RD}$, $\overline{IORQ}$, and $\overline{CE}$. A 2-bit binary code at inputs CS_1 and CS_0 selects the channel to be read. $\overline{M1}$ must be High to distinguish this cycle from an interrupt acknowledge. No additional wait states are allowed.

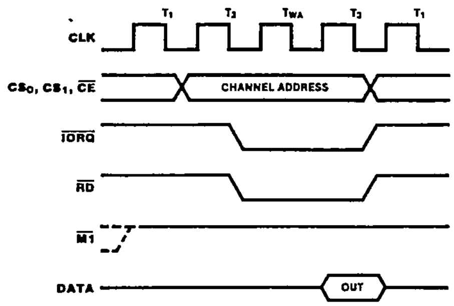


Figure 9. Read Cycle Timing

Write Cycle Timing. Figure 10 shows write cycle timing for loading control, time constant or vector words.

The CTC does not have a write signal input, so it generates one internally when the read ($\overline{RD}$) input is High during T_1. During T_2 $\overline{IORQ}$ and $\overline{CE}$ inputs are Low. $\overline{M1}$ must be High to distinguish a write cycle from an interrupt acknowledge. A 2-bit binary code at inputs CS_1 and CS_0 selects the channel to be addressed, and the word being written is placed on the Z-80 data bus. The data word is

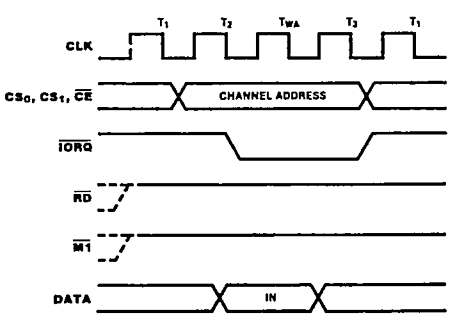


Figure 10. Write Cycle Timing

latched into the appropriate register with the rising edge of clock cycle T_3.

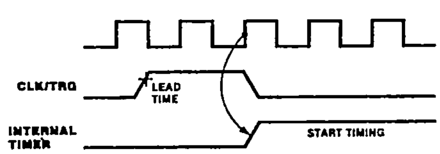


Figure 11. Timer Mode Timing

Timer Operation. In the timer mode, a CLK/TRG pulse input starts the timer (Figure 11) on the second succeeding rising edge of CLK. The trigger pulse is asynchronous, and it must have a minimum width. A minimum lead time (210 ns) is required between the active edge of the CLK/TRG and the next rising edge of CLK to enable the prescaler on the following clock edge. If the CLK/TRG edge occurs closer than this, the initiation of the timer function is delayed one clock cycle. This corresponds to the startup timing discussed in the programming section. The timer can also be started automatically if so programmed by the channel control word.

Z80 CTC

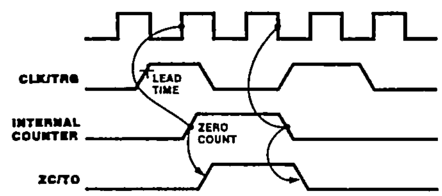


Figure 12. Counter Mode Timing

Counter Operation. In the counter mode, the CLK/TRG pulse input decrements the down-counter. The trigger is asynchronous, but the count is synchronized with CLK. For the decrement to occur on the next rising edge of CLK, the trigger edge must precede CLK by a minimum lead time as shown in Figure 12. If the lead time is less than specified, the count is delayed by one clock cycle. The trigger pulse must have a minimum width, and the trigger period must be at least twice the clock period.

The ZC/TO output occurs immediately after zero count, and follows the rising CLK edge.

Interrupt Operation

The Z-80 CTC follows the Z-80 system interrupt protocol for nested priority interrupts and return from interrupt, wherein the interrupt priority of a peripheral is determined by its location in a daisy chain. Two lines—IEI and IEO—in the CTC connect it to the system daisy chain. The device closest to the +5 V supply has the highest priority (Figure 13). For additional information on the Z-80 interrupt structure, refer to the *Z-80 CPU Product Specification* and the *Z-80 CPU Technical Manual.*

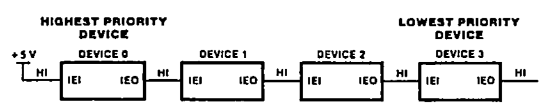
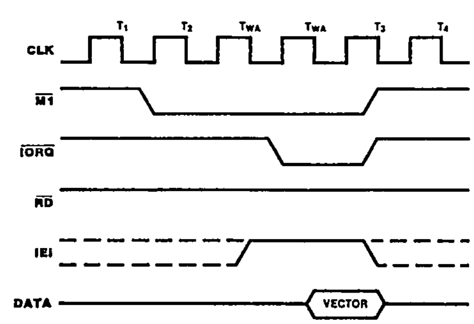


Figure 13. Daisy-Chain Interrupt Priorities

Within the Z-80 CTC, interrupt priority is predetermined by channel number: Channel 0 has the highest priority, and Channel 3 the lowest. If a device or channel is being serviced with an interrupt routine, it cannot be interrupted by a device or channel with lower priority until service is complete. Higher priority devices or channels may interrupt the servicing of lower priority devices or channels.

A Z-80 CTC channel may be programmed to request an interrupt every time its down-counter reaches zero. Note that the CPU must be programmed for interrupt mode 2. Some time after the interrupt request, the CPU sends an interrupt acknowledge. The CTC interrupt control logic determines the highest priority channel that is requesting an interrupt. Then, if the CTC IEI input is High (indicating that it has priority within the system daisy chain) it places an 8-bit interrupt vector on the system data bus. The high-order five bits of this vector



ming process; the next two bits are provided by the CTC interrupt control logic as a binary code that identifies the highest priority channel requesting an interrupt; the low-order bit is always zero.

Interrupt Acknowledge Timing. Figure 14 shows interrupt acknowledge timing. After an interrupt request, the Z-80 CPU sends an interrupt acknowledge ($\overline{M1}$ and $\overline{IORQ}$). All channels are inhibited from changing their interrupt request status when $\overline{M1}$ is active—about two clock cycles earlier than $\overline{IORQ}$. $\overline{RD}$ is High to distinguish this cycle from an instruction fetch.

The CTC interrupt logic determines the highest priority channel requesting an interrupt. If the CTC interrupt enable input (IEI) is High, the highest priority interrupting channel within the CTC places its interrupt vector on the data bus when $\overline{IORQ}$ goes Low. Two wait states (T_{WA}) are automatically inserted at this time to allow the daisy chain to stabilize. Additional wait states may be added.

Return from Interrupt Timing. At the end of an interrupt service routine the RETI (Return From Interrupt) instruction initializes the daisy chain enable lines for proper control of nested priority interrupt handling. The CTC decodes the 2-byte RETI code internally and determines whether it is intended for a channel being serviced. Figure 15 shows RETI timing.

If several Z-80 peripherals are in the daisy chain, IEI settles active (High) on the chip currently being serviced when the opcode ED_{16} is decoded. If the following opcode is $4D_{16}$, the peripheral being serviced is released and its IEO becomes active. Additional wait states are allowed.

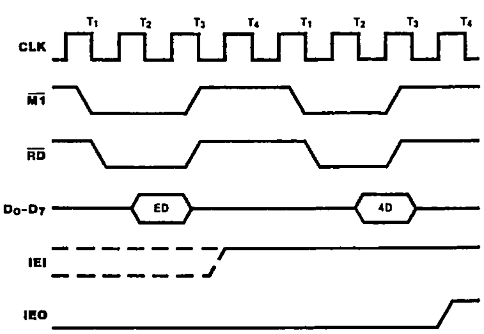


Figure 15. Return From Interrupt Timing

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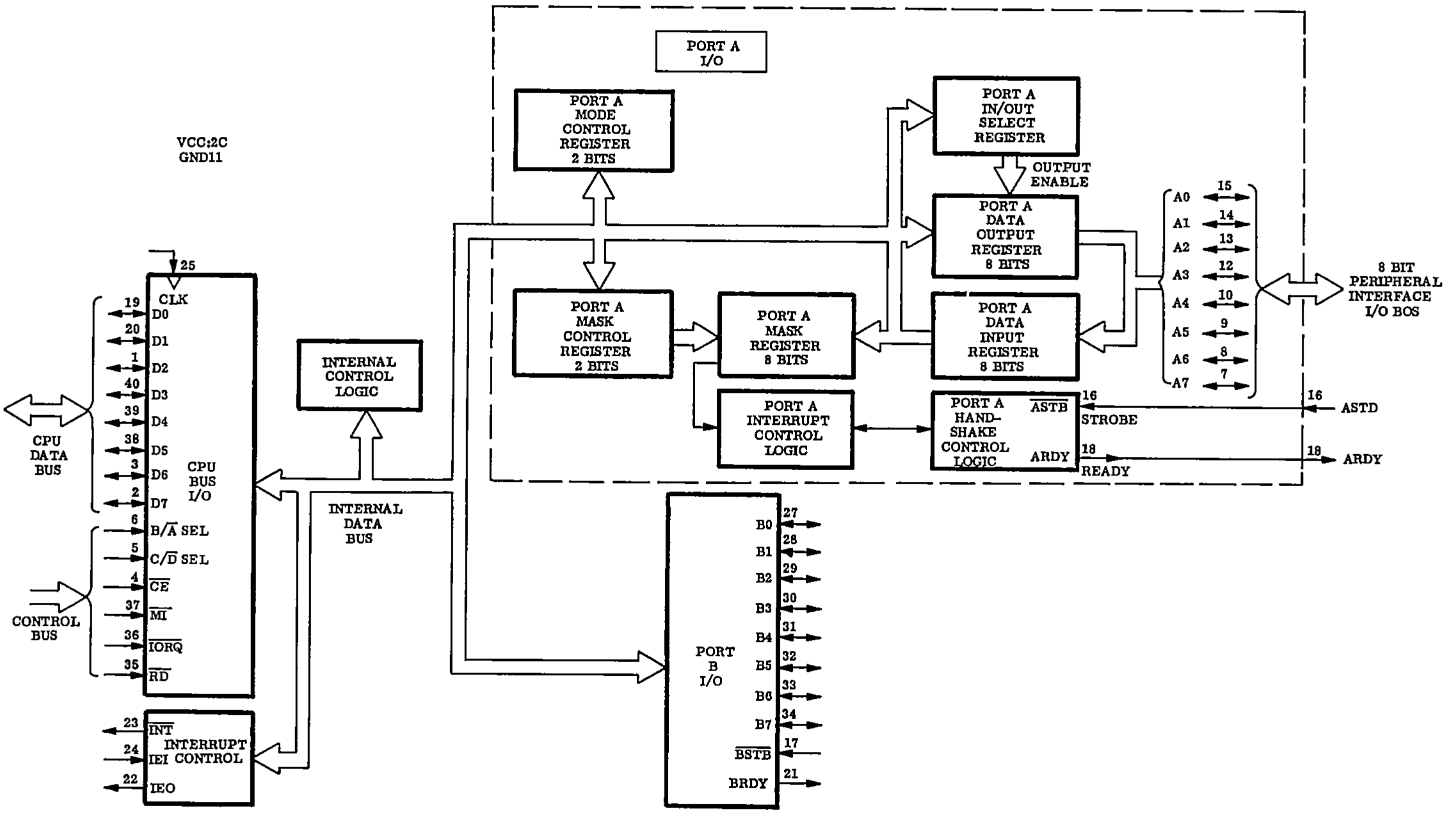
Z80 PIO PARALLEL INPUT/OUTPUT CONTROLLER (VPR-3)



1. The Z80 PIO parallel I/O Circuit is a programmable, dual port device that provides a TTL compatible interface between peripheral devices and the Z80 CPU. All data transfer between the peripheral device and the CPU is done with interrupt control. The PIO can interrupt the CPU upon the occurence of specified status conditions in the peripheral device. It interfaces to peripherals via two independent general purpose I/O ports A and B. Each port has eight data bits and two handshake signals. The READY output indicates to the peripheral that the port is ready for a data transfer, and the strobe is an input from the peripheral when a data transfer has occurred.

2. The ports can be programmed to operate in four modes.

   a. In Mode 0, either Port A or Port B can be programmed to output data. Both ports have output registers that are individually addressed by the CPU; data can be written to either port at any time. An active READY output indicates that the data is available. After the data transfer, the external device responds with an active STROBE input, which can generate an interrupt.

   b. In Mode 1, either Port A or Port B can be configured in the input mode. Each port has an input register addressed by the CPU. When the CPU reads data from a port, the PIO sets the READY signal. The external device can then place data on the I/O lines and STROBE the PIO, latching the data into the port input register, resets READY, and triggers the Interrupt Request, if enabled. The CPU can ready the data at any time, which again sets READY.

   c. Mode 2 is bidirectional and uses Port A, plus the interrupt and handshake signals from both ports. Port B is set to Mode 3 and masked off. Output operation is similar to Mode 0, except that data is allowed out onto the Port A bus only when ASTB is low. For input operation, similar to Mode 1, uses the Port B hand shake and interrupt signals.

   d. Both ports can be used in Mode 3. The individual bits are defined as either inputs or' outputs, defining up to eight separate, individually defined bits for each port. READY and STROBE are not used. Interrupt conditions are defined during the programming operation. The active level is specified as either a high, or a low, and the logic condition is specified as either OR (one or more inputs active) or AND (all conditions active).

3. Each port contains input and output registers, handshake control logic and control registers. all data transfers between the peripheral and the CPU use the data input and output registers. The handshake logic controls data transfers. The two bit mode control register selects one of the four moded.

   In Mode 3 the Input/output control register specifies which of the eight data bits in the port are to be outputs and enables these bits. The remaining bits are inputs. The mask register specifies which of the bits in the port are active and which are masked and inactive. The mask control register specifies the two conditions; first, whether the active state of the input bits is High or Low, and second, whether an interrupt is generated for the OR condition or the AND condition.

4. The Interrupt Control Logic section handles CPU interrupt protcal for nested priority interrupt structures. Any devices's physical location in a daisy chain configuration determines its priority. Within the PIO Port A interrupts have a higher priority than those of Port B. In the byte modes (0, 1, 2) and interrupt can be generated whenever the peripheral requires a data transfer. In bit control Mode 3, an interrupt can be generated when the peripheral status matches a programmed value.

   If the CPU (in interrupt Mode 2) accepts the interrupt, the interrupting devide must provide an eight bit interrupt vector for the CPU. This vector forms a pointer to a location in memory where the service routine is located. Each port has an independent interrupt vector Interrupts are enabled by the PIO when CPU $\overline{M1}$ goes low.

5. The Internal Control Logic receives control words for each port during programming and controls the operating functions. It synchronizes port operation, controls the port mode, port addressing, selects read/write function, and issues appropriate commands. The $\overline{RD}$, $\overline{CE}$, C/$\overline{D}$ and $\overline{IORQ}$ signals generate the write input internally.

6. Programming:

   a. Programming a port for Mode 0, 1 or 2 requires two words per port.

      (1) A mode control word selects the port operating mode, and may be written at any time.

D7	D6	D5	D4	1	1	1	1

- D3–D0 (1 1 1 1): Identifies mode control word
- D5, D4: Don't care
- D7, D6: Mode select:
  - 0 0 Mode 0
  - 0 1 Mode 1
  - 1 0 Mode 2
  - 1 1 Mode 3

      (2) An interrupt vector

D7	D6	D5	D4	D3	D2	D1	0

- D0 (0): Identifies interrupt vector
- D7–D1: User supplied interrupt vector

   b. Programming a port for Mode 3 operation requires a control word, a vector (if interrupts are enabled) and three additional words.

      (1) When Mode 3 is selected, the mode control word must be follwed by a control word that sets the I/O control register to define which port lines are inputs and which are outputs.

D7	D6	D5	D4	D3	D2	D1	D0

- D7–D0: 0 sets bit to output; 1 sets bit to input

      (2) Handshake is not used. Interrupts are generated as a logic function of the input signal levels. The interrupt control word defines the function (AND, OR) and active levels.

D7	D6	D5	D4	0	1	1	1

- D3–D0 (0 1 1 1): Identifies interrupt control word
- D4: 0=No mask word follows; 1=Mask word follows
- D5: 0=Active level is low; 1=Active level is High
- D6: 0=Interrupt on, OR function; 1=Interrupt on, AND function
- D7: 0=Interrupt disabled; 1=Interrupt enabled

(3) The Mask Control Word sets the mask control register, allowing any unused bits to be to be masked off. If any bits are to be masked, then D4 (para (2)) must be set.

D7	D6	D5	D4	D3	D2	D1	D0

D7–D0: MB_0-MB_7 mask bits. A bit is monitored for an interrupt if it is defined as an input and the mask bit is set to zero.

c. The Interrupt Disable control word can be used to enable or diable or enable a port interrupt. It can be used without changing the rest of the interrupt control word.

D7	D6	D5	D4	0	0	1	1

- D3–D0: Identifies interrupt disable word
- D6–D4: Dont care
- D7: D7=0 interrupt disable
  D7=1 interrupt enable.

7. Pin description:

a. A_0-A_7: PORT A BUS (bidirectional, 3-state). Transfers data, status, or control information between Port A and the peripheral device. A_0 is LSB.

b. ARDY: REGISTER A READY (output, active high) depends on the mode of Port A

(1) In OUTPUT mode the signal goes active to indicate that the Port A output register has been loaded, and the peripheral data bus is stable .

(2) In INPUT mode the signal is active when the Port A register is empty and ready to accept data from the peripheral device.

(3) In BIDIRECTIONAL MODE the signal is active when data is available in the Port A register for transfer to the peripheral device. In this mode, data is not placed on the Port A data bus unless $\overline{\text{ASTB}}$ is active. Also see BRDY.

(4) In control (bit) mode the signal is held in a low state (disabled).

c. $\overline{\text{ASTB}}$: PORT A STROBE PULSE FROM PERIPHERAL DEVICE (input, active low) depends on mode for

(1) In OUTPUT mode, the positive edge of the strobe is issued by the peripheral to acknowledge the receipt of data.

(2) In INPUT mode the strobe is issued by the peripheral to load data into the Port A input register.

(3) In BIDIRECTIONAL mode, when this signal is active data from the Port A output register is gated on to the Port A bi-directional bus. The positive edge of the strobe acknowledges the receipt of the data. See $\overline{\text{BSTB}}$

(4) In CONTROL mode the strobe is inhibited internally.

d. B_0-B_7: PORT B BUS (bidirectional, 3-state) transfers data, status, or control information between port B and a peripheral device. B_0 is the LSB. The port B data bus can supply 1.5 mA at 1.5 V to drive Darlington transistors.

e. B/$\overline{\text{A}}$: PORT B OR A SELECT(Input High=B) defines which port is accessed during a data transfer

f. BRDY: REGISTER B READY (output, active High) is similar to ARDY, except that in the PORT A BIDIRECTIONAL mode rthis signal is High when the Port A input register is empty and ready to accept data from the peripheral device.

g. $\overline{\text{BSTB}}$: PORT B STROBE PULSE FROM PERIPHERAL DEVICE (input, active low) is similar to $\overline{\text{ASTB}}$, except that when Port A is in the bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

h. C/$\overline{\text{D}}$: CONTROL OR DATA SELECT (input, High = C)defines the type of data transfer to be performed between the CPU and the PIO. A High during a CPU write to the PIO causes the data bus to be interpreted as a command for the port selected by the B/$\overline{\text{A}}$ line. A Low means that data is being transferred between the CPU and the PIO.

i. $\overline{CE}$: CHIP ENABLE (input, active Low) enables the PIO tomaccept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle.

j. CLK: SYSTEM CLOCK (input). Uses standard single phase Z80 system clock.

k. D_0-D_7: Z80 CPU DATA BUS (bidirectional, 3-state) transfers data and commands between the PIO and the CPU.

l. IEI: INTERRUPT ENABLE IN (input, active high) is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high indicates that no other devicesaof higher priority are being serviced.

m. IEO: INTERRUPT ENABLE OUT (output, active high) is the second signal required to form a daisy chain priority scheme. The IEO output would be connected to the IEI input of the next lower priority device. It is high only if IEI is high and the CPU is not servicing an interrupt from this PIO.

n. $\overline{INT}$: INTERRUPT REQUEST (output, open drain, active low) is active when the PIO is requesting interrupt service from the CPU.

o. $\overline{IORQ}$: INPUT/OUTPUT REQUEST (input from CPU, active low) is used in conjunction wihh B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the CPU and the PIO.

(1) When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are active, the port addressed by B/$\overline{A}$ transfers data to the CPU (read).

(2) When $\overline{CE}$ and $\overline{IORQ}$ are active, but $\overline{RD}$, is not, the port addressed by B/$\overline{A}$ is written into from the CPU with either data or control information, as specified by C/$\overline{D}$.

(3) Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt. The interrupting port automatically places its interrupt vector on the CPU data bus if it is the highest priority device.

p. $\overline{M1}$: MACHINE CYCLE (input from CPU, active low) is used as a sync pulse to control internal PIO operations

(1) When both $\overline{M1}$ and $\overline{RD}$ are active the Z80 CPU is fetching an instruction from memory.

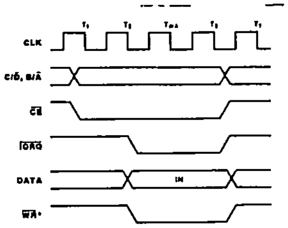
(2) When $\overline{M1}$ and $\overline{IORQ}$ are both active, the CPU is acknowledging an interrupt.

(3) When $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ the PIO is reset.

q. $\overline{RD}$: READ CYCLE STATUS (input from CPU, active low) if active, or an I/O operation is in progress, $\overline{RD}$ is used with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{IORQ}$ to transfer data from the PIO to the CPU.

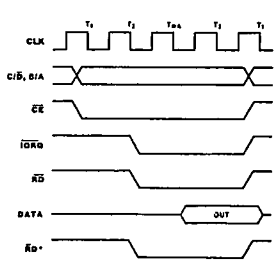
8. TIMING

a. WRITE CYCLE: No wait states are allowed for writing to the PIO other than the automatically inserted T_{WA}. The PIO internally generates its own write signal from the lack of an active $\overline{RD}$.



$^*\overline{WR} = RD \cdot \overline{CE} \cdot \overline{C/D} \cdot \overline{IORQ}$

b. READ CYCLE: Timing for reading the data input from an external device to one of the PIO ports.



$^*\overline{RD} = \overline{RD} \cdot \overline{CE} \cdot \overline{C D} \cdot \overline{IORQ}$

VPR-3 TRANSPORT

The VPR-3 tape transport is unique in that it does not utilize a pinch roller. All tape movement is controlled by a vacuum capstan in all modes. Air and roller guides reduce the effects of friction, permitting very rapid changes in tape speed and direction regardless of reel size.

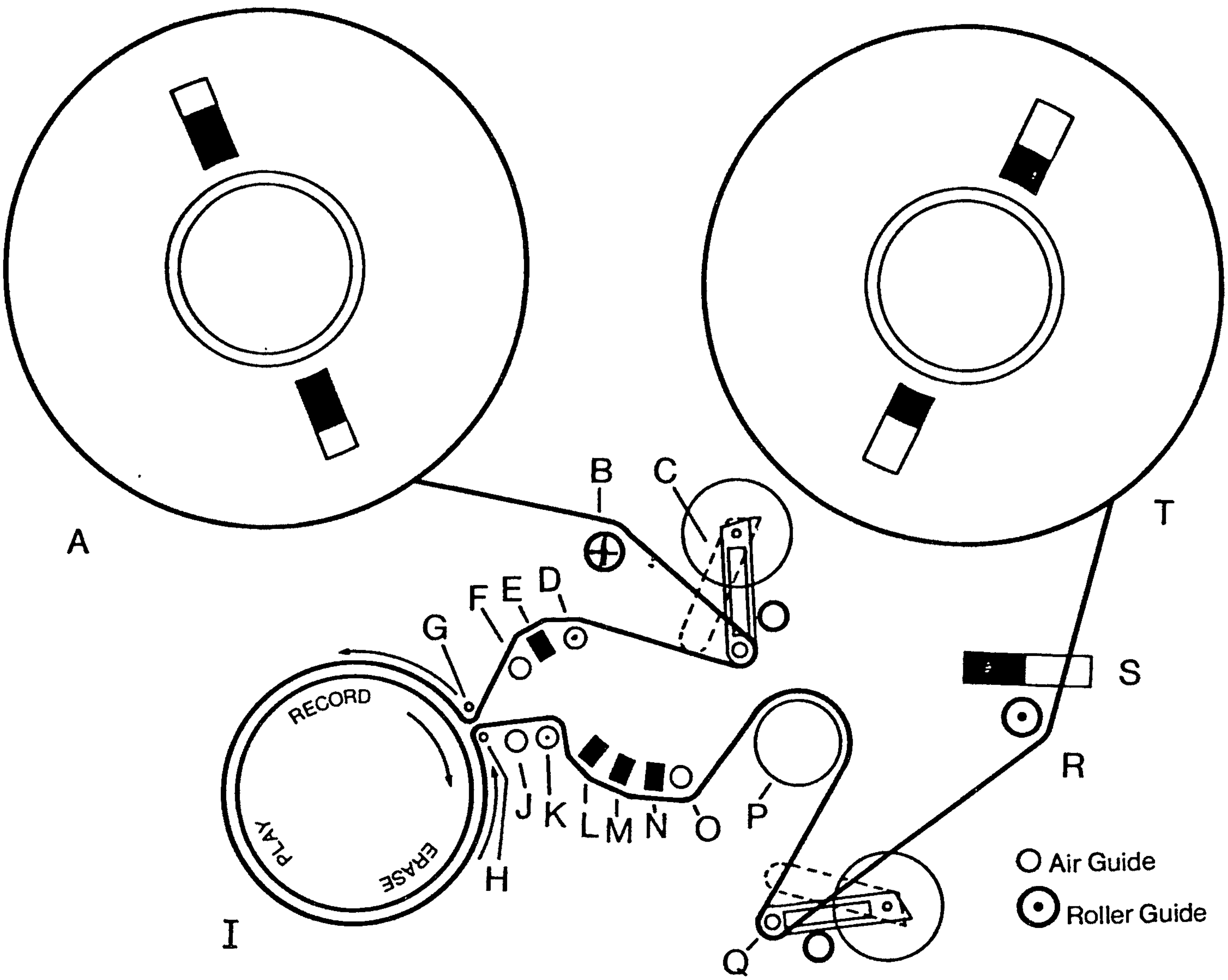
Air supplied by the VPR-3's internal air compressor is forced out of small holes in the air guides, forming a thin film that cushions the tape from the surface of the guide. The same compressor provides the capstan vacuum.

Heavy duty motors drive the supply and take up reels. The VPR-3 is virtually insensitive to differences in reel size and loading. It can handle 3 minute spot reels and 3 hour program reels with equal smoothness.

The VPR-3 utilizes the proven AST (Automatic Scan Tracking) head for playback, which allows playback of broadcast quality pictures through a continuously variable playback speed range of -1x to +3x normal play speed.

The following procedures are covered:

- Tape Path
- Cleaning the transport
- Loading Tape
- The Display Menu
- Tape Timer Set-up
- Standard Play Set-up
- Record Set-up
- Animation Editing
- Search to Cue
- Learn Sequence Mode
- Control Track Re-write


A
B
C
D
E
F
G
RECORD
PLAY
ERASE
H
I
J
K
L
M
N
O
P
Q
R
S
T
Air Guide
Roller Guide

Tape from the Supply reel (A) first passes over a guide (B) which provides initial tape guiding. The tape then contacts an air guide tension assembly (C) which senses tape tension and uses this information to control the supply reel.

The tape then travels over an edge guiding roller guide (D), and then passes the first of two longitudinal head assemblies (E). This assembly contains the full track video and sync erase heads. It also contains a sensor which detects whether or not there is tape loaded onto the tape transport. The tape then passes an air guide (F).

The scanner entrance guide (G) and exit guide (H) are air guides that provide proper tape positioning of the tape at the entrance to and exit from the scanner. When wrapped around the scanner the tape rests on a guide band on the lower, stationary half of the scanner. It is important that this guide band be free of dust and dirt; the tape must ride flush to the guide or tracking problems will arise.

In addition to the entrance and exit guides, the scanner assembly contains three active video heads (erase, record and play) spaced 120° apart and the optional sync heads which lead the video heads by 30° (I).

After leaving the scanner, the tape passes over another air guide (J) and then the flutter idler (K). The flutter idler isolates video head tip disturbances from the audio head stack.

The lower longitudinal head subassembly contains three stacks for audio 1, 2, 3 and control track. The first stack (L) contains the erase heads, the second stack (M) contains the record/play heads, and the third stack (N) provides for confidence playback in record. The head stacks are shielded from interference by a head cover which automatically is raised when tape is tensioned in the transport and retracts when tape is relaxed for ease of tape threading.

After moving across the audio head stack, the tape passes another air guide (O) and on to the capstan (P). The tape is held against the capstan with vacuum. The vacuum capstan controls tape speed and direction in all modes of operation.

Tape leaving the capstan then travels over a second air guide tension arm assembly (Q) which senses tape tension and uses this information to control the take-up reel. The tape then passes over a roller guide (R) which properly positions the tape to the take-up reel (T).

The combination guide/motor switch assembly (S) is designed for tapes that have been taken off a machine with a B-wind on the take-up reel, tails out and require rewinding (VPR-2, VPR-20). To change the direction of rotation of the take-up reel. The assembly is unplugged, rotated 180° and reinstalled. The take-up reel will now rotate clockwise in forward, giving a B-wind.

CLEANING THE TAPE PATH

The heads on the VPR-3 are made of ferrite material which makes them far more delicate than heads found on quad machines.

Additionally the VPR-3 does not use a pinch roller in the tape path; it is replaced by air guides and a vacuum capstan. As a result a specific cleaning procedure has been developed for this VTR in an effort to prevent damage to the machine.

First, unthread any tape that is still on the machine. Locate the entrance and exit air guides at the top of the scanner assembly. Dip a cotton swab in Ampex Head Cleaner (Ampex Part No. 087-007) and clean these guides, with air flowing. To obtain air flow lift one of the tension arm assemblies off the stop.

Run a cotton swab moistened with head cleaner around the edge of the band that is on the lower stationary drum. This is the edge that guides the tape around the scanner. If dirt builds up on this it will cause tracking problems.

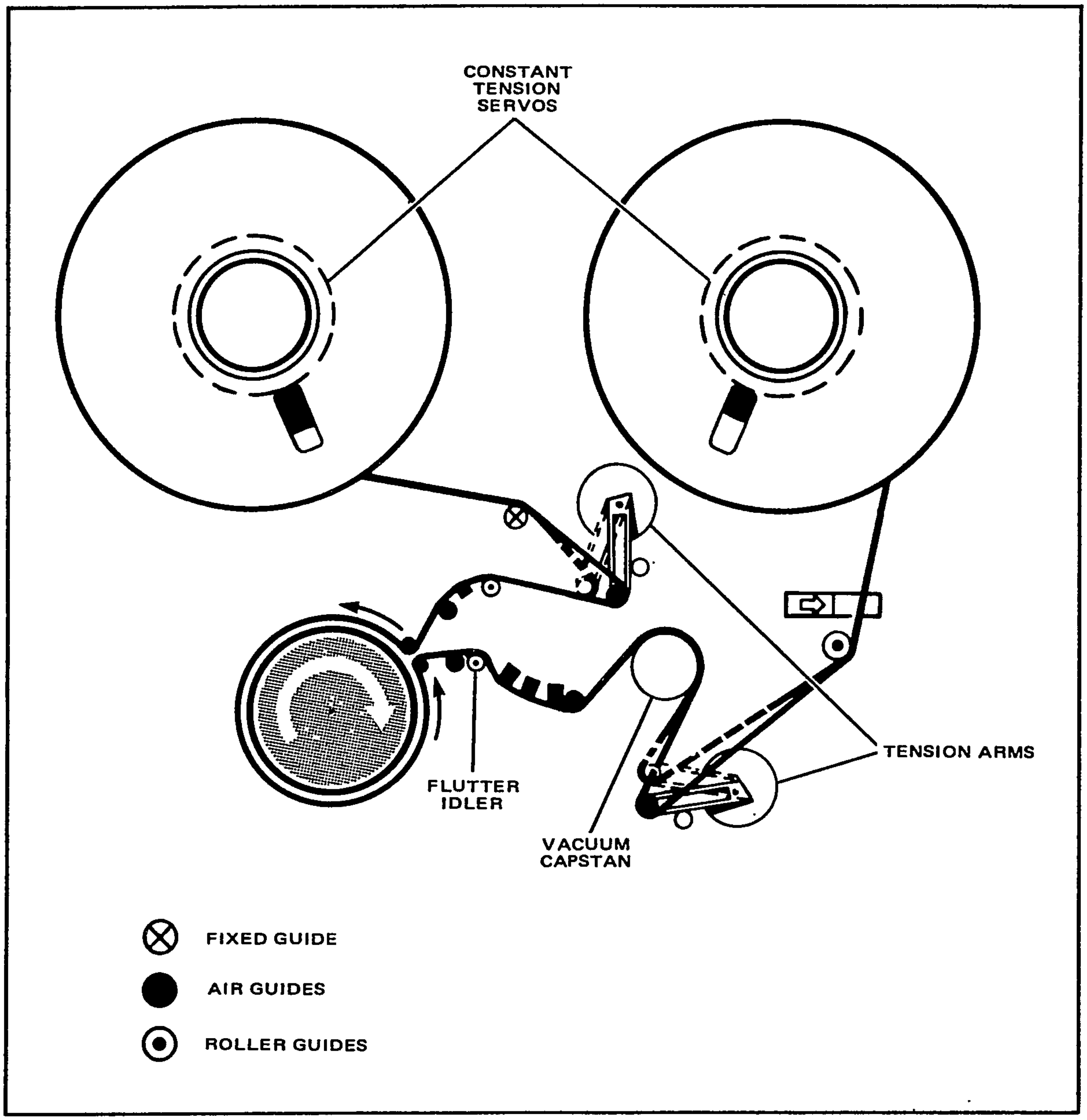
Locate the junction of the upper (moveable) and lower (stationary) halves of the scanner assembly. Position a Kim-wipe moistened with head cleaner on this surface and apply light pressure. Keeping the Kim-wipe in position with one hand rotate the scanner slowly clockwise two or three complete revolutions. DO NOT MOVE THE KIM-WIPE; ANY IN AND OUT MOVEMENT MAY DAMAGE A HEAD.

With a fresh Kim-wipe moistened lightly with head cleaner, clean the video erase head, audio and control track heads and tape guides. When the tape guides are cleaned ensure that air is flowing.

If the capstan requires cleaning, use a lint free linen rag moistened lightly with head cleaner. Allow the capstan dry completely before running the machine, or the cleaning fluid will be sucked into the VPR-3's air system.

After cleaning ensure that the transport is completely dry before loading tape. Any head cleaner still on the transport will dissolve the oxide binder on the tape and cause clogging of heads and air guides.

Care should be taken not to drip any cleaning fluid onto the trim or control panel.



Tape Thread Path

LOADING TAPE

Clean the tape path according to the correct procedure.

Turn the knurled locking ring on the supply hub counter-clockwise until the three locking clips retract into the hub. Place the reel of tape on the hub so that the tape will spill when the reel is rotated counter-clockwise. Gently push down on the reel until it is fully seated. Turn the knurled locking ring clockwise until it is tight and the reel is held firmly in place. Test by grabbing the edges of the reel and trying to remove it without loosening the hub.

The VPR-3's supply and take-up motors are extremely powerful. It is very important that the hold down be securely fastened or the VTR will not work properly and might possibly damage the hub, reel or tape.

Once the scanner and guides are dry, draw a short lead from the supply reel and carefully thread the tape following the threading path given in the diagram.

Feed the tape over the top of the take-up reel from the right side, since the take-up reel normally roattes counter clock-wise. After making sure the tape has grabbed the take-up reel, wrap a few additional turns around the take-up reel by turning the take-up reel counter-clockwise to ensure that the tape is tensioned and held firmly on the reel.

Avoid fold overs to ensure that the tape packs evenly. This is especially important with the VPR-3 to avoid vibration during wind operations at 500 ips.

Pressure the (READY) button on the operator's control panel to apply tension to the tape and start the scanner.

NOTE: Once tension has been applied to the tape, the two tension arms should not be touched. Injury to the operator and damage to the tape may result if the tension arms are forced.

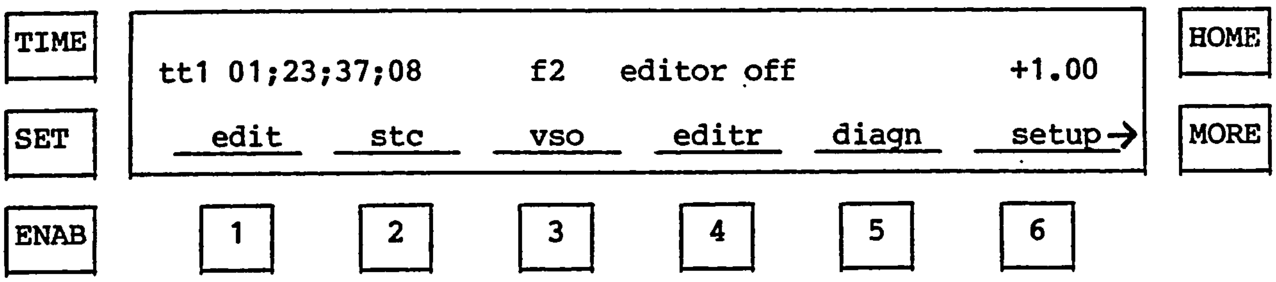
If the machine will not go into ready mode, check for too much slack around the tension arms. Rotate either the take-up or supply reel to remove the slack from the tape path.

Should the take-up reel turn upon readying the machine, the tape is not held tightly enough on the take-up reel. Immediately press(READY), to relax the tape and stop the scanner. Failure to do this may cause damage to the tape. Unwind the tape off the take-up reel and rethread ensuring that the tape is firmly gripped by the take-up reel.

FLUORESCENT DISPLAY AND SOFTKEYS

At the upper right of the operator's control panel is the fluorescent display. It is made up of a 26 x 256 dot matrix which displays letters, numbers and graphics. It is used to display tape position, editor status, and other information related to the operation of the VPR-3. The bottom line of the display is used as a "menu" to identify the functions of each of the six "softkeys" below the display.

By using this menu system, each of the six buttons can be assigned a number of different functions. The example which follows illustrates the use of the menu and six softkeys:



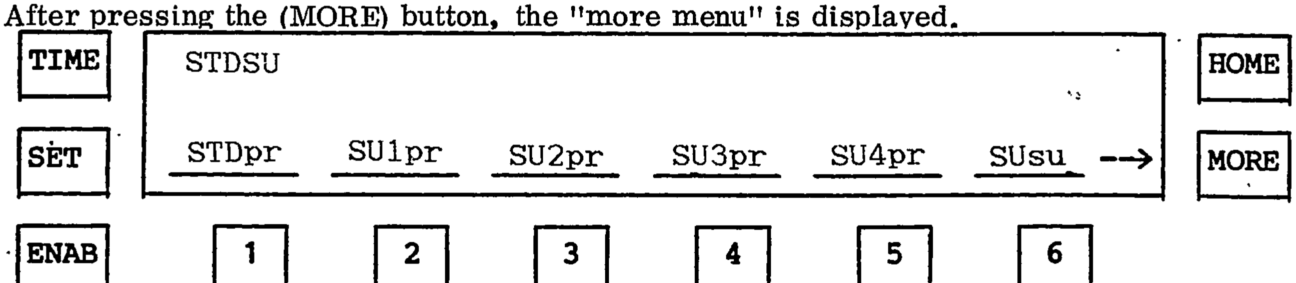
This is what the "home" menu looks like. (The numbers have been added to the softkeys for this example.) Beginning with the top line, from left to right, the display shows that tape timer 1 (tt1) is being used to display tape position in hours, minutes, seconds and frames (01;23;37;08); next is the field indicator (f2); editor status is next (editor off); the speed at which the tape will play when the variable speed mode is selected is shown in the upper right corner (+1.00).

The bottom line of the display is used to identify the softkeys below the display. These are the functions in the home menu and the functions they access.

1. edit - access the edit menus.
2. stc - access the 100 point search-to-cue menu.
3. vso - access the variable speed operations menu allowing special variable speed playback modes.
4. editr - toggles through the editor modes (off, insert, assemble)
5. diagn - accesses the maintenance diagnostics menus.
6. setup - accesses the setup menus.

Some menus, including the home menu, have an arrow to the right of softkey position 6. The arrow to the right of the setup softkey means there is more information in this menu. Since there are only six softkey positions, the remaining portion of the menu is displayed on another menu. To get to this information, press (MORE) to the right of the fluorescent display.

After pressing the (MORE) button, the "more menu" is displayed.



Note that there are now six more functions that access different modes than on the original menu.

TAPE TIMERS

In the HOME menu, and other selected menus, tape position information is displayed in the top left corner of the display. This position information can be from three different sources: tt1 (tape timer 1), tt2 (tape timer 2), and tcr (time code reader). Time is displayed as "hours: minutes: seconds: frames."

Tape timer 1 (tt1) and tape timer 2 (tt2) may be set or reset. The tcr mode will display time code as read directly from the time code that is striped on the videotape. This timer cannot be set or reset, and will always display tape time code when the tape is running.

Tape timer 1 is reset to zero to provide the cue for the cue-to-air operation. For this reason, it can be reset to zero whether or not it is displayed.

The tape timers, tt1 and tt2, are automatically reset when a new tape is loaded onto the VTR. The time that they are reset to is 23:58:00:00. This means that zero time is 2 minutes into the tape and with the standard 2 minutes bars and tone this would be the beginning of program.

Pressing the (TIME) button at the left of the display will toggle through the three tape timers.

SETTING THE TAPE TIMER MODE

The VPR-3 tape timers may be set to operate in the drop frame or non-drop frame (full frame) mode. The preferred mode is drop frame, which will correct for the difference between time code running at 30 frames/second and the color video rate of 29.97 frames/second.

Without drop frame, a color program picks up an extra 0.03 frames every second of time code. After an hour of time code has elapsed, the programs real running time will be 3 seconds and 18 frames longer than the indicated by the time code.

Drop frame time code reduces this error by omitting the first two frame counts (frames 00 and 01) at the start of each new minute, except every tenth minute. The tape timer reading then will agree with a program length that is measured with a stopwatch.

To select the drop frame mode press the (HOME) key, the (setup) softkey and the (MORE) key. This displays the (ttmod) softkey which toggles between "full" and "drop." Once the desired mode has been selected press (HOME) to return to the "home" menu.

The tape timer displays indicate which mode is in use: In the drop frame mode, the numbers are separated by semicolons (;) for field 2 and commas (,) for field 1; in full frame (non-drop) mode the numbers are separated by colons (:) for field 2 and periods (.) for field 1.

CHANGING THE TIME IN TAPE POSITION REGISTER tt1

The time in register tt1 may either be instantly set to zero (00:00:00:00), or to any desired preset time. The timer may be set or reset when the tape is parked or while it is rolling.

TO ZERO THE REGISTER

To reset tt1 to 00:00:00:00, press the (SET) button to the left of the display. The timer is reset and when tape rolls it will count from 00:00:00:00 when the tape moves.

NOTE: Pressing the (SET) button will always set or reset tt1 regardless of which register is displayed.

TO SET THE TIMER TO A PRESET VALUE

Enter the desired time into the keypad register using the numeric keypad at the center of the control panel. The specified time is displayed under the current tape position. When entering the time remember the last two digits will be the frames.

Transfer the time indicated in the keypad register to the timer register by pressing the (SET) button. The timer will count from the entered value when the tape is moved. If an invalid number was loaded in any of the time slots (greater than 59 for minutes and seconds or 29 for frames) then the number will not be entered. The invalid numbers will be shown in reverse display. The keypad register must be "cleared" and the correct number entered before it can be loaded into tt1.

CHANGING THE TIME IN TAPE POSITION REGISTER tt2

The time in register tt2 may either be instantly set to zero (00:00:00:00), or to any desired preset time. The same restrictions for setting or resetting tt1 apply to tt2. The procedure, though, is slightly different:

To set or reset tt2, press the (TIME) button to step to tt2. While holding down the (TIME) button press (SET).

NOTE: When tt2 is set or reset this will also set or reset tt1 to the same value.

STANDARD PLAYBACK SETUP

Before loading the tape to be played back clean the transport according to the approved cleaning procedure. Load the tape on the transport correctly, READY the transport and SHUTTLE forward to the pre-recorded bars and tone. On this section of tape carry out the following checks and adjustments.

AUDIO LEVELS CHECK

Playback mode audio level adjustments are made on the front panel. Each audio channel has own VU meter and playback audio level adjustment control. Pre-recorded tone should be set at 0VU on the meter. If adjustment is required, use the appropriate (AUDIO OUT) level control below the meter.

NOTE: If the (UNITY/VARIABLE) switch is set to the unity position, the audio level controls will not work.

To hear the audio during the level checks, select the appropriate channels on the audio monitoring selector switches.

AUDIO 1 & AUDIO 2 LEVEL CONTROL

Once the levels for channels 1 & 2 are set, the output of both can be adjusted together using the (A1 & A2 LEVEL) control. Pull the control out to activate it and adjust as required. NOTE: If the (UNITY/VARIABLE) switch is set to the unity position, this control will not work.

AUDIO 1 & AUDIO 2 MONO MIX

Audio channels 1 & 2 can be premixed and fed as a monaural audio output present at both audio channel output jacks. This is a very useful feature when preparing tapes with a voice-over announcer on one channel and natural sound or effects on the other. The following procedure, although not a normal playback set-up, is used to set-up the Mix 1 & 2 feature:

Preset the levels on audio channels 1 & 2 following the above procedure. Access the mix mode by pressing in order (HOME), (setup), (audio) and (1 & 2 mix). The (1 & 2 mix) softkey is an on/off pushbutton; pressing it alternately turns the mix feature on and off. When 1 & 2 mix is ON, the word 1 & 2 mix is in reverse display. The words "A1/A2 MIX" to the right of the (A1 & A2 LEVEL) control will also be lit to indicate that the VPR-3 mix mode is activated.

The (A1 & A2 LINE OUT) control is particularly useful in this mode. Pulling the control out activates it, allowing the control to be used as a master control for the mix.

The 1 & 2 mix mode will remain on until cancelled.

SETTING VIDEO LEVELS FOR PLAYBACK

On the waveform monitor switching select video out and the sweep on the monitor to 2V or 2H.

Before making these adjustments, it is very important that the waveform monitor vertical centering be adjusted to place the blanking line on the 0 IRE line.

Adjust the playback levels in the following order while playing back the standard color bar reference section of the tape.

NOTE: The controls will not work if the (UNITY/VARIABLE) switch is in the unity position.

Demodulator Level - For this adjustment the (DEMOD OUT) should be selected on the video waveform monitor selector. The sync tip should be on the -40 IRE units line, if necessary adjust the vertical centering of the waveform monitor, and then by adjusting the demod level control ensure that the peak is at 100 IRE. Return the monitoring to (VIDEO OUT) and ensure that the blanking line is on the 0 IRE units, adjusting the vertical centering if necessary.

Black Level - The waveform monitor should indicate a setup level of 7.5 units. If the level is incorrect adjust it with the (BLACK LEVEL) control located on the TBC control panel to the right side of the operator's control panel.

Video Level - The waveform monitor should indicate a video level of 100 units. If the level is incorrect adjust it with the (VIDEO LEVEL) control located on the TBC control panel.

Since black level (set-up) and video level interact, these adjustments should be repeated as necessary.

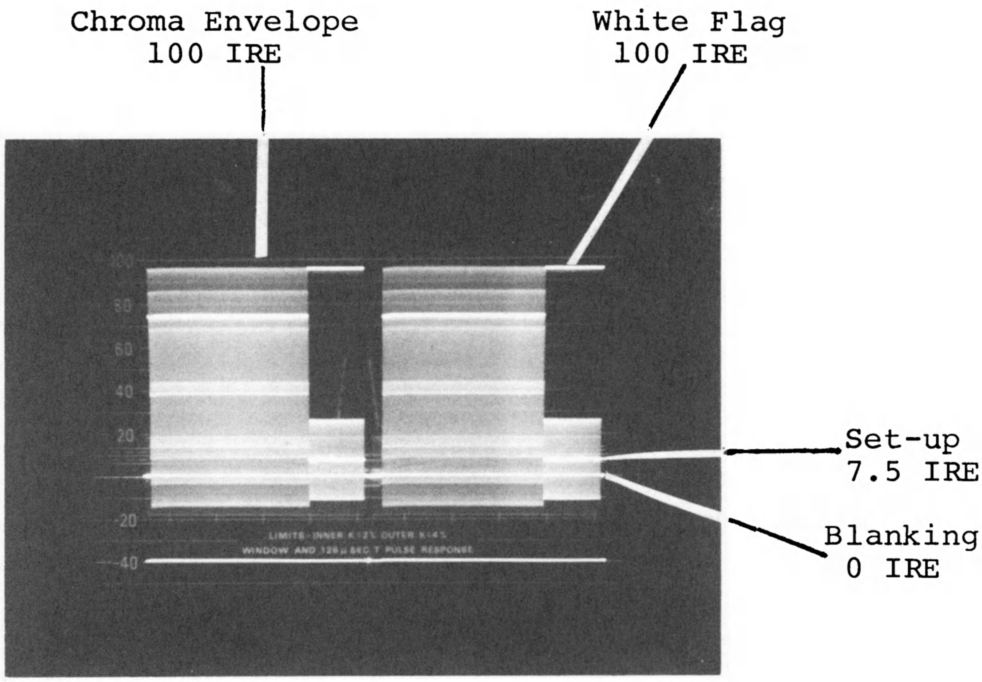
Chroma Phase - On the vectorscope the burst should be on the burst line. If it is not then adjust the phase control on the vectorscope. The blue vector dot should not lie in its appropriate box. If it is not use the (CHROMA PHASE) control located on the TBC control panel. As a result of this adjustment the other vectors should lie in their proper positions.

If as a result of these adjustments the vector dots are not precisely in the small boxes on the vectorscope proceed to the next adjustments.

Auto Chroma Reference Level - The chroma level should be at the same level as the white flag on the waveform monitor. If it is not the (AUTO CHROMA VARIABLE) adjustment is required. This is located on the edge of board 2, Demodulator, in the card cage. The switch towards the top should be in the down position to allow the control to be active and then adjusted to make chrome at the same level as the white flag.

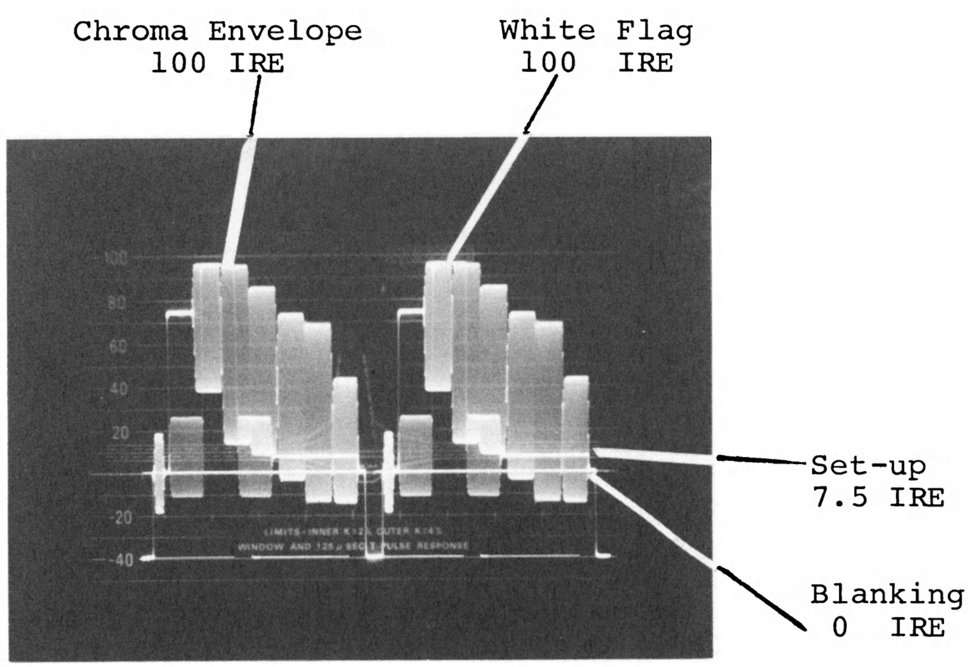
Differential Gain - If the yellow vector dot is out of the box when the blue vector dot is in then the differential gain requires adjustment. This control is the knob that is towards the top of board 3, Equaliser, and should be adjust to get all dots into the boxes on the vectorscope.

SCH Phasing Adjustment - An internal SCH monitoring system is provided to help eliminate shifts when editing. For normal playback to help determine correct picture position this control can be adjusted. Adjust the control under the SCH meter until the indicator on the meter is centered at 0°.



Video Set-up Waveform

WFM = 2V, Flat

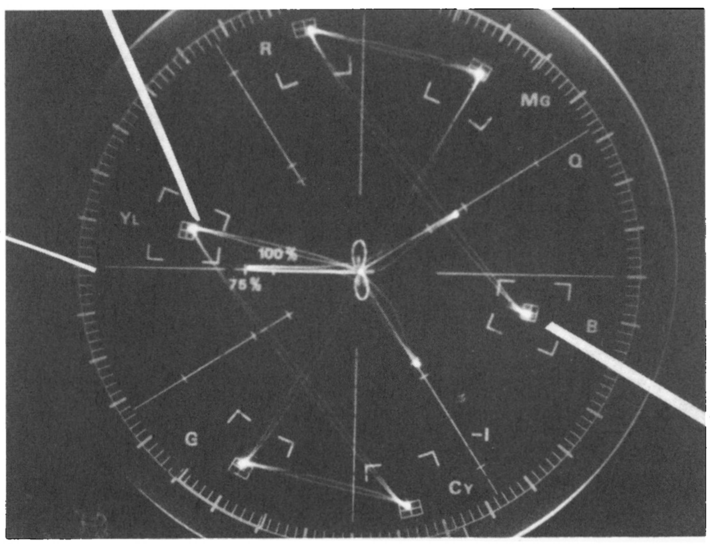


Video Setup Waveform

WFM = 2H, Flat

Yellow Vector
(picture left,
high luminance)

Reference
Burst Phase



Blue Vector
(picture right,
low luminance)

Vectorscope
Video Setup Waveform

SETTING UP THE VPR-3 FOR RECORDING

Prior to recording thoroughly clean the tape path and load the tape to be recorded onto the transport correctly.

RECORD INHIBIT SWITCHES

Video, audio 1, audio 2, audio 3 (time code), audio 4/sync, and control track are each independently protected from accidental erasure through the inhibit/record feature of the VPR-3. If the inhibit switch is on for any channel or channels, recording on the channel(s) will be locked out. In the inhibit position, no recording can be made.

Prior to recording, care should be taken that the correct channels are enabled for recording. For example, if it is desired only to record time code on audio channel 3, all other channels must be inhibited.

Call up the enable/inhibit menu, press (ENAB) (ENABLE) to the lower left of the fluorescent display. The following menu will be displayed:

v	a1	a2	a3	a4/ sync	CT

Press the softkey under the channel to be activated or inhibited. Each button is an on/ off switch; pressing the button will alternately turn the record inhibit for that channel on and off.

The status of the channel record inhibits may be changed from any menu by pressing the (ENAB) button. Use the softkeys as indicated in the display to enable or inhibit the desired channels for recording. The menu from which the enable menu was called may be recalled by pressing the (ENAB) button a second time.

An additional record lockout control may be found on circuit board A20 in the front of the electronics bay. When the two-position toggle switch is up (on), the record lockout is activated, and no recording on any channel may be made. The record inhibit switches will not function. The words "RECORD LOCKOUT" above the (RECORD) button will illuminate to indicate the feature has been activated. Placing the two-position toggle switch in the down (off) position turns the record lockout feature off, allowing control through the record enable/inhibit switches.

Another record lockout is found in the "edit - more" menu.

(HOME)→(edit)→(MORE)

tcr 2; 34; 27; 19			on		off
tag	rcall	undo	syncro		safe

When the safe feature is turned on, the VPR-3 will not go into record when the (RECORD) and (PLAY) buttons are pressed. This is to prevent the operator from accidentally making a straight recording while editing; edits, however, will be performed. If the VPR-3 will not go into record when the (RECORD) and (PLAY) buttons are pressed, check that the safe feature is off. The (safe) softkey alternately turns the feature on and off; the status is shown in the display above the word "safe."

As an additional safeguard, the word "safe" will appear on the top line of the home menu display to show that the feature is active.

tcr 2; 46; 15; 00	f2	editor_off		safe	+1.50
edit	stc	vso	editr	diagn	setup

OPTIMIZATION OF RECORD PARAMETERS

The adjustments for video and record optimization may be recalled from one of four different memories. The first three are electronic storage registers which may be set up automatically. These would be used to store setup parameters for three different tape types.

The fourth storage register is made up of manual controls located on the circuit boards in the front of the electronics bay. These controls are maintenance setups generally for the tape type most frequently used. If the operator is unsure of the settings in the tape type memories, the preset should be selected.

Prior to making a recording, the operator must check to see which optimization adjustments are being used. The three tape type selections, as well as the maintenance presets, may be selected by pressing (HOME), (setup), and (tape).

(HOME)→(setup)→(tape)

		TAPE 1			
tape 1	tape 2	tape 3	preset	setup	end

If a tape type is selected that has not been set up then both on the tape setup menu and the home menu there will be the diagnostics display, "TAPE TYPE NOT SET UP."

Additionally when selecting (tape 1), (tape 2) or (tape 3) the (MANUAL/AUTOMATIC) switch on board A1 in the front of the electronics bay must be in the up (automatic) position. When using the maintenance presets, the switch should be in the down (manual) position.

AUDIO LEVEL CHECKS

Set the (TAPE/INPUT) switch to input.

Record mode audio adjustments are done on the front panel. Each audio channel has its own input level meter and adjustment control. Incoming tone should be set at the 0VU level on the meter. If adjustment is required, use the appropriate input level control below the meter. Audio channel 3 may be used to record time code and if this is so then the correct level is +3VU on the meter.

SETTING VIDEO LEVELS FOR RECORDING

The video monitor selector switch should be set to demodulator video. The waveform monitor sweep should be set to 2V or 2H. The peak white calibrate pulse switch (second switch from the top on Modulator board A1) should be ON (up), and the scanner should not be running.

With a standard NTSC color bar signal as an input, use the (VIDEO IN) control to adjust the video level so that the white level is equal to the peak white calibrate pulse.

ALTERNATE METHOD OF SETTING VIDEO LEVELS FOR RECORDING

For this method the monitor selector switch should be set to modulator video. Adjust the levels in the following order using a standard NTSC color bar signal as input.

Video Level - The waveform monitor should indicate a video level of 100 IRE units. If the level is incorrect, adjust it with the (VIDEO LEVEL) control.

Chroma - The chroma level should be at the same level as the white flag on the waveform monitor. If it is not, use the (CABLE EQUALIZER) control on board A1 to adjust it.

MAKING A RECORDING

Once the VPR-3 has been set up according to the previously outlined procedures it is ready to make a standard recording.

Simultaneously press the (RECORD) and (PLAY) buttons to initiate recording.

To view the picture on the video monitor, press the (VIDEO OUT) button on the monitor select bus at the bottom left of the control panel. To hear the audio while recording, select the desired channels using the eight channel select buttons at the lower left of the control panel. Each audio channel can be assigned to either the left or right monitor speaker. Right and left speaker volume may be adjusted using the dual concentric controls to the left of the eight channel select pushbuttons.

End the recording by pressing the (STOP) button.

ANIMATION EDITING

In the VPR-3 animation is treated as a special edit function. Because of the ability of the transport to move tape rapidly and accurately the machine can make edits down to one field.

To set up for animation the editor must be in the animate mode. This achieved by being in the home menu and pressing the (editr) softkey until the word "insert" is displayed above it.

SETTING ANIMATION PREROLL

Since animate is treated as a special edit mode, the edit preroll is used for animation. To set the edit preroll the edit setup menu is to be displayed.

(HOME)→(edit)→(setup)

5:00	onstd	ct	unity	off	
prerl	cfrmr	cfsrc	trckng	edopt	end

Press the following buttons in order (HOME), (edit), (setup). From the keypad enter the desired preroll and enter it by pressing the (prerl) softkey. For animation a one second preroll is satisfactory for NTSC and a one to two second preroll for PAL.

To access the animation menu press the following keys; (HOME), (edit), (anim).

(HOME)→(edit)→(anim)

ttl 00; 02; 44; 03		en cel		ex don	
<s	>>	entry	cell	done	end

SETTING THE ENTRY POINT

Note: if you have been doing edits in the edit menu, the entry and exit points will remain in the animation menu.

Entry points can be loaded either from the selected tape time or from the keypad. The entry point is loaded simply by pressing the (entry) softkey after the desired point is found on tape with the selected tape timer or the number is loaded into the keypad register from the keypad.

CELL SIZE

Edit duration or cell size is set from the keypad. The cell length is entered by pressing the appropriate keys on the keypad, being whole frame numbers or a field with the field key. The number is entered to the (cel) register by pressing the (cell) softkey.

When the cell length is entered the exit point is automatically calculated to be the entry point plus the cell length.

DONE SIZE

The done register keeps track of the amount of animation editing that has been done. It is normal at the start of an animation sequence to zero the done register by pressing 0 on the keypad and then pressing the (done) softkey. If there was already some period of animation already on the tape then this period could be entered into the done register from the keypad.

PERFORMING THE ANIMATION EDIT

Once the preroll time, entry point, cell size and done time are set the system is ready to do the animation edit. The "edit animation" menu is now as follows:

tt1	00;00;00;00;	en 00;00;00;00		ex 00;00;00;01	
		cel 00;00;00;00		don 00;00;00;00	
≪	≫	entry	cell	done	end

To perform the edit press the (EDIT) button. The VPR-3 will search to the entrance point minus the edit preroll time, go into PLAY RECORD mode, perform the edit at the entry point and then search back to the new entry point minus the edit preroll time.

When the animation edit is performed, the entry and exit points and the done registers are all automatically incremented by the cell size. The VPR-3 has cued back to the new entry point minus the edit preroll and is ready for the next animation edit.

REVIEWING INDIVIDUAL ANIMATION EDITS

The animate review softkeys ≪ and ≫ are used to review the animation edits that have been done. The ≪ softkey scrolls done one cell while the ≫ softkey scrolls up one cell. When these keys are used the entry, exit and done registers are scrolled accordingly. The VPR-3 also cues to the new entrance point.

By using the animation review keys the edit point can be moved forwards or backwards one cell at a time. If a cell is found that needs to be redone then press the (EDIT) key and the VPR-3 will perform a 1 cell edit on this cell.

SEARCH TO CUE:

The VPR-3 can store up to 100 cue points for easy and immediate access. The cue points can be specified in three ways:

1. While tape is parked at a desired cue point.
2. While tape is rolling.
3. As a preselected value using the numeric keypad.

Cue points may be entered referenced either to tt1, tt2 or tcr. When searching to cue points, it is necessary to be using the tape position register from which the cue points were taken.

(HOME)→(stc)→(search-to-cue)

frame

tcr: 1;29;17;20		f2	field		+1.25
			cue point	#02-->	1;25;18;15
cue# ↓	cue# ↑	cue#	ast	clear	enter

Press the (TIME) button to select the desired tape time display mode. Enter the search-to-cue mode by pressing the (stc) softkey on the home menu. If desired press clear to clear the cue point location displayed. This is not essential when a new cue point is entered the old point is automatically cleared and lost.

A new cue point number may be specified by typing the desired number on the keypad, and pressing (cue#). It is also possible to change the cue point number by scrolling through the cue point list using either (cue# ↓) (scroll down) or (cue# ↑) (scroll up) button.

If the tape is parked at the desired cue location, press (enter) to transfer the displayed time value to the cue point register. The cue location may also be entered "on-the-fly" by pressing (enter) as the tape is moving.

If the location of the cue point is already known, the value may be typed on the keypad and entered as the cue point value by pressing the (enter) softkey.

RECALLING A PRESELECTED CUE POINT

Press the (TIME) button to select the desired tape time display mode. Enter the search-to-cue mode by pressing (stc) on the home menu.

With the (ast) (automatic scan tracking) softkey select either the field or frame mode. This key toggles between them. Field should be selected when playing back or freezing sequences with motion. Frame should be used when playing back graphics.

Enter the desired cue number either via the keypad or scrolling.

Once the desired cue point is displayed, press the (SEARCH) button, located below the six softkeys. The tape will search for and park at the selected cue point. If the (CUE) button is pressed the tape will search for and park at the cue point minus the set system preroll.

LEARN SEQUENCE MODE

(HOME)→(vso)→(Lrseq)

tcr:	2;19;11;00	DUR:	2:00:00		-1.00
		en:	2;15;43;18	ex:	2;17;43;18
clear	learn	entry	rplay	exit	end

LEARNING

The "Lrseq" (Learn Sequence) mode enables the VPR-3 to memorize complex variable speed sequences for special effect plackbacks during air play or editing. The VPR-3 can memorize up to 2 minutes of real time variable speed effects.

Enter the learn sequence by pressing, in order, HOME, (vso) and (lrseq). Select the desired Tape Timer for the effect by pressing the TIME button until the desired register is displayed. Clear any previously memorized sequences by pressing (clear).

Locate the area on the tape which contains the segment to be replayed. Park the tape at the spot the variable speed segment will begin. The speed indicator in the upper right portion of the display shows the speed at which the tape will play when the (VAR) button is pressed. Adjust the Knob to the desired starting speed.

Press (learn). The word learn will be highlighted in reverse display to indicate that the learn mode is activated.

Press the (VAR) button to initiate the learn process. The tape will start to move at the speed shown on the indicator. The VPR-3 can now be "taught" the speed transitions by rotating the control knob for the desired effect.

Note that upon initiating the sequence the entry point is loaded and the duration counter is incrementing in real time. This timer keeps track of the elapsed time of the variable speed sequence from the point it began, regardless of the tape speed.

When the segment has finished, exit the learn mode by either pressing the (learn) softkey again or STOP. When the machine exits the learn mode the exit point is loaded and the duration timer stops counting.

The exit time of the memorized segment must be at a point after the furthest forward point in that segment, or in replay the replay will be ended at the exit point without completing the remainder of the sequence. If this is not the case then a suitable time may be added to the exit point, a suitable time being 5 mins. This is done with the keypad by pressing 5:00:00, +, and the (exit).

REPLAY

Once the sequence has been memorized, it can be recalled and replayed at any time. The changes in speed entered into the VPR-3's memory may also be applied to any segment of tape.

Enter the replay mode by pressing (rplay). The word "rplay" will be highlighted in reverse display to indicate that the replay mode is active. Press the VAR button. The tape will play back at the variable speed entered into the memory during the learn mode.

CONTROL TRACK REWRITE

If a tape is recorded with incorrect phase or no control track then it can be rewritten. This is achieved by using the synthetic control track feature of the VPR-3 where the control servo is locked to the off-tape video and this is used to produce a new control track that is recorded on tape.

Access to this mode is in the "servo-setup-more" menu. Ensure that the editor is OFF.

(HOME)——► (setup)——► (servo)——► (more)

off	off	norm		unity	
synCT	ctrw	svgain		trkng	end -->

WRITING NEW CONTROL TRACK

This is done to a tape where for the entire recorded portion there is no or bad control track.

Ensure that the (UNITY/VARIABLE) button is selected to unity. This mode will give a highlighted "unity" label above the (trkng) softkey. Select control track on the waveform monitoring.

Press the (synCT) softkey to access synthetic control track playback, the label will become "on".

Ensure that the tape is positioned at the head of the section for which new control track is to added. Press the (ctrw) softkey, the label will go to "on." In this mode if the HOME menu is returned to there will be a "diagnostics display" NONSTD-CT REWRITE. The video and audio channel record inhibit indicators will also be light.

Press (PLAY) and (RECORD) to initialize the recording. Press (STOP) once the end of the recording is reached.

REWRITING A PORTION OF CONTROL TRACK

This is used where only a portion of the control track requires to be rewritten. It will be necessary to phase the machine up to the good portion of the control track before going into record so that there will be continuous phase throughout the recording.

With the (UNITY/VARIABLE) button select variable. The label above the (trkng) softkey will be unhighlighted "unity" or "non-std." On a portion of the tape that has good control track go into PLAY. While observing the control track waveform press the (synCT) softkey. If there is a change in the control track phase then press the (trkng) softkey and with the KNOB adjust the phase so that the phase is the same as it was with synthetic control track off. To ensure that the pase is correct toggle the (synCT) softkey "on" and "off" while adjusting the KNOB to obtain correct phasing.

Press the (ctrw) softkey, the "on" label will be displayed.

Return to the HOME menu, located a position near the start of the portion of tape with bad control track. Select ttl and zero. Press (PLAY) and (RECORD) and record for the period of tape that new control is required.

VPR3 Control PWA 20

Switch 7 Functions.

S7-1 OFF Normal VPR3 operation, waits for scanner lock before going into record.
ON VPR3 goes into record immediately, rather than wait for scanner lock.

S7-2 OFF Control Panel active while in remote.
ON Control Panel operation inhibited while in remote.

S7-3 OFF Tape video displayed during search.
ON EE video displayed during search.

S7-4 OFF Noise protection disabled.
ON Noise protection enabled.

S7-5 Unused.

S7-6 OFF Inhibits access to audio record timing menu.
ON Enables access to the audio record timing menu.

S7-7 OFF Normal.
ON RAM clear mode, doing a First Birthday on every power up. (This should be used only if the RAM is trashed so bad that a normal First Birthday cannot be done, i.e. the CPU wont wake up).

S7-8 OFF Inhibits User Setup Learn.
ON Enables User Setup Learn and Labels.

VPR-3 USER SETUP LEARN
PROGRAM VERSION 5.X

A record of user set-ups should be maintained for each of the four set-ups on the SET-UP menu. If the need to do a first birthday arises, as when a software update is installed, the menus are set to a default condition shown in **bold letters** below. Audio record timing set-up values are also set to their default value. The time code generator is put in HOLD mode until cancelled by a soft key or Audio 3 record is initiated.

ACCESS PATH FOR USER LEARN SET-UPS

Video Pre-process	[HOME] [setup] [video] [p proc]		[**off**/on]
Playback Head	[HOME] [setup] [video] [pb head]		[**ast hd**/rcrd hd]
Audio 1&2 Mx	[HOME] [setup] [audio] [1&2mx]		[**off**/on]
Audio Process	[HOME] [setup] [audio] [proc]		[**off**/on]
AST	[HOME] [setup] [servo] [ast]		[**field**/frame]
Color Framer	[HOME] [setup] [servo] [crfmr]		[**onstd**/oninv/off]
Clr Frmr Source	[HOME] [setup] [servo] [cfsrc]		[**vid**/ct/tc]
Remote Edit Field	[HOME] [editor] [setup] [MORE] [remfld]		[**field2**/remote/ field1]
Reel Servo Gain	[HOME] [setup] [servo] [MORE] [svgain]		[**norm**/low]
TAPE Setup	[HOME] [setup] [tape] [tape1-tape3/preset]		[**preset**/tape 1-3]
Char Gen status	[HOME] [setup] [chgen] [chgen]		[**on**/off]
Character Gen	[HOME] [setup] [chgen] [chgen]		[**on std**/on inv/off]
Char Gen display	[HOME] [setup] [chgen] [mode]		[**ttm**] [various]
Time code clr fr	[HOME] [setup] [tcgen] [tc ϕ]	NTSC	[**tc ϕA**/tc ϕB]
		PAL	[**STDA**/NONSTDA/ STDB/NONSTDB]
Time code source	[HOME] [setup] [tcgen] [src]		[**int**/ext/jam/slv]
Time code frame	[HOME] [setup] [tcgen] [df/ff]	NTSC	[**drop**/full]
		PAL	[full]
System Pre-roll	[HOME] [setup] [MORE] [syspr]	NTSC	[**5:00**]
		PAL	[**7:00**]
Edit pre-roll	[HOME] [edit] [setup] [prerl]	NTSC	[**5.00**]
		PAL	[**7.00**]
Tape Timer mode	[HOME] [setup] [MORE] [ttmod]	NTSC	[**drop**/full]
		PAL	[full]
Remote 1	[HOME] [setup] [MORE] [rem1]		[**paral**/serial]
Serial	[HOME] [setup] [MORE] [serial]		[**SMPTE**/VPR3/SMC]
Remote Switches	[control panel Remote 1 & 2 switches]		[**OFF**]
Time	[HOME] [TIME]		[**tt1**/tt2/tcr]
Rcrd Chan enable	[ENAB] [individual enables]		**all enabled**
Edit mode	[HOME] [editr]		[**off**/insert/assem]
Sycronize	[HOME] [edit] [MORE] [syncro]		[**on**/off]
Label	[HOME] [MORE] [SUsu] [SUsel] [lblsu] [KNOB]		[**STDSU**]

VPR 3 USER SETUP RECORD

Machine No.__________ Serial No.________________ Room No.________________

Date________________ Operator____

Soft Key	[STDpr]	[SU1pr]	[SU2pr]	[SU3pr]	[SU4pr]
label	[STDSU]				
video pre-process	off				
playback head	ast				
audio 1&2 mx	off				
audio process	off				
ast	field				
color framer	on std				
clr frmr src	std				
rem field	field 2				
reel servo gain	norm				
tape	PRESET				
char gen status	on				
char gen	on std				
char gen display md	ttm				

Soft Key/Label	[STDSU]				
tm code color frm *					
time code source	int				
time code frame *					
system preroll tm *					
edit preroll tm *					
tape timer mode *					
remote 1	paral				
serial	A-SMPTE				
remote switchs	both off				
TIME	ttl				
REC chan en	all				
EDIT mode	off				
sycronize	on				

* Depends on standard - NTSC/PAL

AUDIO RECORD TIMING SETUP
CONTROL PWA S7-6 controls access to [rectm] menu

Erase In: [HOME] [setup] [audio] [rectm] [ersin] **[2.0]**	
Erase Out: [HOME] [setup] [audio] [rectm] [ersot] **[5.0]**	

VPR 3
OPERATIONS #7
CUE AND SEARCH RULES

1. Pressing **CUE** and **SEARCH** simultaneously:
   - All menus
   - Parks at TT #2 00:00:00:00 minus system pre-roll

2. If a number is present in **keyboard entry slot** of the menu, as a result of **COPY** or a key pad entry: result of COPY, or keyboard entry (except TRIM):
   - All menus
   - Searches to that number with respect to selected timer (TT#1, #2, or TCR)
   - Cues to that number minus the system preroll. If the **EDIT** menu has been selected, then the EDIT pre-roll is used.

3. If the Keyboard register display is empty, or has a TRIM number in it, and EDIT or STC menu has **not** been selected:
   - Searches to TT#1 00:00:00:00 ± trim.
   - Cues to TT#1 00:00:00:00 ± trim - system preroll.

4. **Editor menu:**
   - Searches to ENTRANCE ± trim with respect to selected TT#1, TT#2, or TCR.
   - Cues to ENTRANCE ± trim - system EDIT pre-roll.

5. **Search to Cue (STC) menu:**
   - Searches to CUE # time displayed ± trim, with respect to selected TT#1, TT#2, or TCR.
   - Cues to CUE # time displayed ± trim - system pre-roll.

VPR3 CONTROL PWA 20
Switch 7 Functions
Version 6 Software

S7-1	OFF	Normal VPR3 operation, waits for scanner lock before going into record.
	ON	VPR3 goes into record immediately, rather than wait for scanner lock.
S7-2	OFF	Control Panel active while in remote.
	ON	Control Panel operation inhibited while in remote.
S7-3	OFF	Tape video displayed during search.
	ON	EE video displayed during search.
S7-4	OFF	Normal NTSC operation. Serial output of tape time has a 2 Frame delay.
	ON	Normal PAL operation. Serial output of tape time does not have a 2 frame delay.
S7-5	OFF	Normal position.
	ON	SPECIAL FUNCTION; for future development. If used then the message "S7-5 ON EFFECTS REC TIMING" is displayed in the menus.
S7-6		Unused
S7-7	OFF	Normal
	ON	RAM clear mode, doing a First Birthday on every power up. (This should be used only if the RAM is trashed so bad that a normal First Birthday cannot be done, i.e. the CPU wont wake up).
S7-8	OFF	Normal position, this inhibits changing any of the menu enables in the <mnenb> menu. Provides operator lockout of preset functions.
	ON	Allows changing of the enables in the <mnenb> menu.

Tape Timer Display shows the selected Tape Timer. Either tape timer 1 [tt1] or [tt2] or Time Code Reader [tcr]. For the tape timers it is a field display that operates Full Frame or Drop Frame, as selected in the SET-UP-MORE menu.

For Full Frame, period or colon is used:
00.00.00.00 Field 1, 3
00:00:00:00 Field 2, 4
For Drop Frame, comma or semi-colon
00,00,00,00 Field 1, 3
00;00;00;00 Field 2, 4

When tape initially blocks the Tape in Transport sensor, both tt1 and tt2 are set to:

FF: 23:58:00:00
DF: 23;58;00;02

Field Indicator Indicates the Demod Video field. In STILL it indicates the field the transport is stopped on.

EDITOR status as selected by [editr] soft key. Will be off, insert, or assemble. Status also displayed above [RECORD] button.

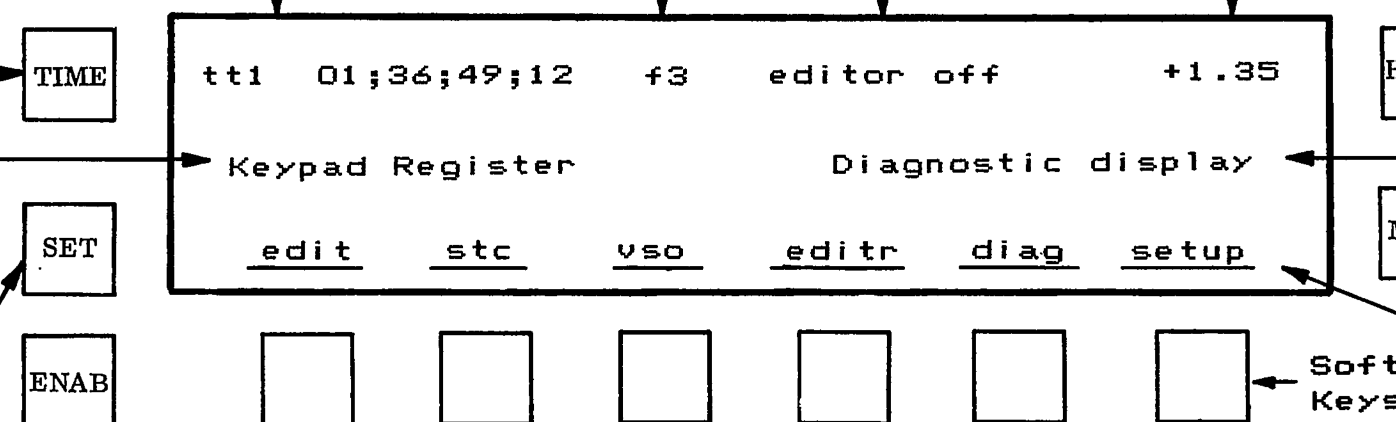
Variable speed indicator. The number represents the speed times PLAY that tape will be moved when VARIABLE PLAY is selected.

In any menu, this key will return the display to this HOME menu.

Selects Tape Timer to be displayed. Toggles tt1, tt2, and tcr.

When buttons on the 10 digit keypad are pressed they will be displayed in this area for transfer to other registers.

Displays 47 machine status conditions and faults, when a fault exists.



In some menus, including HOME, more than six soft keys are required. The arrow on the display indicates this. By pressing the MORE key the extra menu is available.

SET key allows setting of the tape timers. Upon pressing SET the contents of the keypad register is transferred to tt1. If the keypad register is empty, tt1 goes to 00,00,00,00,. To set tt2 the SET button must be pressed as the TIME button is held down and tt2 accessed. This will also change tt1.

Accesses the edit menu allowing auto edit functions.

Access the VSO VARIABLE SPEED OPS menu allowing special variable speed playback.

Accesses to the diagnostics menu to aid trouble-shotting.

Accesses the ENABLE Menu that allows individual channel Record Enables/inhibits. INHIBIT is also displayed under the appropriate soft key. This can be accessed from any menu and on re-pressing (toggle action) the key it will return to the original menu.

Access to the 100 point SEARCH TO CUE menu.

Access to the SET-UP menus allowing the VPR-3 to be set-up for certain operational parameters.

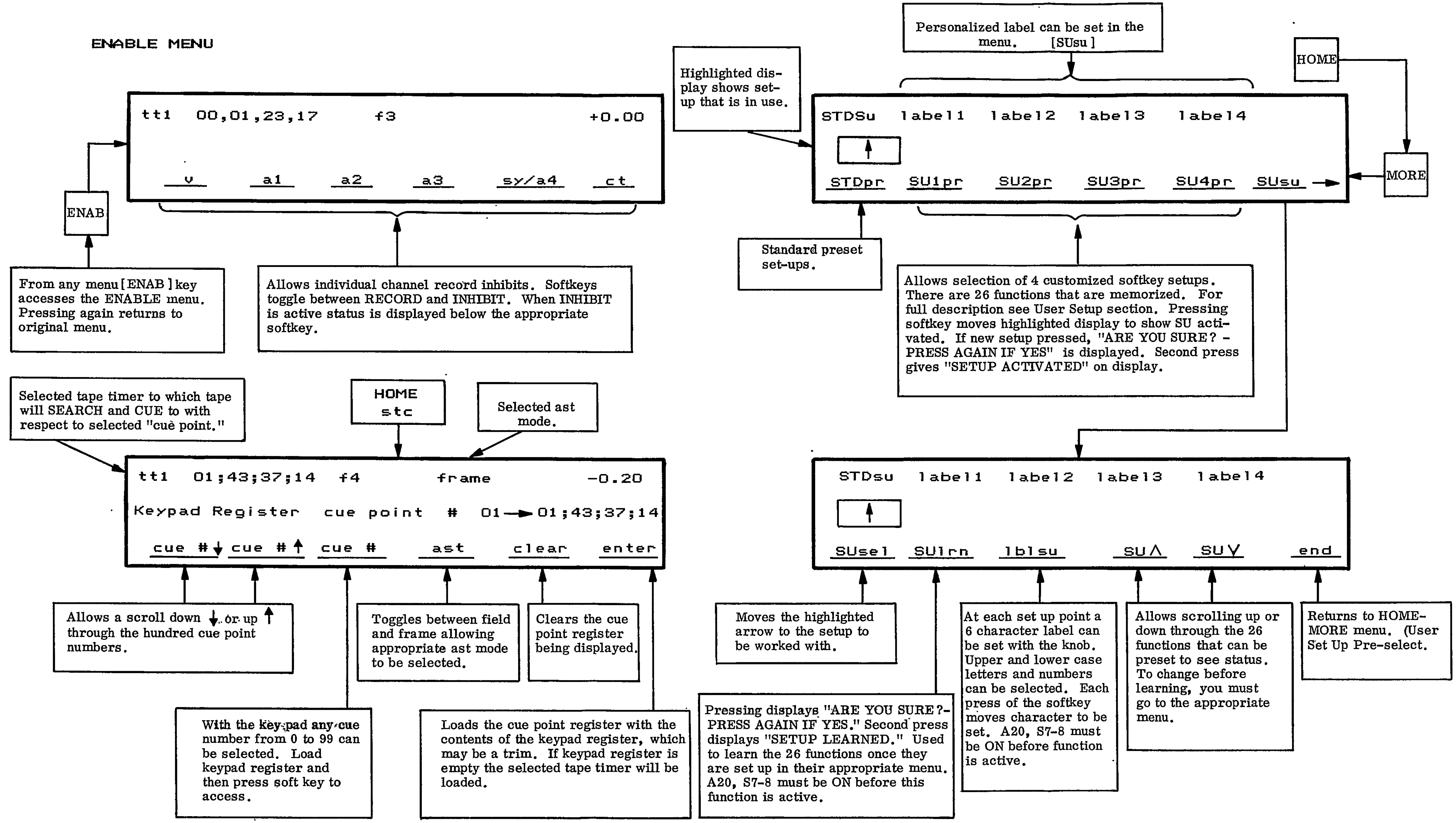
Controls the EDITOR. Turns it on/off.
Toggle: OFF
INSERT
ASSEMBLE
Status is also displayed above the RECORD key.

VPR-3
OPERATIONS
HOME MENU

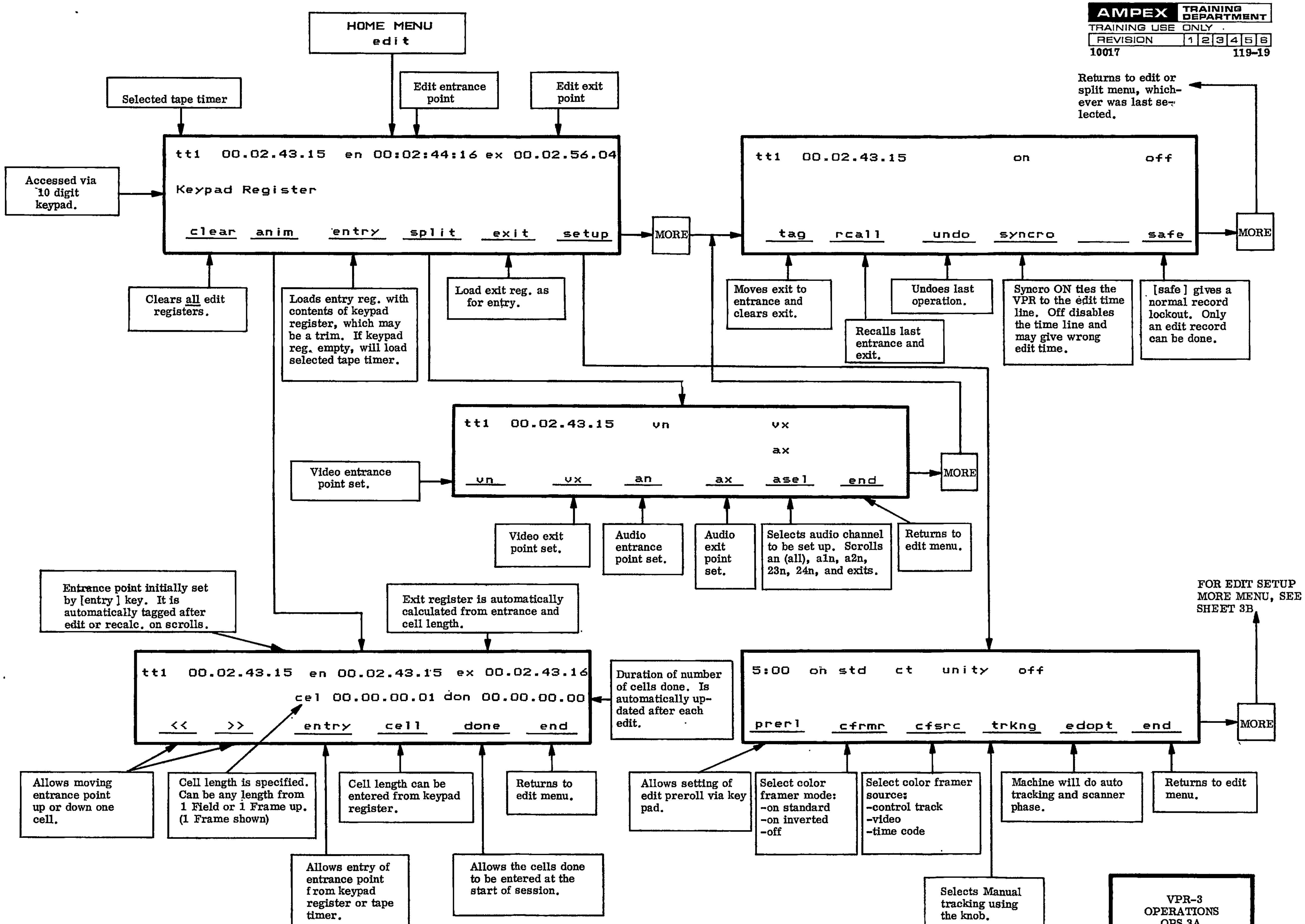
USER SETUP

PRESELECT MENU

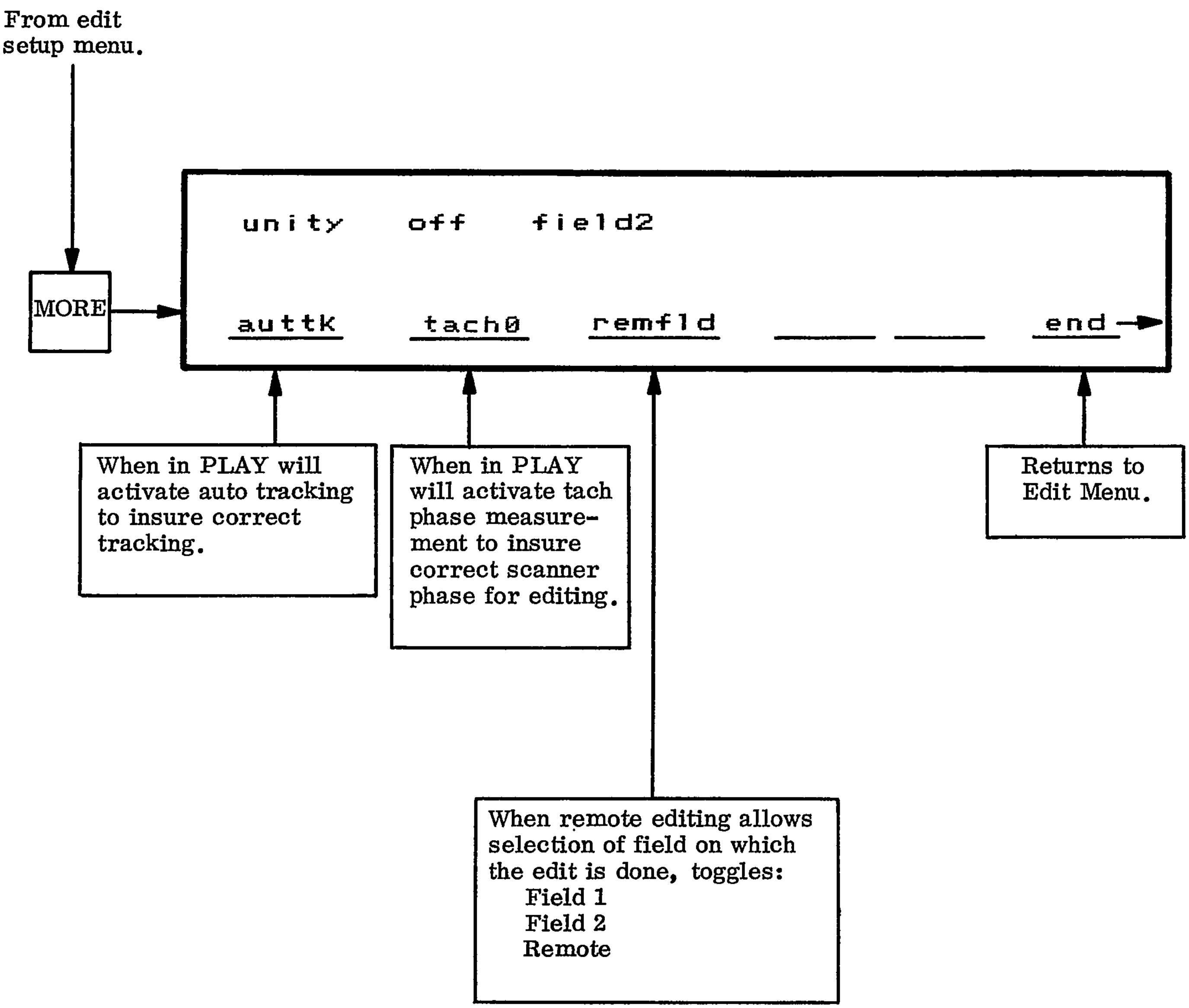
ENABLE MENU



VPR-3
OPERATIONS
OPS 2
ENABLE, USER, PRESELECT
AND
SEARCH TO CUE MENUS



VPR-3
OPERATIONS
OPS 3A
EDIT MENU



VPR-3
OPERATIONS
OPS 3B
EDIT SET UP MORE MENU

SERVO SETUP MENU

HOME MENU
setup

servo

field on std ct nonstd off
ast cfrmr cfsrc trkng tach0 end

MORE

off off norm nonstd
synCT ctrw svgain trkng end→

- ast: Selects ACT mode, field or frame re-play.
- cfrmr: Determine color frame mode for capstan servo. Toggles On standard On inverted Off.
- cfsrc: Selects color frame source: Control track Video Time Code
- trkng: Accesses the variable tracking using the knob.
- tach0: Measures scanner phase error for edit phasing.
- end: Returns to setup menu.
- synCT: Turns on synthetic control track replay.
- ctrw: Enables Control Track rewrite allowing new control track to be recorded.
- svgain: Toggles servo gain from normal (high) speed lock-up to low giving slower accell-eration during fast wind modes.
- trkng: Allows variable tracking using the knob.
- end→: Returns to setup, menu.

TIME CODE GENERATOR SETUP MENU

HOME MENU
SETUP

TCGEN

tcg 13.56.12.26 0A int drop
hold enter tc0 src df/ff end→

MORE

aaaa
↑
usb

- hold: Stops TCG from running.
- enter: Allows entry of time to the TCG via the keypad.
- tc0: Toggles Phase A, Phase B, determining whether color Frame ID flag is on Frame A (STD) or Frame B.
- src: Selects the source for the TCG. Toggles [ext] External [int] Internal [jam] Locked to tc reader [slv] Slaved to ext time code generator
- df/ff: On 525, selects full frame or drop frame mode.
- end→: Returns to setup menu.
- usb: On pressing soft key, arrow moves to each of 4 characters, that may be set with the knob.

CHARACTER GENERATOR SETUP MENU

HOME MENU
SETUP

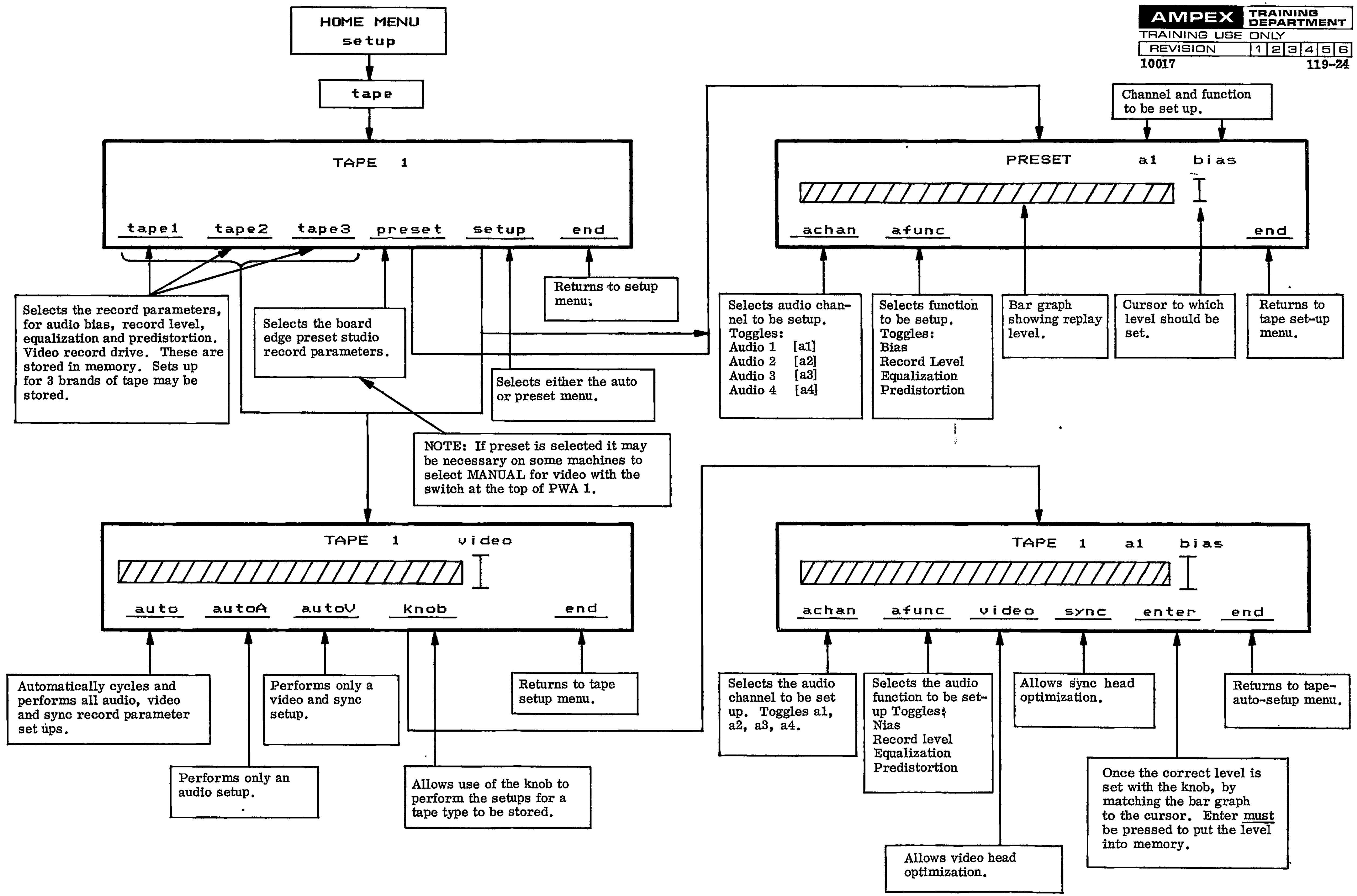
CHGEN

off on on std ttm
pos status chgen size mode end

- pos: Toggles: Off horiz position vert position allowing the characters to be positioned on the monitor.
- status: Turn on/off fault status of diagnostics on character display.
- chgen: Mode of Chara Generator. Toggle: OFF On std-Blk chara on inv-white chara
- size: Toggles: Large Small
- mode: Selects mode of display tcr, ttm (selected tape timer) user bits, tcg, all of the above together.
- end: Returns to setup menu.

VPR-3
OPERATIONS
OPS 5B

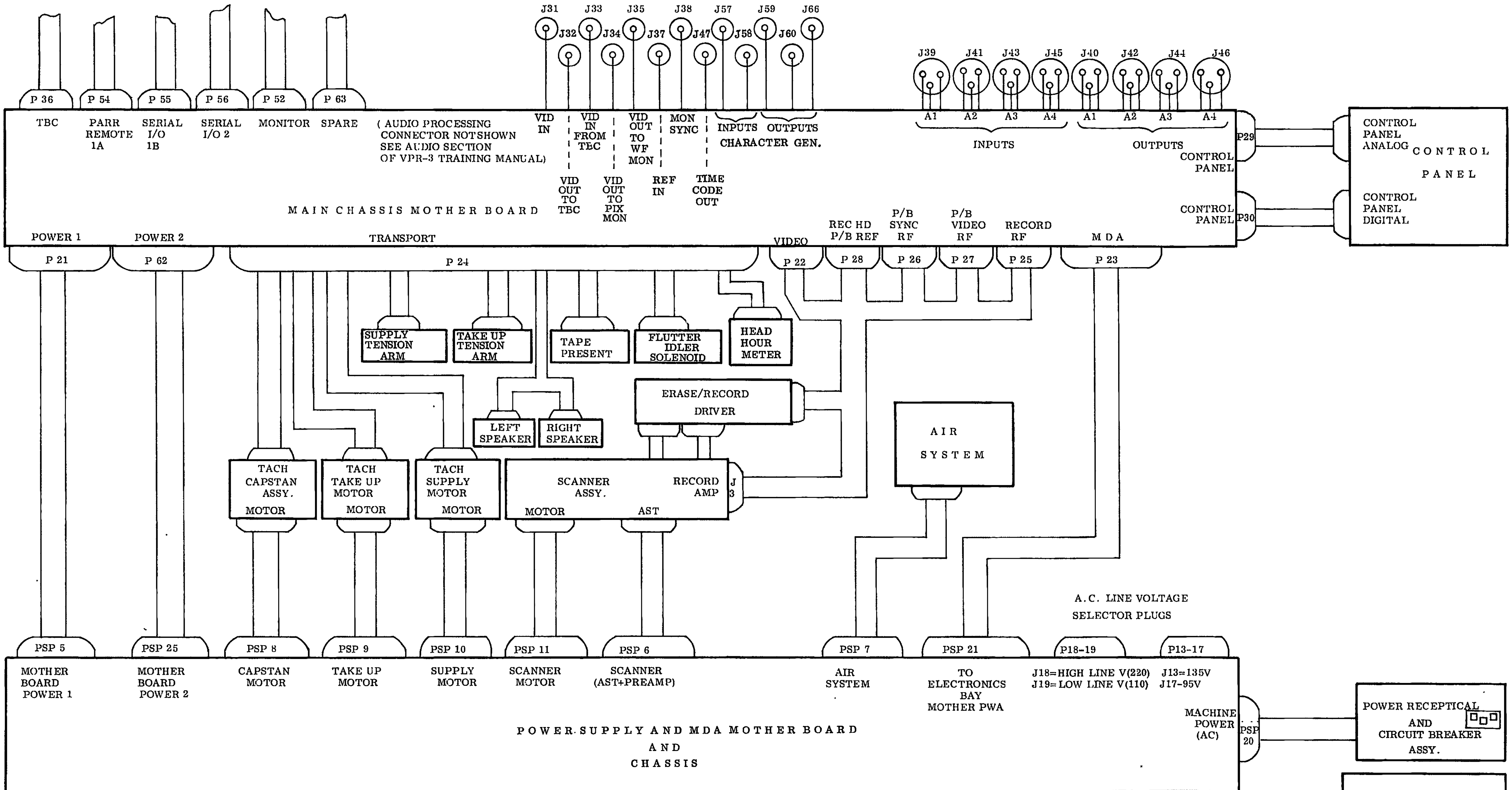
SERVO, TIME CODE, CHARACTER GENERATOR, SET UP MENUS



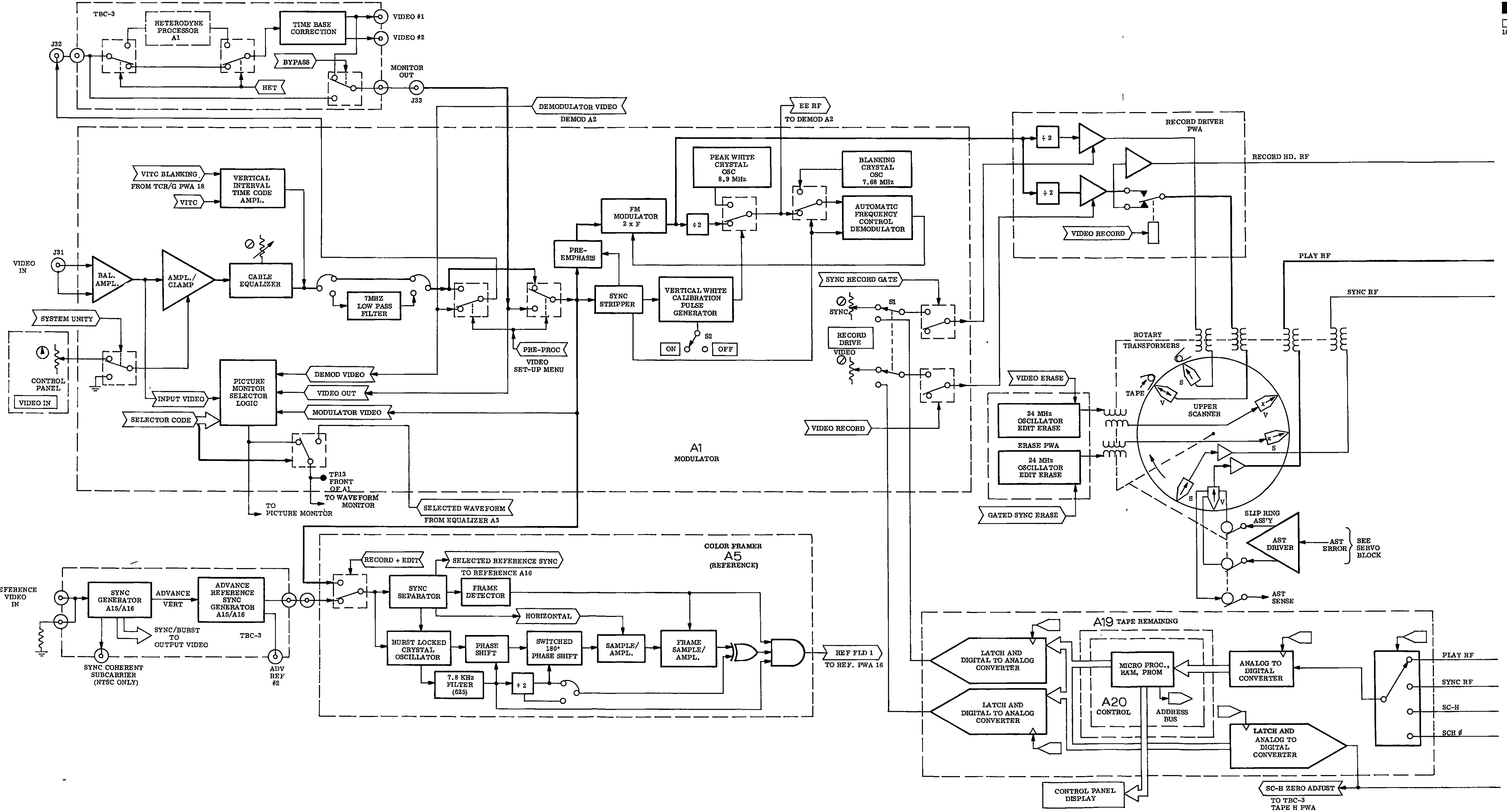
For audio setups the following signals are internally generated:
Bias: 10 kHz at 0 VU
Record Level: 1 kHz at 0VU
Equalization: 10 kHz at 0 VU
Predistortion: 1 kHx at +8 VU

VPR-3
OPERATIONS
OPS 5C

TAPE SETUP
MENUS

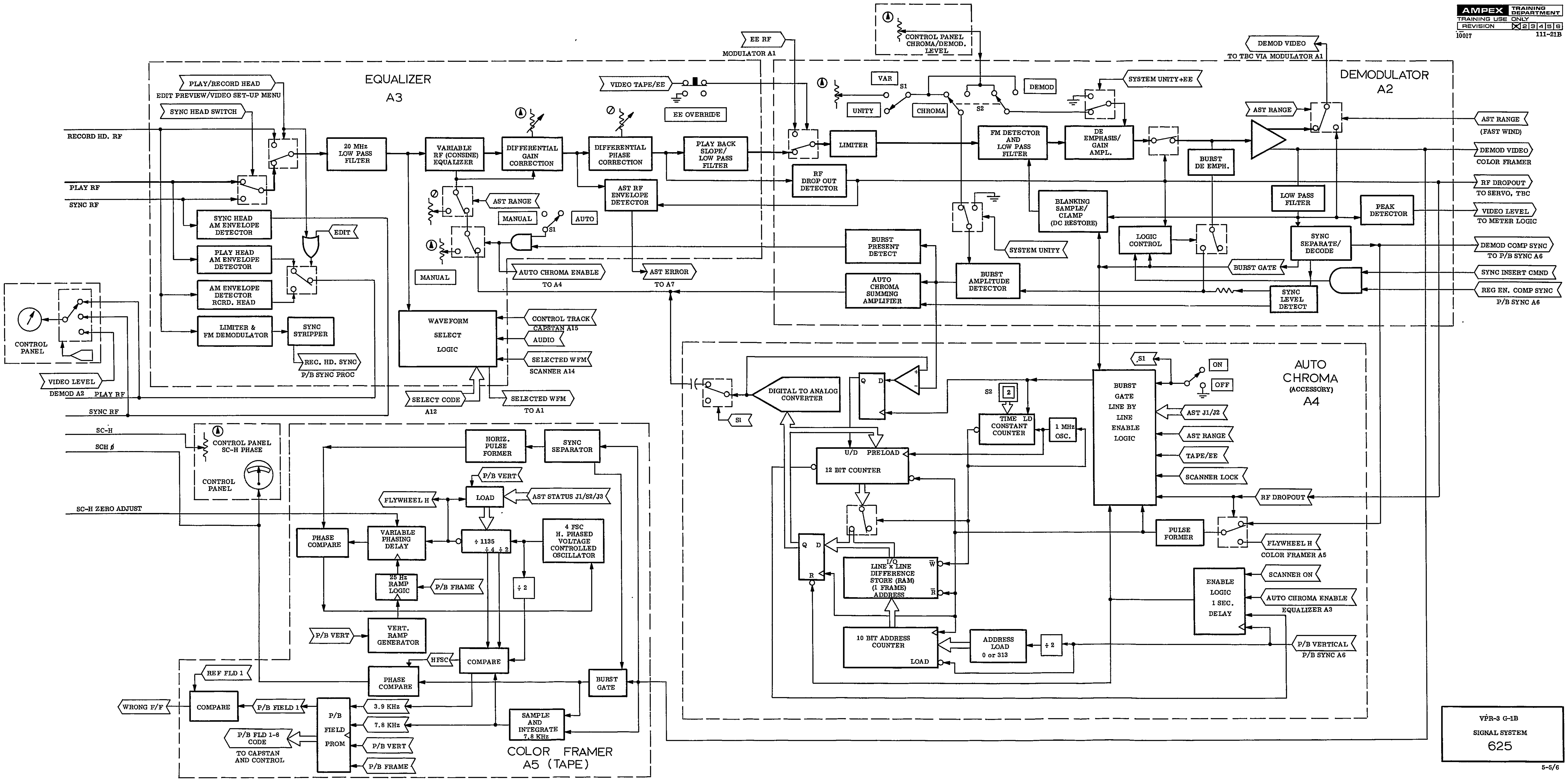


VPR-3
GENERAL SYSTEM INTERCONNECT

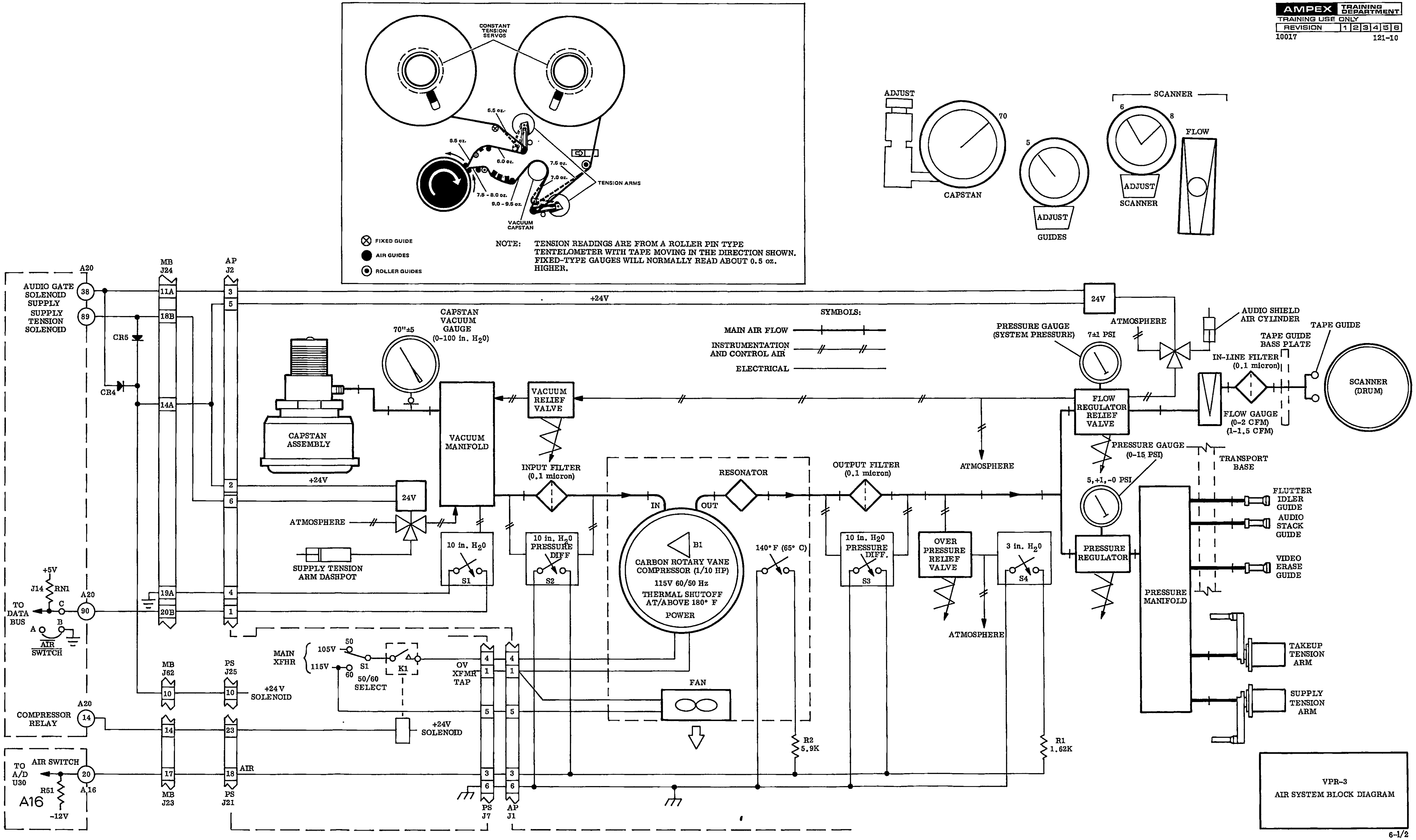


VPR-3 G-1A
SIGNAL SYSTEM
625

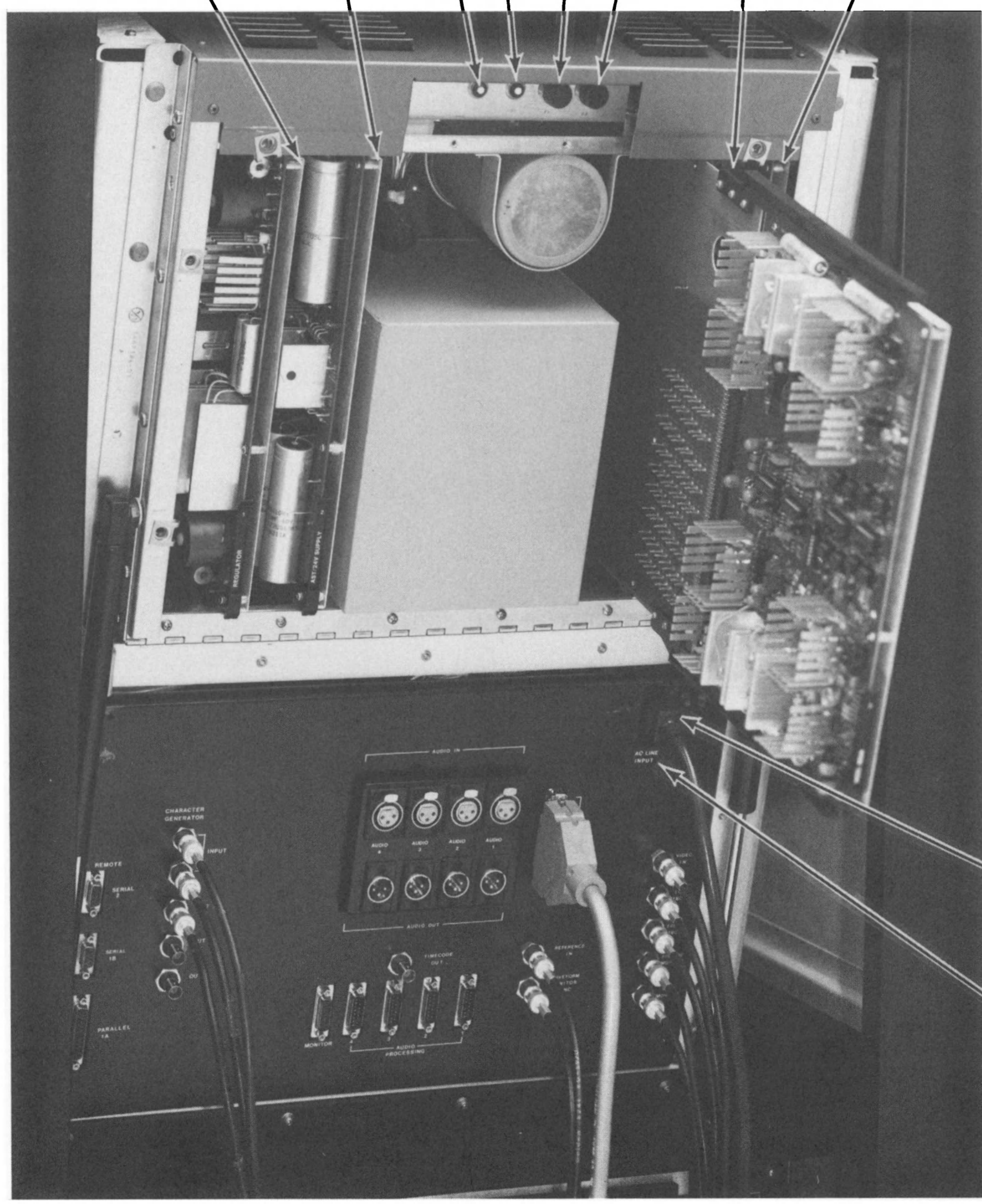
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 2 3 4 5 6
10017 111-21B

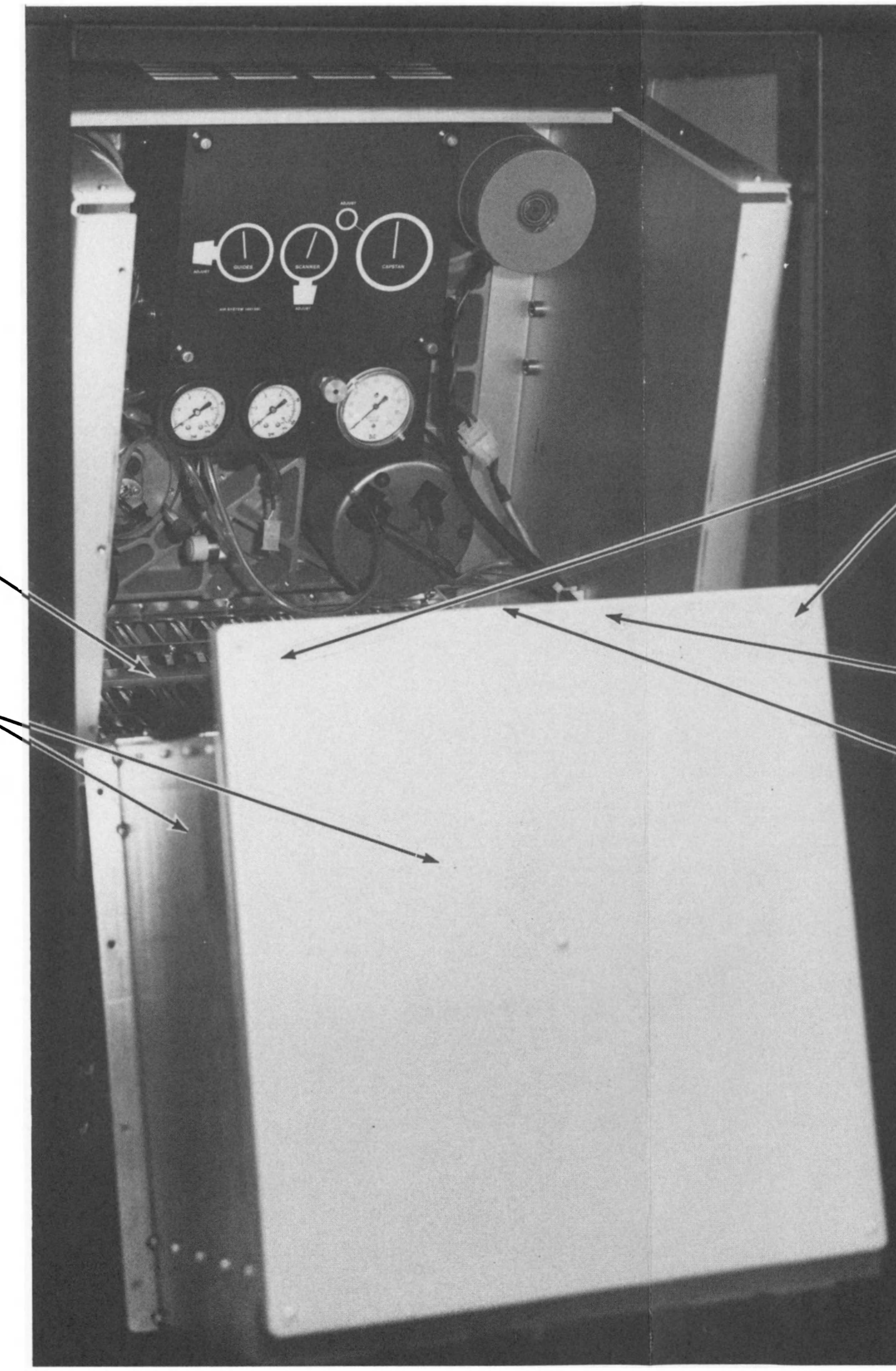


VPR-3 G-1B
SIGNAL SYSTEM
625



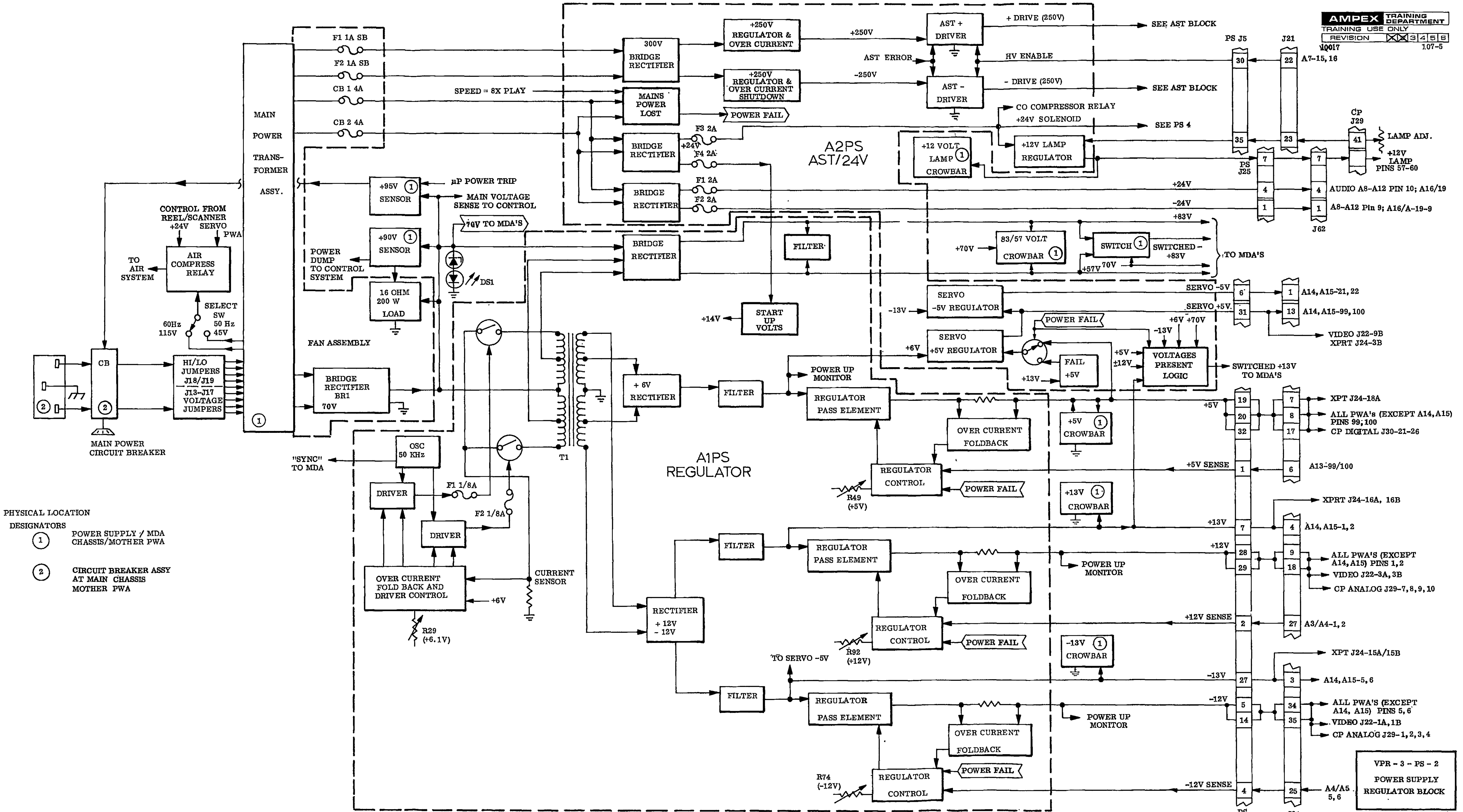
VPR-3
AIR SYSTEM BLOCK DIAGRAM



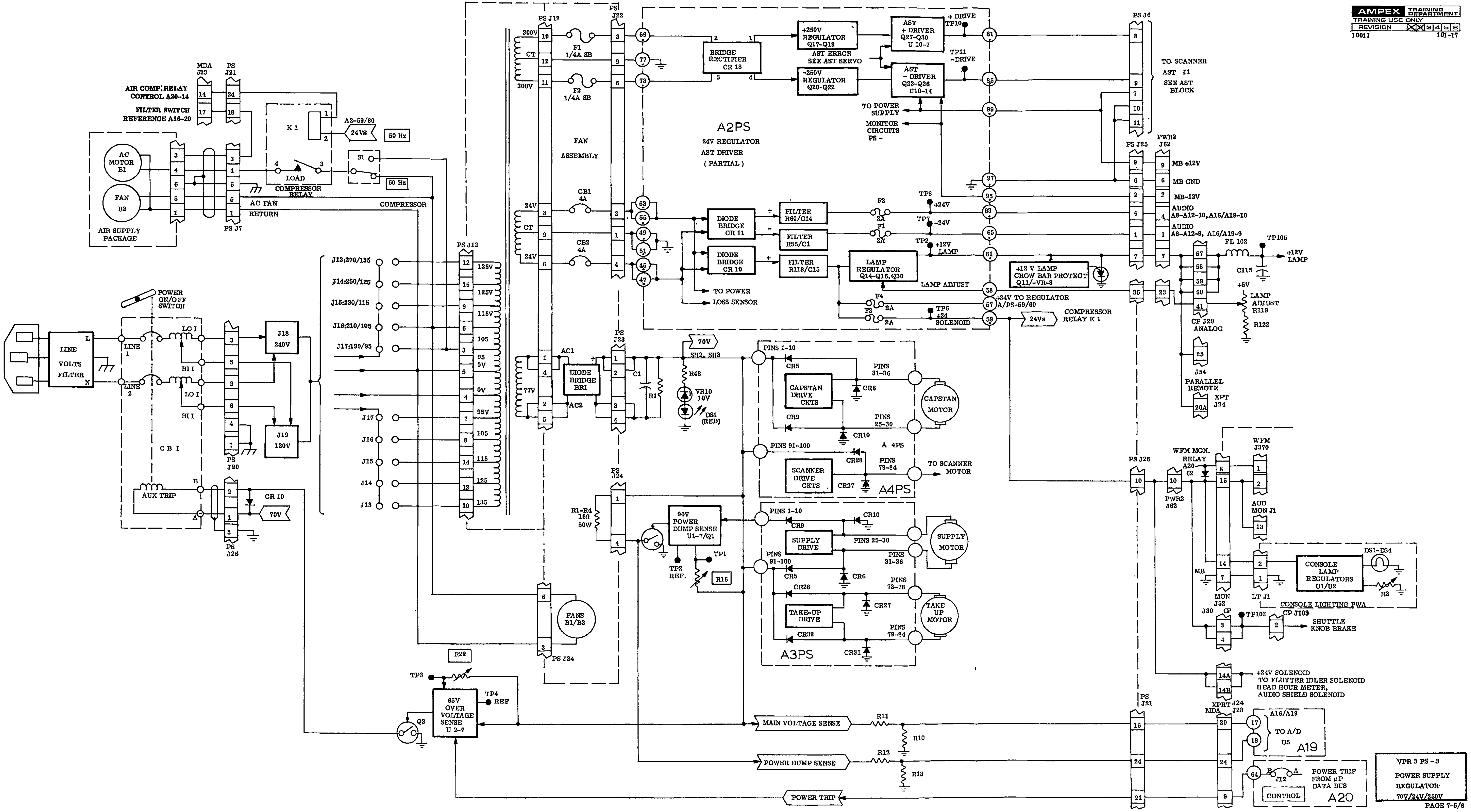


VPR-3 1/4

POWER SUPPLY COMPONENT LOCATION

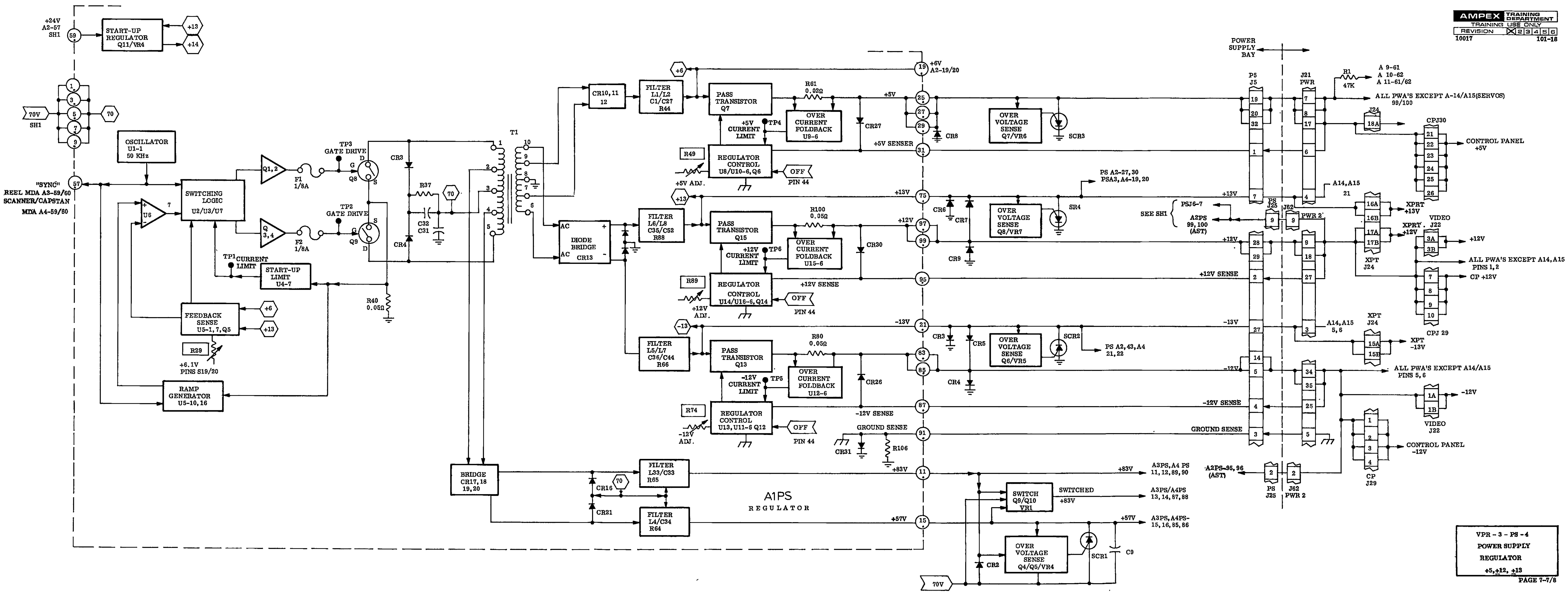

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 3 4 5 6
10017
107-5
F1 1A SB
F2 1A SB
CB 1 4A
CB 2 4A
MAIN POWER TRANS-FORMER ASSY.
300V BRIDGE RECTIFIER
+250V REGULATOR & OVER CURRENT
+250V
+250V REGULATOR & OVER CURRENT SHUTDOWN
-250V
AST + DRIVER
AST - DRIVER
AST ERROR
+ DRIVE (250V)
HV ENABLE
- DRIVE (250V)
SEE AST BLOCK
SEE AST BLOCK
SPEED = 8X PLAY
MAINS POWER LOST
POWER FAIL
CO COMPRESSOR RELAY
+24V SOLENOID
SEE PS 4
BRIDGE RECTIFIER
+24V
F3 2A
F4 2A
A2PS AST/24V
+12 VOLT LAMP CROWBAR
+12V LAMP REGULATOR
PS J5
J21
A7-15, 16
CP J29
LAMP ADJ.
+12V LAMP PINS 57-60
PS J25
J62
F1 2A
F2 2A
+24V
-24V
AUDIO A8-A12 PIN 10; A16/19
A8-A12 Pin 9; A16/A-19-9
µP POWER TRIP
+95V SENSOR
MAIN VOLTAGE SENSE TO CONTROL
CONTROL FROM REEL/SCANNER +24V SERVO PWA
AIR COMPRESS RELAY
TO AIR SYSTEM
70V TO MDA'S
+90V SENSOR
POWER DUMP TO CONTROL SYSTEM
16 OHM 200 W LOAD
DS1
BRIDGE RECTIFIER
FILTER
+83V
+70V
83/57 VOLT CROWBAR
SWITCH
SWITCHED - +83V
+57V
70V
TO MDA'S
SELECT SW
60Hz 115V
50 Hz 45V
START UP VOLTS
+14V
SERVO -5V REGULATOR
-13V
SERVO -5V
SERVO +5V
A14, A15-21, 22
A14, A15-99, 100
VIDEO J22-9B
XPRT J24-3B
POWER FAIL
SERVO +5V REGULATOR
+6V
-13V
+6V +70V
FAIL +5V
+5V
±12V
+13V
VOLTAGES PRESENT LOGIC
SWITCHED +13V TO MDA'S
FAN ASSEMBLY
CB
HI/LO JUMPERS J18/J19
J13-J17 VOLTAGE JUMPERS
BRIDGE RECTIFIER BR1
70V
MAIN POWER CIRCUIT BREAKER
+ 6V RECTIFIER
FILTER
POWER UP MONITOR
REGULATOR PASS ELEMENT
OVER CURRENT FOLDBACK
+5V CROWBAR
+5V
XPT J24-18A
ALL PWA's (EXCEPT A14, A15) PINS 99, 100
CP DIGITAL J30-21-26
+5V SENSE
A13-99/100
OSC 50 KHz
"SYNC" TO MDA
T1
A1PS REGULATOR
REGULATOR CONTROL
POWER FAIL
R49 (+5V)
DRIVER
F1 1/8A
F2 1/8A
DRIVER
+13V CROWBAR
XPRT J24-16A, 16B
+13V
A14, A15-1, 2
+12V
REGULATOR PASS ELEMENT
POWER UP MONITOR
ALL PWA'S (EXCEPT A14, A15) PINS 1, 2
VIDEO J22-3A, 3B
CP ANALOG J29-7, 8, 9, 10
OVER CURRENT FOLD BACK AND DRIVER CONTROL
CURRENT SENSOR
+6V
R29 (+6.1V)
OVER CURRENT FOLDBACK
RECTIFIER +12V -12V
REGULATOR CONTROL
+12V SENSE
A3/A4-1, 2
R92 (+12V)
POWER FAIL
-13V CROWBAR
TO SERVO -5V
XPT J24-15A/15B
-13V
A14, A15-5, 6
FILTER
FILTER
REGULATOR PASS ELEMENT
-12V
POWER UP MONITOR
ALL PWA'S (EXCEPT A14, A15) PINS 5, 6
VIDEO J22-1A, 1B
CP ANALOG J29-1, 2, 3, 4
OVER CURRENT FOLDBACK
R74 (-12V)
REGULATOR CONTROL
POWER FAIL
-12V SENSE
A4/A5 5, 6
PHYSICAL LOCATION DESIGNATORS
1 POWER SUPPLY / MDA CHASSIS/MOTHER PWA
2 CIRCUIT BREAKER ASSY AT MAIN CHASSIS MOTHER PWA
VPR - 3 - PS - 2
POWER SUPPLY REGULATOR BLOCK

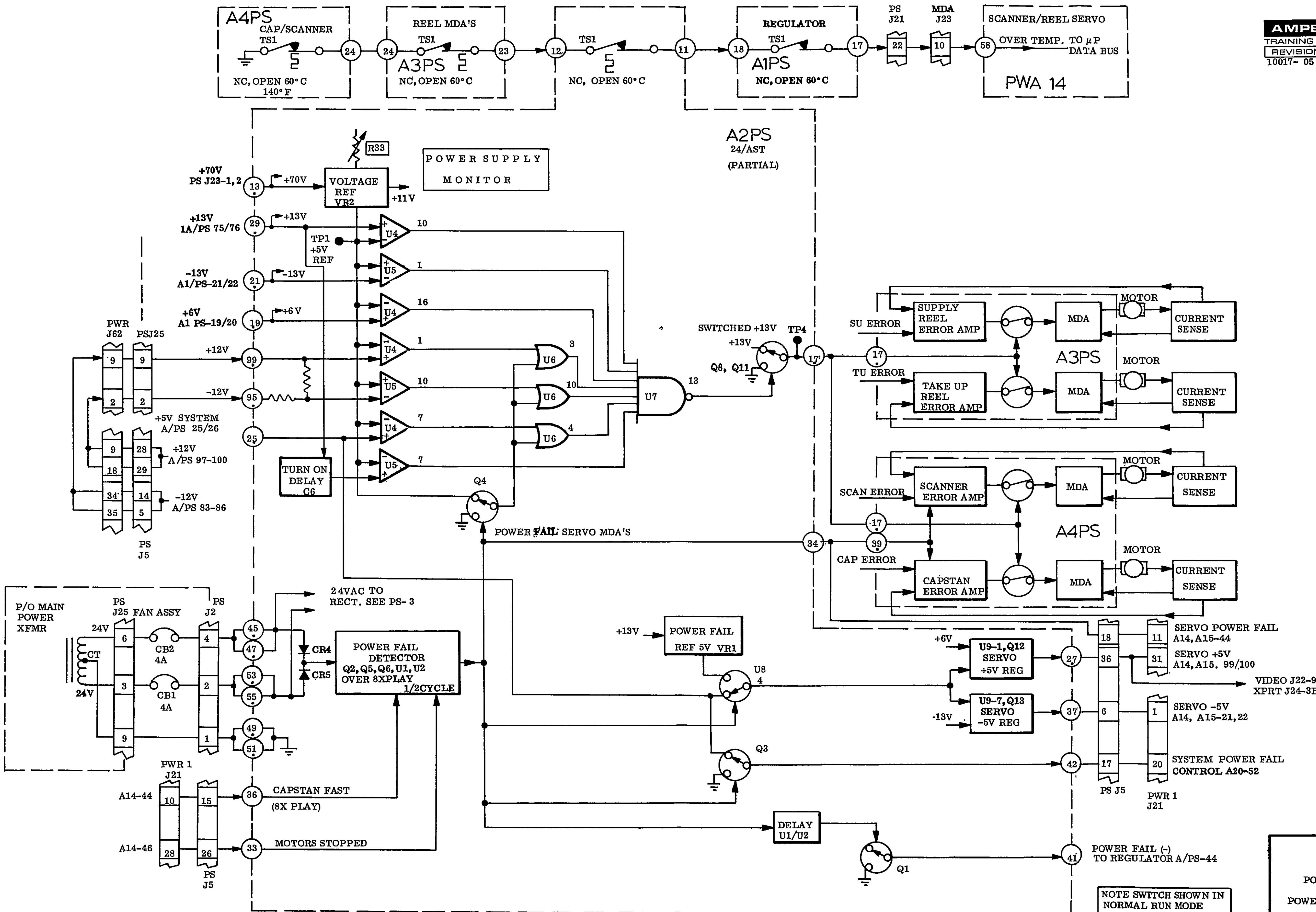
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 3 4 5 6
10017 101-17



VPR 3 PS - 3
POWER SUPPLY REGULATOR
70V/24V/250V

PAGE 7-5/6

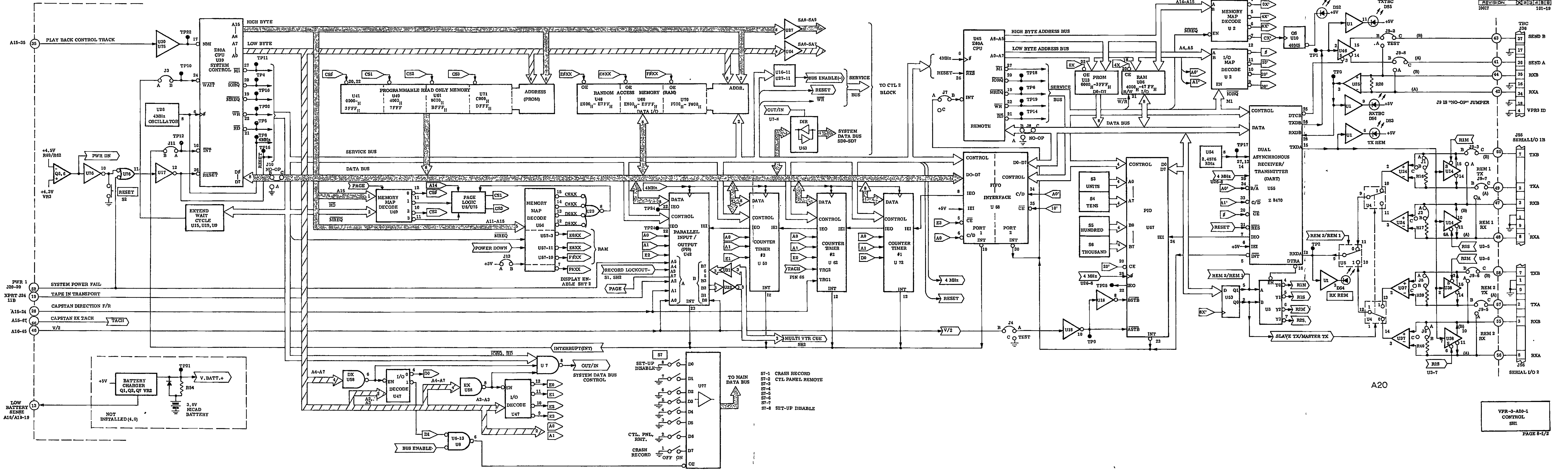

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
101-18
+24V A2-57 SH1
START-UP REGULATOR Q11/VR4
+13
+14
70V SH1
70
OSCILLATOR U1-1 50 KHz
"SYNC" REEL MDA A3-59/60 SCANNER/CAPSTAN MDA A4-59/60
SWITCHING LOGIC U2/U3/U7
U6
Q1, 2
Q 3, 4
F1 1/8A
F2 1/8A
TP3 GATE DRIVE
TP2 GATE DRIVE
Q8
Q9
CR3
CR4
R37
C32 C31
T1
TP1 CURRENT LIMIT
START-UP LIMIT U4-7
R40 0.05Ω
FEEDBACK SENSE U5-1, 7, Q5
+6
R29
+6.1V PINS S19/20
RAMP GENERATOR U5-10, 16
CR10, 11 12
FILTER L1/L2 C1/C27 R44
DIODE BRIDGE CR13
FILTER L6/L8 C35/C52 R88
FILTER L5/L7 C36/C44 R66
PASS TRANSISTOR Q7
R61 0.02Ω
OVER CURRENT FOLDBACK U9-6
+5V CURRENT LIMIT
TP4
R49
REGULATOR CONTROL U8/U10-6, Q6
OFF PIN 44
+5V ADJ.
PASS TRANSISTOR Q15
R100 0.05Ω
OVER CURRENT FOLDBACK U15-6
+12V CURRENT LIMIT
TP6
R89
REGULATOR CONTROL U14/U16-6, Q14
+12V ADJ.
+12V SENSE
-13
PASS TRANSISTOR Q13
R80 0.05Ω
OVER CURRENT FOLDBACK U12-6
-12V CURRENT LIMIT
TP5
R74
REGULATOR CONTROL U13, U11-6 Q12
-12V ADJ.
-12V SENSE
GROUND SENSE
CR31
R106
+6V A2-19/20
+5V
+5V SENSER
CR27
CR8
CR30
CR26
OVER VOLTAGE SENSE Q7/VR6
SCR3
+13V
PS A2-27, 30 PSA3, A4-19, 20
CR6
CR7
CR9
OVER VOLTAGE SENSE Q8/VR7
SR4
+12V
-13V
CR5
OVER VOLTAGE SENSE Q6/VR5
SCR2
PS A2, 43, A4 21, 22
-12V
BRIDGE CR17, 18 19, 20
CR16
CR21
FILTER L33/C33 R65
FILTER L4/C34 R64
A1PS
REGULATOR
+83V
+57V
A3PS, A4 PS 11, 12, 89, 90
SWITCH Q9/Q10 VR1
SWITCHED +83V
A3PS/A4PS 13, 14, 87, 88
A3PS, A4PS- 15, 16, 85, 86
OVER VOLTAGE SENSE Q4/Q5/VR4
SCR1
C9
CR2
70V
POWER SUPPLY BAY
P5 J5
J21 PWR
R1 47K
A 9-61 A 10-62 A 11-61/62
ALL PWA'S EXCEPT A-14/A15(SERVOS) 99/100
J24
CPJ30
CONTROL PANEL +5V
A14, A15 21
SEE SH1
PSJ6-7
A2PS 99, 100 (AST)
PS J25
J62
PWR 2
XPRT +13V
XPRT +12V
VIDEO J22
XPT J24
ALL PWA'S EXCEPT A14, A15 PINS 1, 2
CP +12V
CPJ 29
A14, A15 5, 6
XPT -13V
ALL PWA'S EXCEPT A14/A15 PINS 5, 6
VIDEO J22
CONTROL PANEL -12V
CP J29
A2PS-95, 96 (AST)
PS J25
J62 PWR 2
VPR-3-PS-4
POWER SUPPLY
REGULATOR
+5, ±12, ±13
PAGE 7-7/8



VPR-3 -PS-5

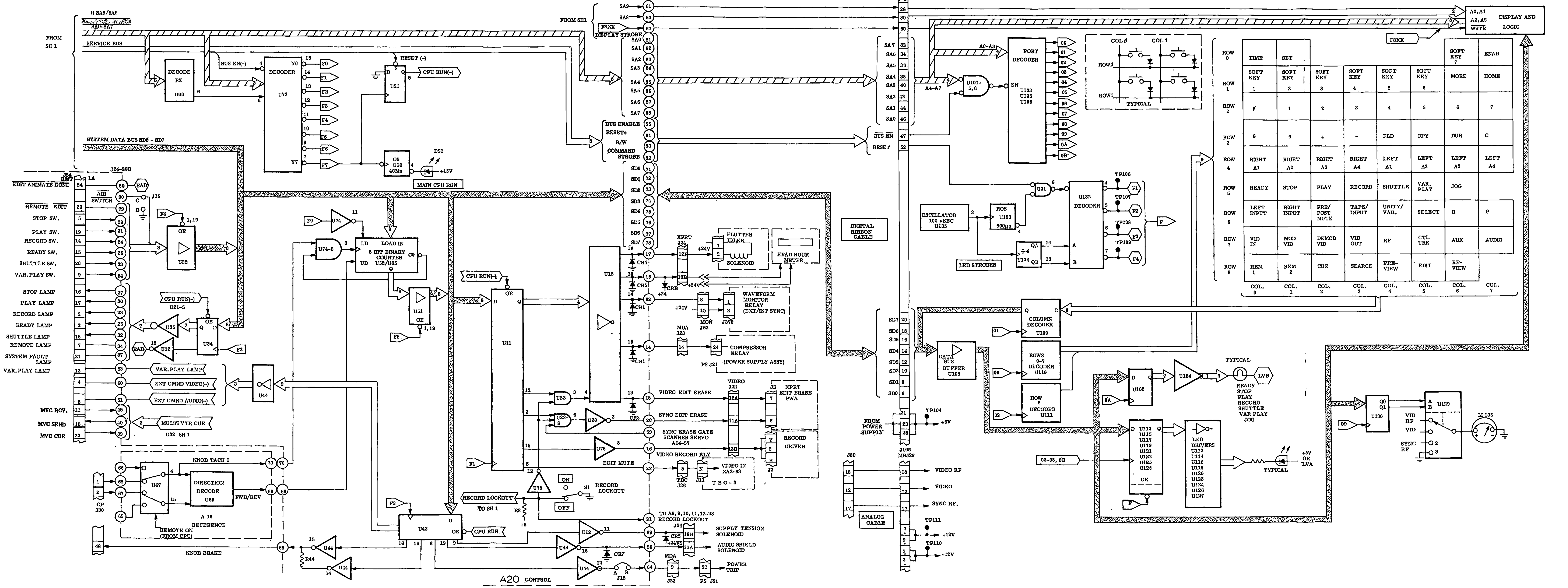
POWER SUPPLY

POWER FAIL SYSTEM

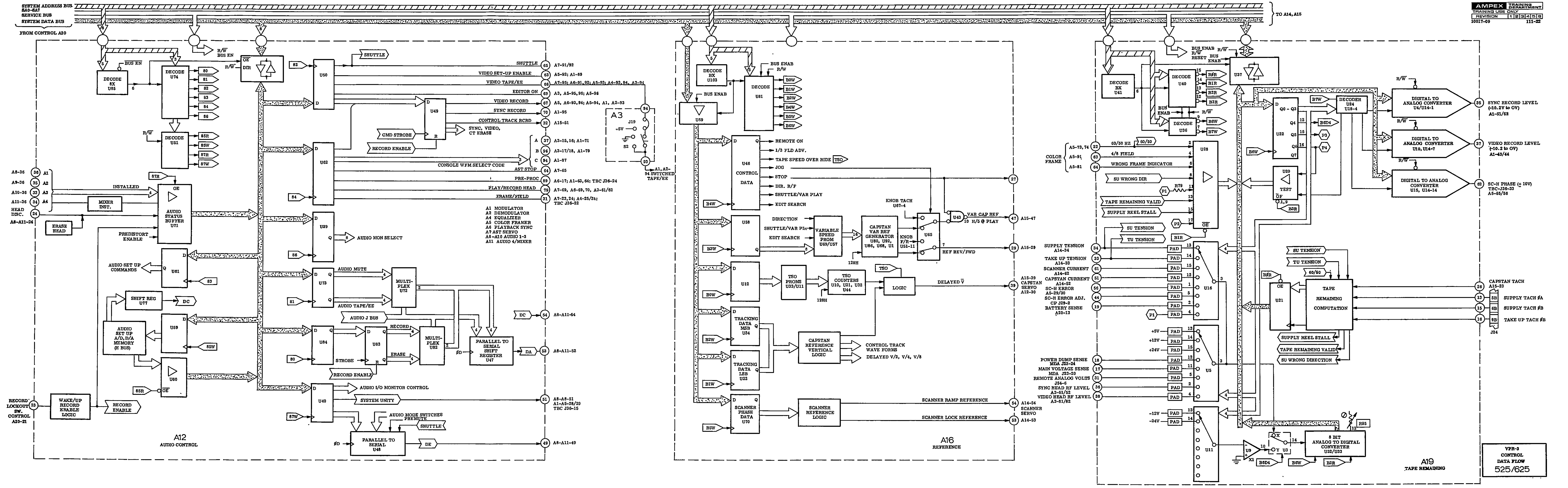


VPR-3-A20-1
CONTROL
SH1

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION
10017 '101-20'



VPR-3-A20-2
CONTROL LOGIC
BLOCK
SH2


SYSTEM ADDRESS BUS SA0-SA7
SERVICE BUS
SYSTEM DATA BUS
FROM CONTROL A20
TO A14, A15
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
A12
AUDIO CONTROL
A16
REFERENCE
A19
TAPE REMAINING
A3
DECODE 8X U85
DECODE U74
DECODE U51
AUDIO STATUS BUFFER U71
MIXER INST.
ERASE HEAD
SHIFT REG U77
AUDIO SET UP A/D, D/A MEMORY (H BUS)
WAKE/UP RECORD ENABLE LOGIC
RECORD ENABLE
PARALLEL TO SERIAL U48
PARALLEL TO SERIAL SHIFT REGISTER U47
MULTI-PLEX U72
MULTI-PLEX U82
SHUTTLE
VIDEO SET-UP ENABLE
VIDEO TAPE/EE
EDITOR ON
VIDEO RECORD
SYNC RECORD
CONTROL TRACK RCRD
CONSOLE WFM SELECT CODE
AST STOP
PRE-PROC
PLAY/RECORD HEAD
FRAME/FIELD
AUDIO MON SELECT
AUDIO MUTE
AUDIO TAPE/EE
AUDIO J BUS
AUDIO I/O MONITOR CONTROL
SYSTEM UNITY
AUDIO MODE SWITCHES
A1 MODULATOR
A2 DEMODULATOR
A4 EQUALIZER
A5 COLOR FRAMER
A6 PLAYBACK SYNC
A7 AST SERVO
A8-A10 AUDIO 1-3
A11 AUDIO 4/MIXER
DECODE 8X U103
DECODE U81
CONTROL DATA U46
REMOTE ON
1/3 FLD ADV.
TAPE SPEED OVER RIDE
JOG
STOP
DIR. R/F
SHUTTLE/VAR PLAY
EDIT SEARCH
VARIABLE SPEED PROM U69/U57
CAPSTAN VAR REF GENERATOR U80, U92, U86, U68, U1
VAR CAP REF
REF REV/FWD
TSO PROMS U33/U11
TSO COUNTERS U10, U21, U32 U44
LOGIC
DELAYED V
TRACKING DATA MSB U34
TRACKING DATA LSB U22
CAPSTAN REFERENCE VERTICAL LOGIC
CONTROL TRACK WAVE FORMS
DELAYED V/2, V/4, V/8
SCANNER PHASE DATA U70
SCANNER REFERENCE LOGIC
SCANNER RAMP REFERENCE
SCANNER LOCK REFERENCE
DECODE 8X U41
DECODE U40
DECODE U36
DECODER U24 U18-4
DIGITAL TO ANALOG CONVERTER U4/U14-1
DIGITAL TO ANALOG CONVERTER U10, U14-7
DIGITAL TO ANALOG CONVERTER U15, U14-14
SYNC RECORD LEVEL
VIDEO RECORD LEVEL
SC-H PHASE
COLOR FRAME
WRONG FRAME INDICATOR
SU WRONG DIR
TAPE REMAINING VALID
SUPPLY REEL STALL
SU TENSION
TU TENSION
SUPPLY TENSION
TAKE UP TENSION
SCANNER CURRENT
CAPSTAN CURRENT
SC-H ERROR
SC-H ERROR ADJ.
BATTERY SENSE
POWER DUMP SENSE
MAIN VOLTAGE SENSE
REMOTE ANALOG VOLTS
SYNC HEAD RF LEVEL
VIDEO HEAD RF LEVEL
TAPE REMAINING COMPUTATION
CAPSTAN TACH
SUPPLY TACH ØA
SUPPLY TACH ØB
TAKE UP TACH ØB
SU WRONG DIRECTION
8 BIT ANALOG TO DIGITAL CONVERTER U32/U33
VPR-3 CONTROL DATA FLOW 525/625

VPR-3 SYSTEM CONTROL

1. The Transport Control PWA 20 uses a Z80A microprocessor (the CPU), with the control program stored in three 16k x 8 EPROMS, U41, U49, U61, and U71. Data storage uses three 2k x 8 Random Access Memories (RAM), U48, U60, and U70. The 26 x 256 matrix display on the control panel is treated as a write only memory. The memory map (all addresses are in HEXadecimal format):

HEX ADDRESS	DEVICE SELECTED AND ADDRESS DECODER
0000-3FFF	First 16k of program in PROM U41, decoded by U69.
4000-7FFF	Second 16k of program in PROM U49, decoded by U69.
8000-BFFF	Third 16k of program in PROM U61, decoded by U69.
C000-DFFF	Last 8k of program in PROM U71, decoded by U56.
E000-E7FF	First 2k of data storage in RAM U48, decoded by U56.
E800-EFFF	Second 2k of data storage in RAM U60, decoded by U56.
F000-F7FF	Third 2k of data storage in RAM U70, decoded by U56.
F800-FFFF	Control Panel 26 x 256 display.

1.1 The INPUT/OUTPUT (I/O) addressing mode is used by the CPU to communicate with peripheral devices. The same address lines from the CPU are used. CPU MREQ line is low when addressing memory; IORQ is low and M1 high if a peripheral is addressed. These peripherals include:

1. Input ports on the Control PWA that look at switches, sensors, etc.,and output ports that drive relays, lamps, etc.
2. Counter/timer chips on the Control PWA.
3. The parallel input/output controller on the Control PWA.
4. The First In/First Out (FIFO) on the Control PWA that provides an interface with the Z80A CPU that handles the serial remote lines.
5. The Control panel switches and lamps. Their status is checked once every vertical interval.
6. Audio Control PWA 12. The system data bus is decoded on Audio Control for all communications with the video signal system. Data, including set-up information, for the audio boards and optional mixer are converted into a sixteen bit serial word for communication with the Audio PWA's.
7. Reel and Scanner Servo PWA 14.
8. Control Track and Capstan Servo PWA 15.
9. Reference PWA 16 and Tape Remaining PWA 19.
10. Time Code Reader/Generator and Character Generator PWA 18.

2. TRANSPORT CONTROL PWA 20 system data bus buffer is U63. The address buffer is U64. Five of the I/O (Input/Output) ports on the Control PWA form a daisy chain interrupt bus. Interrupt priority is determined by the interrupt logic lines IEI (Interrupt Enable In) and IEO (Interrupt Enable Out). If the IEI line is high on a Z80 peripheral, that device has priority. The interrupting device will pulll its IEO line low, to inhibit the next device in the daisy chain.

The CPU acknowledges the interrupt by pulling M1 and IORQ outputs low, allowing the interrupting device to place a unique interrupt vector (address) on the system data bus, selecting the starting address of a particular interrupt routine. After the CPU has serviced the routine, an RETI instruction from the CPU resets the interrupting device, allowing the next highest priority device to request service. The interrupt priority is:

1. First In/First Out (FIFO) Z8083 U68, which interfaces between control CPU U39 and Serial Data Control CPU U45.
2. Counter Timer #1, U72, Edit Timing.
3. Counter Timer #2, U62, which generates an interrupt when the capstan reverses direction, and also when Capstan tach has been divided down to frame rate (similar to the ADD 1 pulse in the VPR-2). At play speed, this will occur at a frame rate. The Non-maskable Interrupt (NMI) input to the CPU establishes the phasing of this divider so that this interrupt has a specific timing relationship to the reference frame, since this pulse updates the tape timers and time code reader.
4. Counter Timer #3, U50 Edit Timing.
5. The Z8420 Parallel Input/Output Controller (PIO) U42 generates an interrupt at a vertical rate. On Port A: **D0**-V/2; **D1**-capstan direction; **D2**-tape in transport sensor; **D3**-Record Lockout Switch; **D5**-System Power Fail. On Port B: **D0**-V/2; **D1**-MVC Cue; **D2**-MVC Send; **D3**-MVC Receive; **D5**-MVC Receive (in); **D6**-MVC Send (in); **D7**-MVC Cue (in).

2.1 The Address decoders for these ports are U58, U59, and U47. The I/O adresses are:

HEX ADD.	FUNCTION/IC
D0-D3	Counter Timer U72
E0-E3	Counter Timer U62
E4-E7	Counter Timer U50
E8-EB	Parallel Input/Output (PIO) U42
EC-EF	First In/First Out (FIFO) U58

2.2 The Decoders for the following I/O ports on Control PWA 20 are U-66/U73.

ADDRESS	LATCH/BUFFER & FUNCTION
F0	U65/U52. Output Port. Load shuttle knob tach counter with data bus information.
F1	Output Latch U 11. **D0**-flutter idler solenoid; **D1**-compressor relay; **D1**-video record relay; **D3**-video edit erase; **D4**-waveform monitor relay; **D5**-edit mute; **D6**-sync head edit erase; **D7**-head hour meter.
F2	U34/U35. Parallel remote outputs. **D0**-stop lamp; **D1**-play lamp; **D2**-record lamp; **D3**- ready lamp; **D4**-shuttle lamp; **D5**-remote lamp; **D6**-system fault lamp.
F3	U43/U44. **D0**-audio shield solenoid; **D1, D2**-knob brake; **D3**-variable play lamp; **D4**-power trip (disconnected by J12); **D5**-external command video; **D6**-external command audio.
F4	U22. Parallel remote inputs. **D0**-stop; **D1**-play; **D2**-record; **D3**-ready; **D4**-shuttle; **D7**-variable play.
F5	U51. Write contents of knob tach counter to CPU data bus.
F6	Control ready via pin 65 to time code reader/generator.
F7	U10. Main CPU run lamp.

CONTROLLING THE VPR-80 AND VPR-3 VIA THE SERIAL INTERFACE

1. Transmission and receiving are by 4-wire full duplex, i.e., a dedicated pair of wires for each direction. Communications is bit-serial at 38.4K baud, one start bit, 8 data bits, one (even)[1] parity bit, and one stop bit (mark) per character sent. The voltage levels are described in the proposed American Standard PH22.207M, to be found in the appendix of the Sept. 1982 issue of the Journal of the Society of Motion Picture and Television Engineers.

2. When the VTR wakes up it is in the "idle" mode. (see RP113, same issue, p. 894). It will not communicate in this mode, and will respond only by sending it a "break", consisting of spacing for 17 to 20 bit periods followed by a minimum of two bit periods of marking.

   At this time the "idle" mode will be exited and the "active" mode entered. In this mode the VTR will respond to a two-byte address established by the operator from the VPR-80 keyboard or with a card-edge switch on the VPR-3. While the operator establishes a simple decimal number, this number is translated into a two-byte binary address as follows:

DECIMAL	
1	80A2 (hex)
2	80A4
3	80A6
-	----
47	80FE
48	8180
---	---
---	---
---	---
	FFFE

   Note that the most significant bit of both bytes is always one. The most significant byte is sent first.

   When the VTR receives the first byte of this address it takes one step away from the "active" state and waits for the second byte. If the second byte does not match its own, or does not arrive within 3 TV frame periods, it will revert to the "idle" state. If the second byte does match, the VTR will transit to the "select" state.

   The VTR's are currently using "user defined communications" as described in RP-113, hence the next character transmitted should be "escape" (ESC)

or 03 hex. The VTR will respond by replying with an (ACK) character, (04 hex) and enter the "Ampex Select" state. At this point communications have been established. Commands may now be sent to the VTR
NOTE: The definition of ACK, NAK, etc., are as per the referenced documents, and may differ from other definitions, i.e., ASCII.

3. Commands are of two types - those which direct the machine to do something, and those which request the machine to reply with some specified data about itself. In the first case, the VTR will respond to the command with an (ACK) if the command is received properly, or with a (NAK) (05 hex) and an exit to the idle state, if not. In the second case, the VTR again gives (NAK) and exit to idle if there is a communication error, or responds with (STX) (02 hex), followed by a byte count of the requested message(s) (not counting the (STX) or the byte count or the check sum at the end), followed by an echo of the command which elicited the data, followed by the requested data, and terminated by a check-sum byte. The byte count includes the echo.

   The check sum is the 2's complement of the sum (without carry) of the data, including the byte count and echo bytes. Each response is prefaced with the command echo.

4. Once communications have been established, commands from the controller to the VTR are in this form:

   (STX)
   Byte count of the message
   The message(variable length)
   The Checksum
   Multiple commands or subcommands may be sent in one message. In this case:

   (STX)
   Byte count of the entire message
   Command 1
   Command 2
   Command 3
   Checksum

5. Following, in ascending numeric order, are global commands which apply to all sorts of devices, not just video recorders. (numbers are base 16 (hex))

01:	Send your status.	1 byte
02:	Send extended status	1 byte

03: Defer the following commands: N bytes
Byte 0-3: Time-line time code number at which the command(s) are to be executed.
Byte 4: Byte count of the commands to be deferred.
Bytes 5-N: The commands to be deferred..

04: Cue to the earliest event on the time line. For devices requiring pre-roll, the actual cue or "park" position should be calculated by the controlled device. (1 byte)

05: Stop incrementing the time line (1 byte)

06: Clear the time line buffers (1 byte)
All events associated with the time line are cleared.

07: Load and begin incrementing the time line (5 bytes)
07 + 4 bytes of BCD time code

08-25 Not involved in VPR-80 or VPR-3

26: Treat the following as a tape transport sub-command (1 byte)

Sub-commands have the following format:

Hex 26: The sub-command identifier
Byte count The sub-command count
Sub-command

NOTE: There is no separate sub-command checksum. The sub-commands are listed below in ascending order, again in hex.

01 Ready Switch (2 bytes)
01 + Zero = off, 1 = on

02 EE/Tape switch (2 bytes)
02 + Zero = Tape, 1 = EE

03 Color Framer (2 bytes)
03 + Zero = off, 1 = on

04 Longitudinal time code (2 bytes)
04 + zero = off, 1 = on

05 Vertical interval time code
05 + zero= off, 1=on
NOTE: The VPR-80 does not support VITC.

06 Edit mode (2 bytes)
06 + zero = off, 1 = insert, 2 = assemble, 3= rehearse, 4 = crash record. Establish edit mode several seconds before edit event time to allow scanner to re-phase.

07 Record enable (2 bytes)
07 + Bit 0 = 1 - Video rec. enable
Bit 1 = 1 - Audio one enable
Bit 2 = 1 - Audio two enable
Bit 3 = 1 - Audio three enable
Bit 4 = 1 - Audio four enable
Bit 7 = 1 - Time code record
NOTE: For any channel to record it must be both enabled beforehand and invoked in the entry command, See 17, next page.

08 Time code mode (2 bytes)
08+Zero = Hold, 1 = run now, 2 = jam slave

09 Set Speed (3 bytes)
09 + two bytes of signed magnitude, most significant first.
Range depends on function being controlled, but never exceeds 1FF
In the VPR-80, the least significant bit is ignored, but should be set high. See appendix A.

OA Preset the time code generator (5 bytes)
OA + 4 bytes of BCD time code

OB Load user bits into the time code gen. (5 bytes)
OB + 4 bytes of binary, MS byte first

OC Stop (1 byte)

OD Play (1 byte)

OE Roll (Play and synchronize to ext. ref) (1 byte)

OF Tape speed over-ride (3 bytes)
OF + 2 bytes of magnitude (see 09, above)
±1FF = ±15% speed change from nominal

10 Slow play (3 bytes)
10 + 2 bytes of magnitude (see 09, above)
Zero = Stop, + 1FF = 3 times play speed
Reverse play not implemented in the VPR-80
See appendix A.

11 Shuttle (3 bytes)
11 + 2 bytes of magnitude (see 09, above)
See appendix A.

12 Set pre-roll duration (5 bytes)
12 + 4 bytes of time code
Due to complications created by slow motion speeds and editing constraints, the transport is responsible for determining its own

"park" position. This duration is meant as a real time roll duration in front of deferred events. The controller must start the time line earlier than event minus pre-roll. Pre-roll must be non-zero for edit record.

13 Set sync point (5 bytes)
13 + 4 bytes of time code
This sets a point of synchronism for the cue command.

14 Set control point (7 bytes)
14 + 4 bytes time code + 2 bytes of play speed magnitude. This marks the point of synchronism for a non-standard play speed.

15 Cue (one byte). Causes transport to go to a "park" point which is pre-roll in front of the current sync or control point

16 Search (5 bytes)
16 + 4 bytes time code
Causes transport to move to the specified time code location, ignoring pre-roll

17 Entry (2 bytes)
17 + same format as in 07 above
Causes recording to commence on the specified channel(s). The corresponding record enables must have been previously set.

18 Exit (2 bytes)
Same as above, but exits record. It is prudent to clear record enables after the last record exit.

19 Not used on VPR-80 or VPR-3.

1A Send the ready status (one byte)

1B Send the tape/EE status (one byte)

1C Send the color framer status (one byte)

1D Send the longitudinal time code status (one byte)

1E Send vert. interval time code status (one byte)
(Not used in VPR-80)

1F Send editor mode (one byte)

20 Send record enable status (one byte)

21	Send the time code generator mode	(1 byte)
22	Send the transport speed setting	(1 byte)
23	Send the contents of the time code reader	(1 byte)
24	Send the user bits from the time code reader	(1 byte)
25	Forward jog (one byte). Advance one frame	(1 byte)
26	Reverse jog (one byte). Go back one frame	(1 byte)
27	Set accuracy window 27 + one byte = Zero thru OA Normally set to zero for time code editing. May be widened to as much as 10 frames. Non-zero values may be used for rough-cut editing or for editing with the tape timer.	(2 bytes)
28	Set tape timer 28 + 4 bytes time code	(5 bytes)

6. VTR response to commands which elicit data:

If the command is garbled, the VTR will send (NAK) and exit to idle mode, otherwise (STX) plus byte count, plus one or more of the following replies, and terminated by a checksum. These commands should not be deferred.

Send reply: status 7 bytes 01 (command echo) plus:
4 bytes of time code (current position)
+ one byte as follows:

Bit 0: 1 = NTSC, 0 = PAL
Bit 1: 1 = Drop frame, 0 = non-drop frame
Bit 2: 1 = Time line running, 0 = time line stopped
Bit 3: 1 = Deferred buffer full, 0 = not full
Bit 4: 1 = Current event executing
Bit 7: 1 = Error, 0 = no error

+ Another Byte as Follows:

00 Stopped
01 Stopping
02 Playing
03 Tape speed over-ride on
04 Shuttle mode
05 Fast forward

06 Rewind
07 Synchronizing
08 Source sync roll
09 Master sync roll
0A Master edit period
0B Record
0C Cueing
0D Cued (parked)
0E Searching
0F search complete
10 Executing an event
11-12 Not used at this time
13 Slow play
14 Power not on
15 Not in remote mode

Send extended status 5 bytes: 02 plus:

One byte - machine type no. (3 for transports)
Two bytes - Machine ID (0008 hex for VPR-80, 0003 for VPR-3)
One byte extended status as follows:

0 = No error
1 = Communications parity error
2 = Communications checksum error
3 = Communications error, other
4 = Command unknown
5 = Bad command arguments
6 = Command currently impossible
7 = Machine not configured to do command
8 = Machine not (ever) capable of command
9 = Time line entry data bad

In the following, note that transport sub-command identifier <u>and</u> the sub-command are echoed.

Send Ready status, 3 bytes: 26 + 1A + 0 = off, 1 = on

Send Tape/EE status, 3 bytes: 26 + 1B + 0 = tape, 1 = EE

Send Color framer status, 3 bytes: 26 + 1C + 0 = off, 1 = on

Send Longitudinal time code status,3 bytes: 26 + 1D + 0 = off, 1 = ON

Send vertical interval time code status, 3 bytes 26 + 1E + 0 = off, 1 = on
(Not used in VPR-80)

Send Editor mode, 3 bytes: 26 + 1F plus

0 = off
1 = insert
2 = assemble
3 = rehearse

Send channel enables, 3 bytes: 26 + 20 +

Bit 0 = 1, Video enabled
Bit 1 = 1, Audio 1 enabled
Bit 2 = 1, Audio 2 enabled
Bit 3 = 1, Audio 3 enabled
Bit 4 = 1, Audio 4 enabled
Bit 7 = 1, Time code enabled

Send time generator code mode, 3 bytes: 26 + 21 +

0 = Holding
1 = Running
2 = Jam slave mode

Send speed, 4 bytes: 26 + 22 + 2 bytes of magnitude

Send time code, 6 bytes: 26 + 23 + 4 bytes of time code.

Send user bits, 6 bytes: 26 + 24 + 4 bytes of user bits.

7. NOTE: Time code is always sent most significant byte first. The most significant nibble is tens, and least significant is units.

In a typical implementation, status and extended status are requested on alternate frames. It is one task of the controller to monitor error conditions, as the VPR-80 never speaks unless spoken to.

Note 1: While the SMPTE document specifies even parity, Ampex, Sony, and Grass Valley use odd parity, in which the number of ones in the data and including the parity bit itself is an odd number.

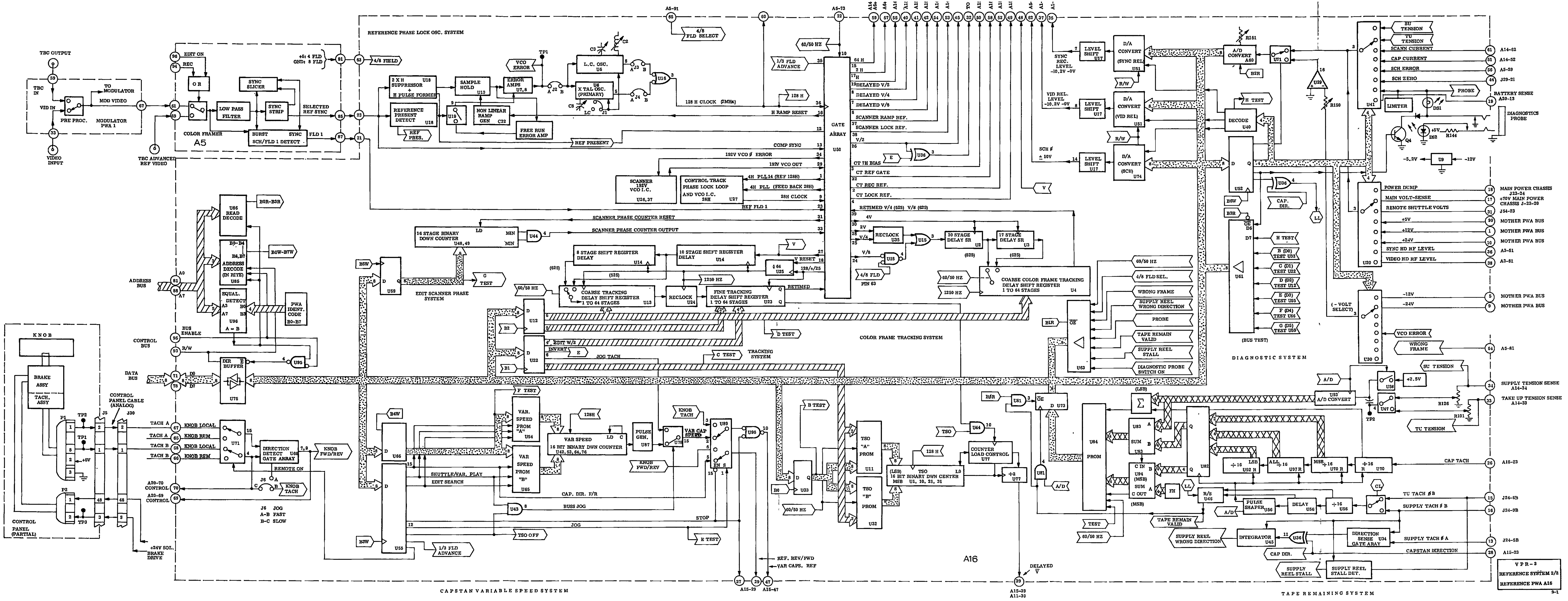
ESB:wc

APPENDIX A

In tape speed override mode, -511 produces a tape speed 15% slow, zero produces normal speed and +511 produces 15% fast.

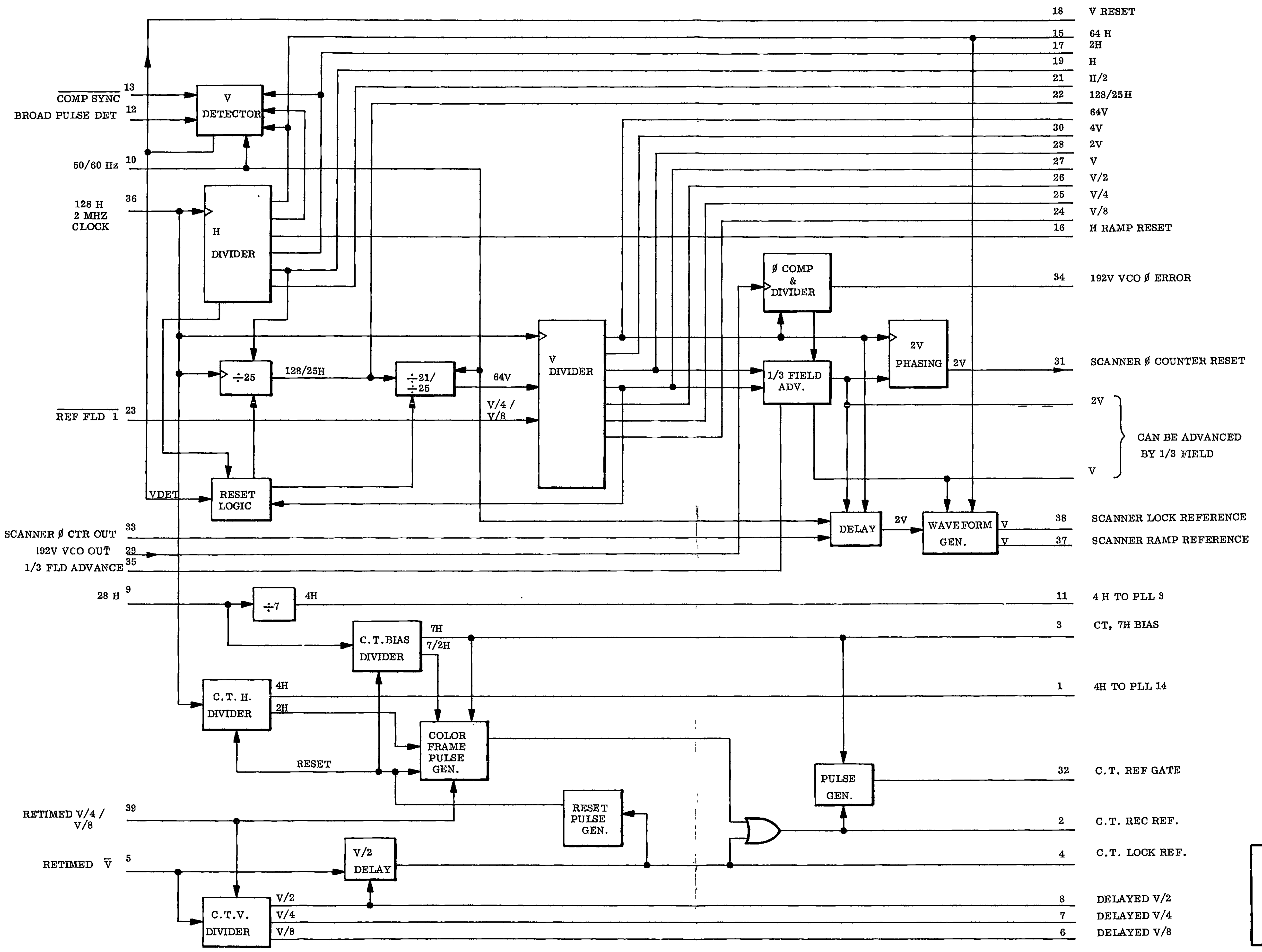
In variable play, +511 produces 3 times normal fast motion, zero produces stop, and in the VPR-3, any number less than minus 170 (512/3) produces reverse motion at play speed. The VPR-80 does not support reverse play, and its fast motion is limited at +1.5 play speed.

In shuttle, positive numbers produce forward motion and negative numbers produce reverse motion. Numbers in the range ±384 produce speeds up to 10 times play speed. Numbers in the range +385 to +510 and -385 to -510 cause speed from 10 times play to 30 times play. -511 or +511 produce maximum shuttle speed, whatever it might be.

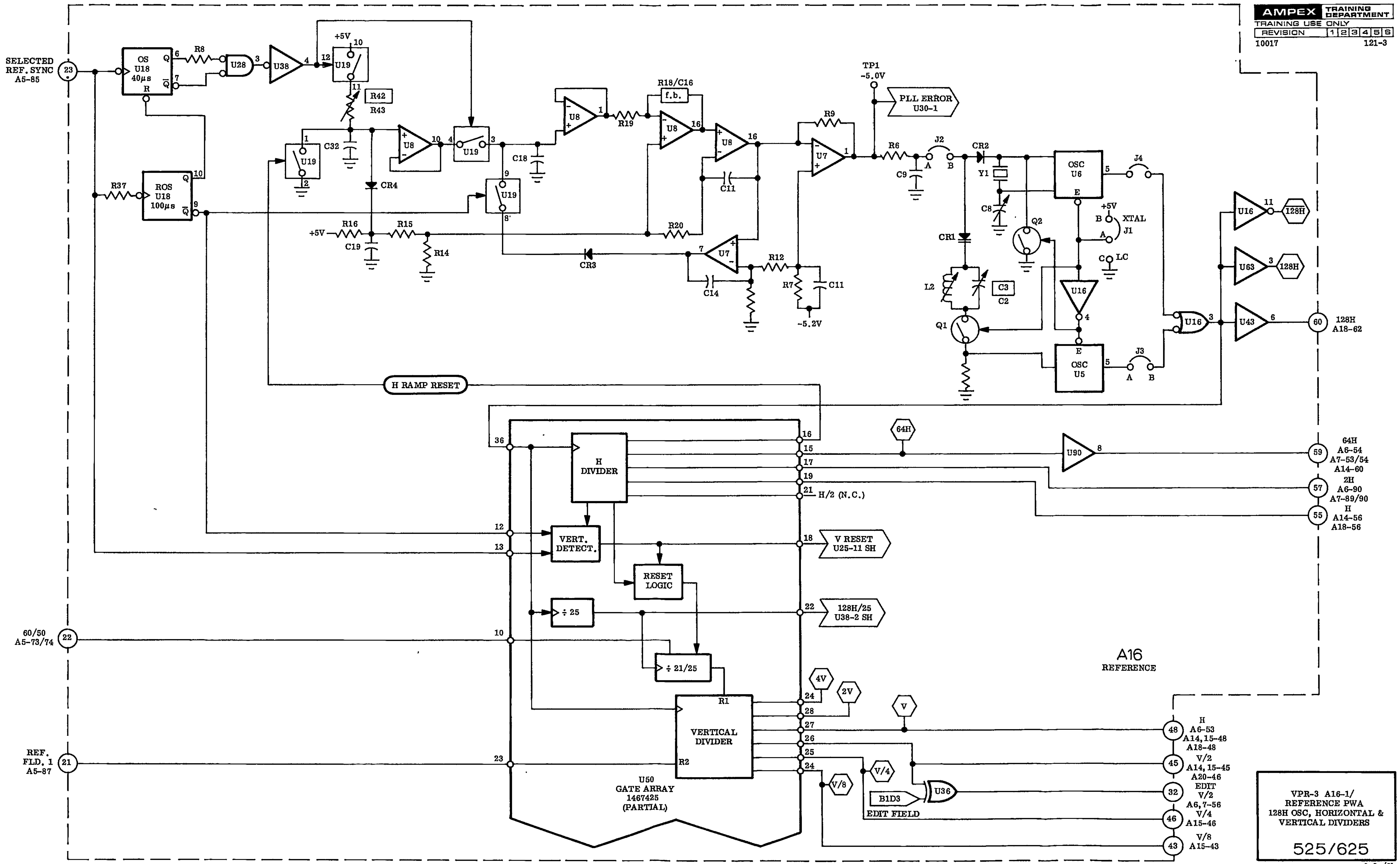


VPR-3
REFERENCE SYSTEM 2/2
REFERENCE PWA A16

9-1



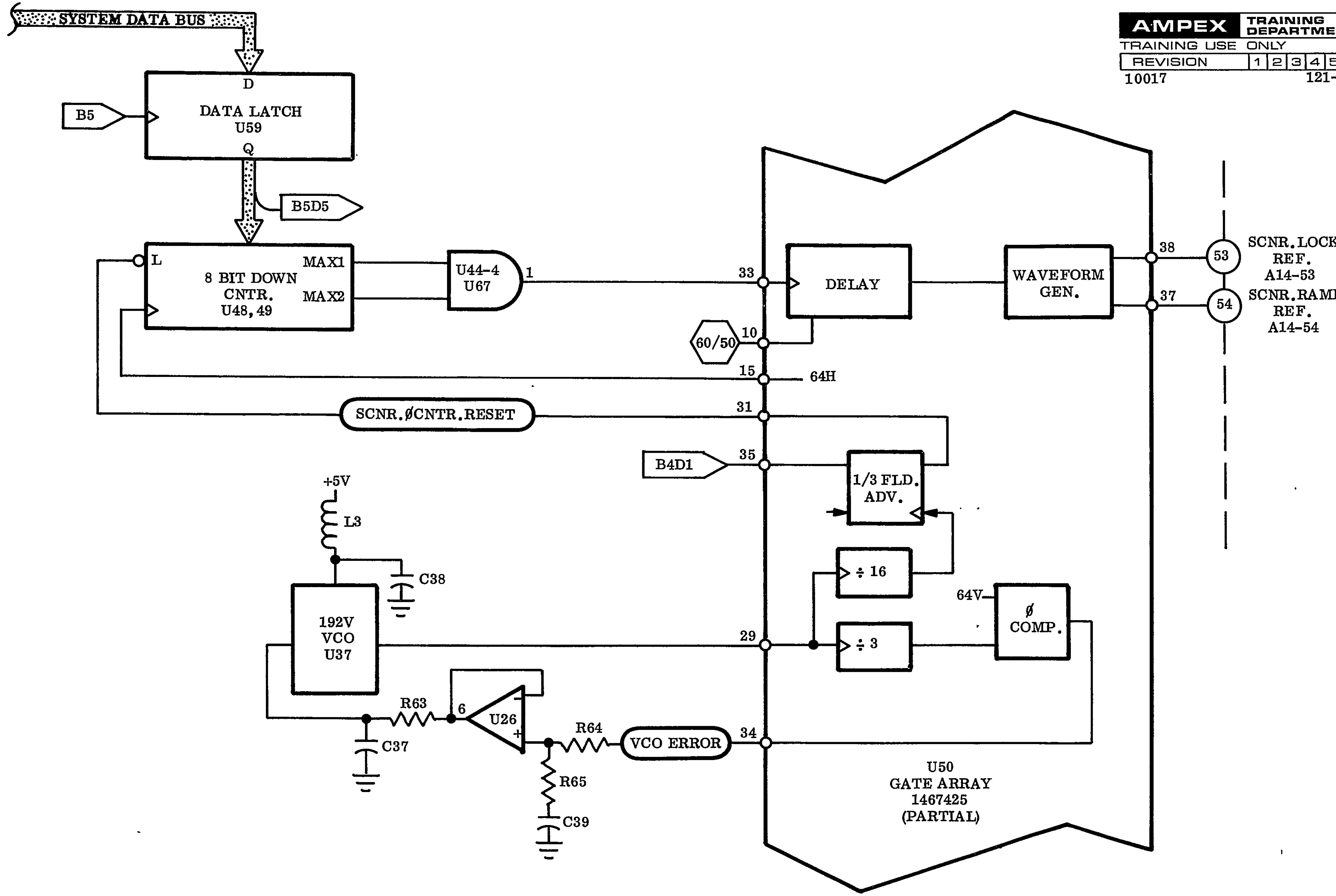
VPR-3
REFERENCE GENERATOR
GATE ARRAY BLOCK DIAGRAM
P/N 1467425-01 (HC 12608)



VPR-3 A16-1/
REFERENCE PWA
128H OSC, HORIZONTAL &
VERTICAL DIVIDERS

525/625

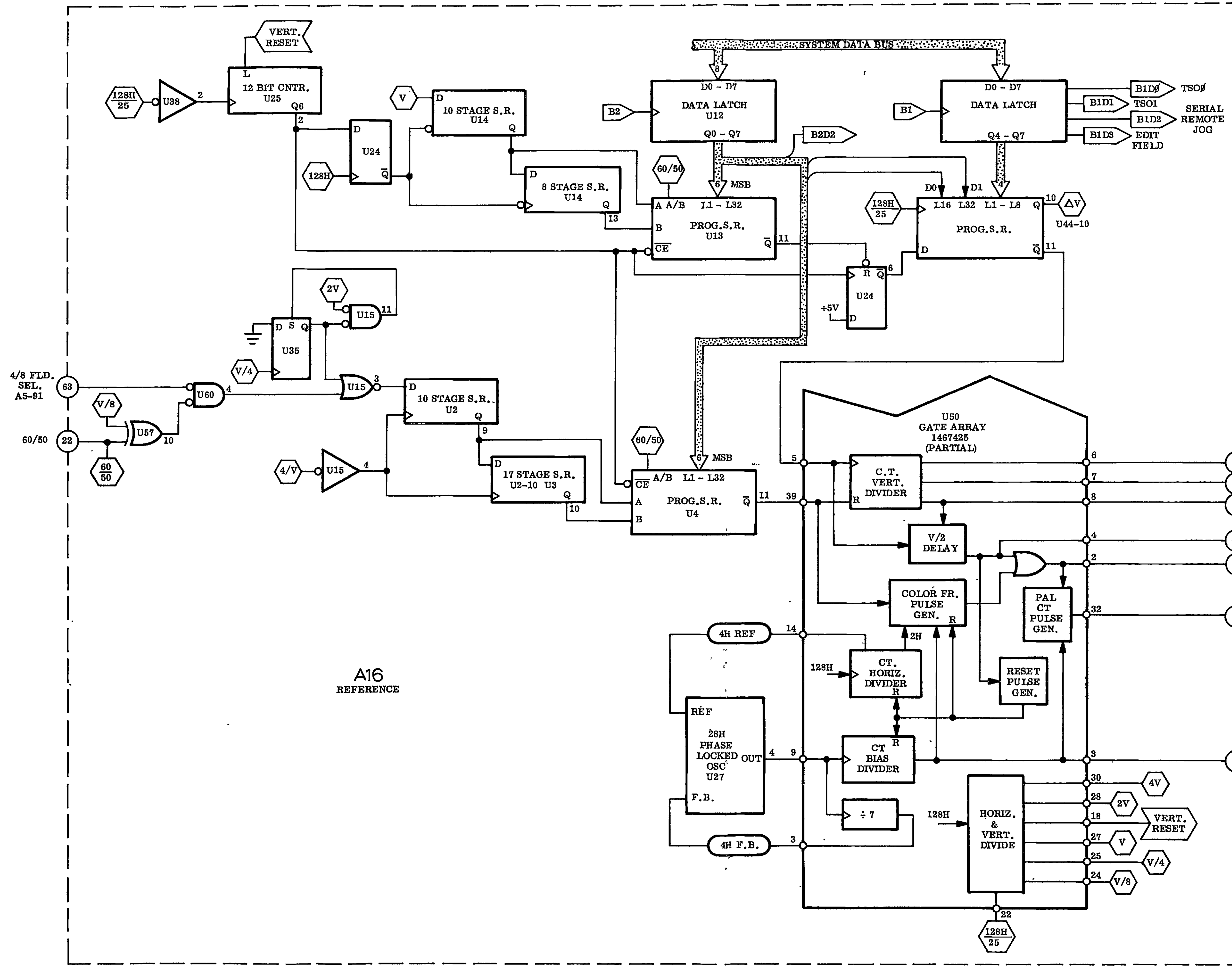
9-2a/2b



VPR-3 A16-
REFERENCE PWA
SCANNER REFERENCES

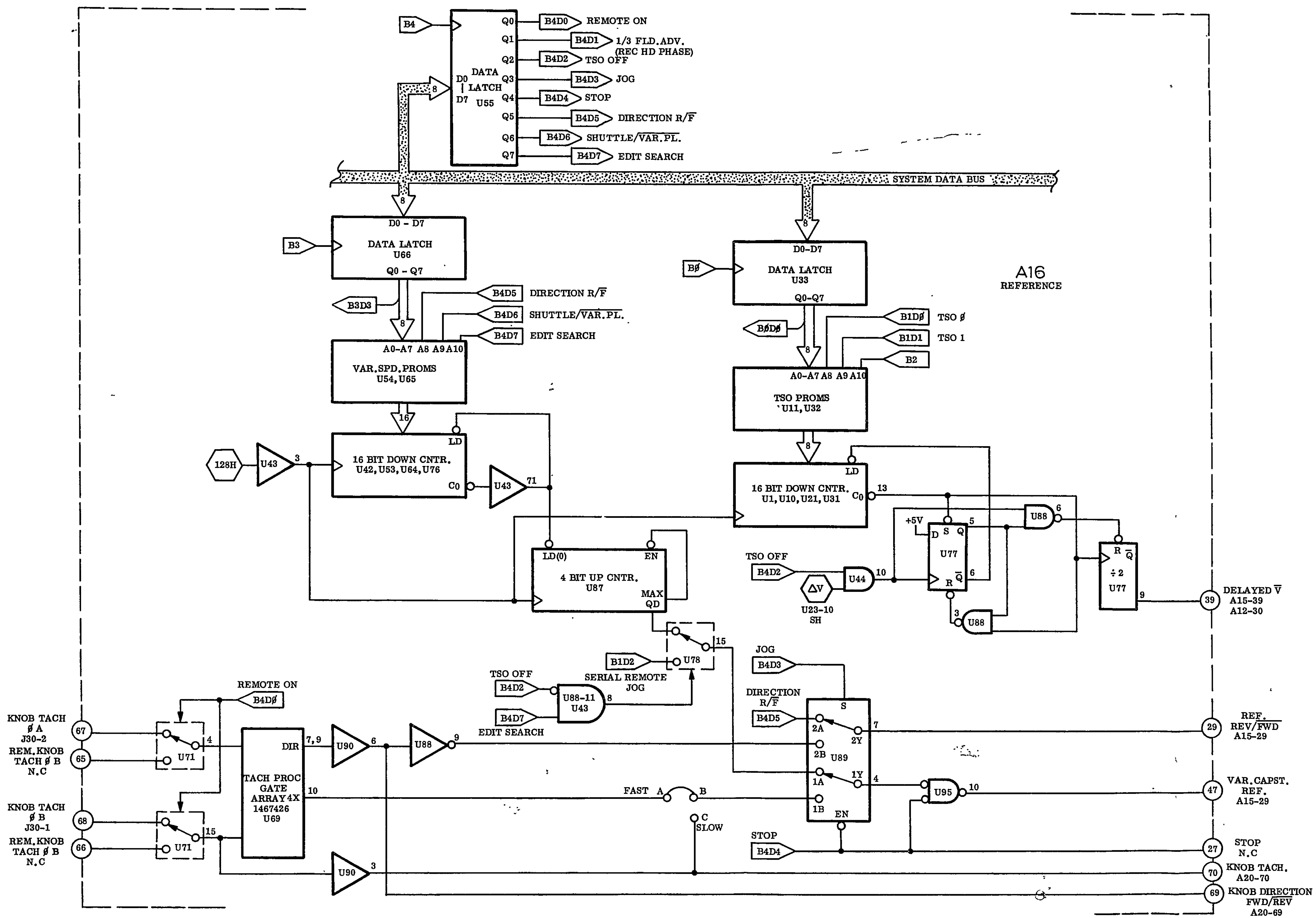
525/625

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 121-2



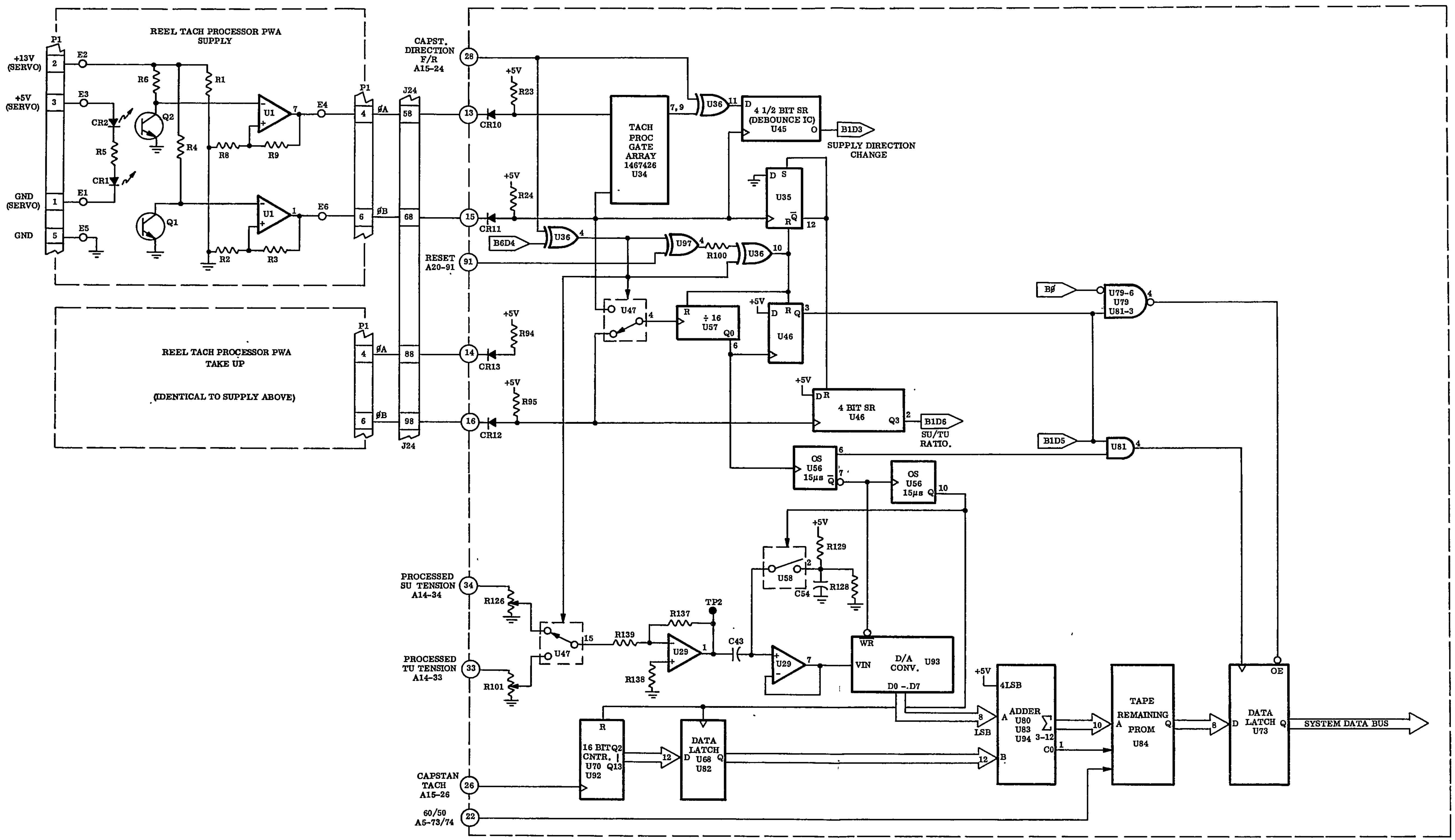
VPR-3 A16- REFERENCE PWA C.T. REFERENCES

525/625

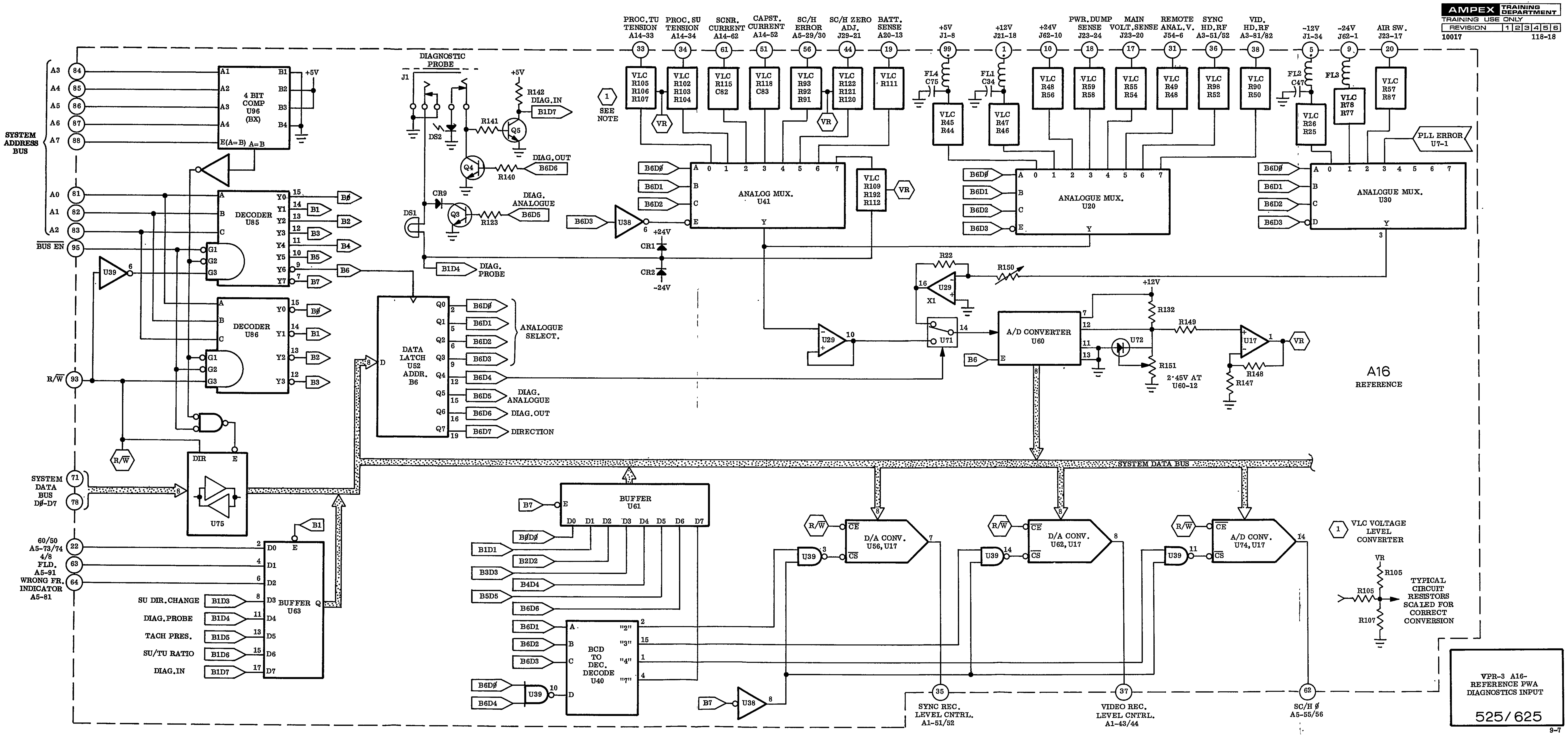


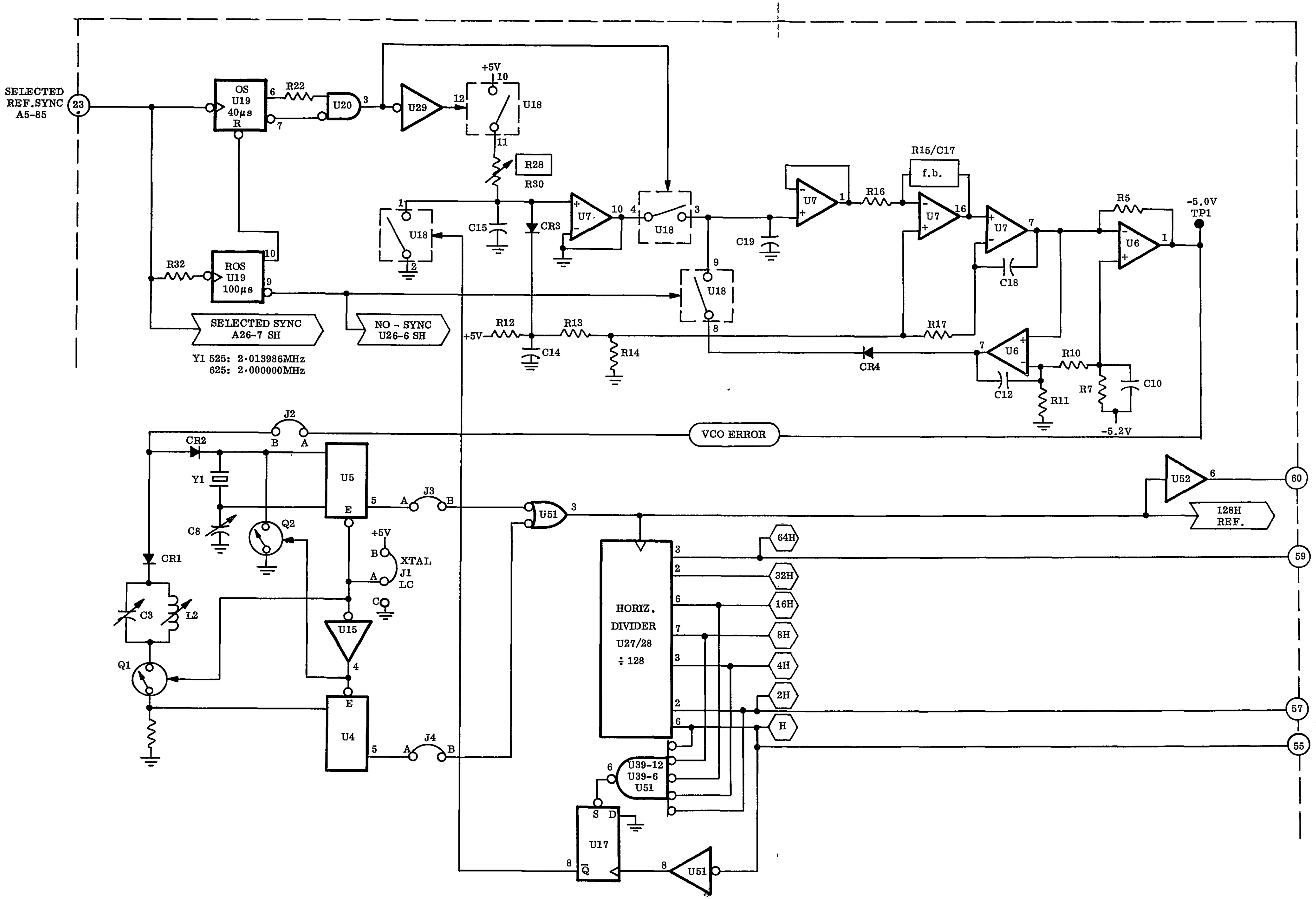
VPR-3 A16-
REFERENCE PWA
CAPSTAN REFERENCES
525/625

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 119-11



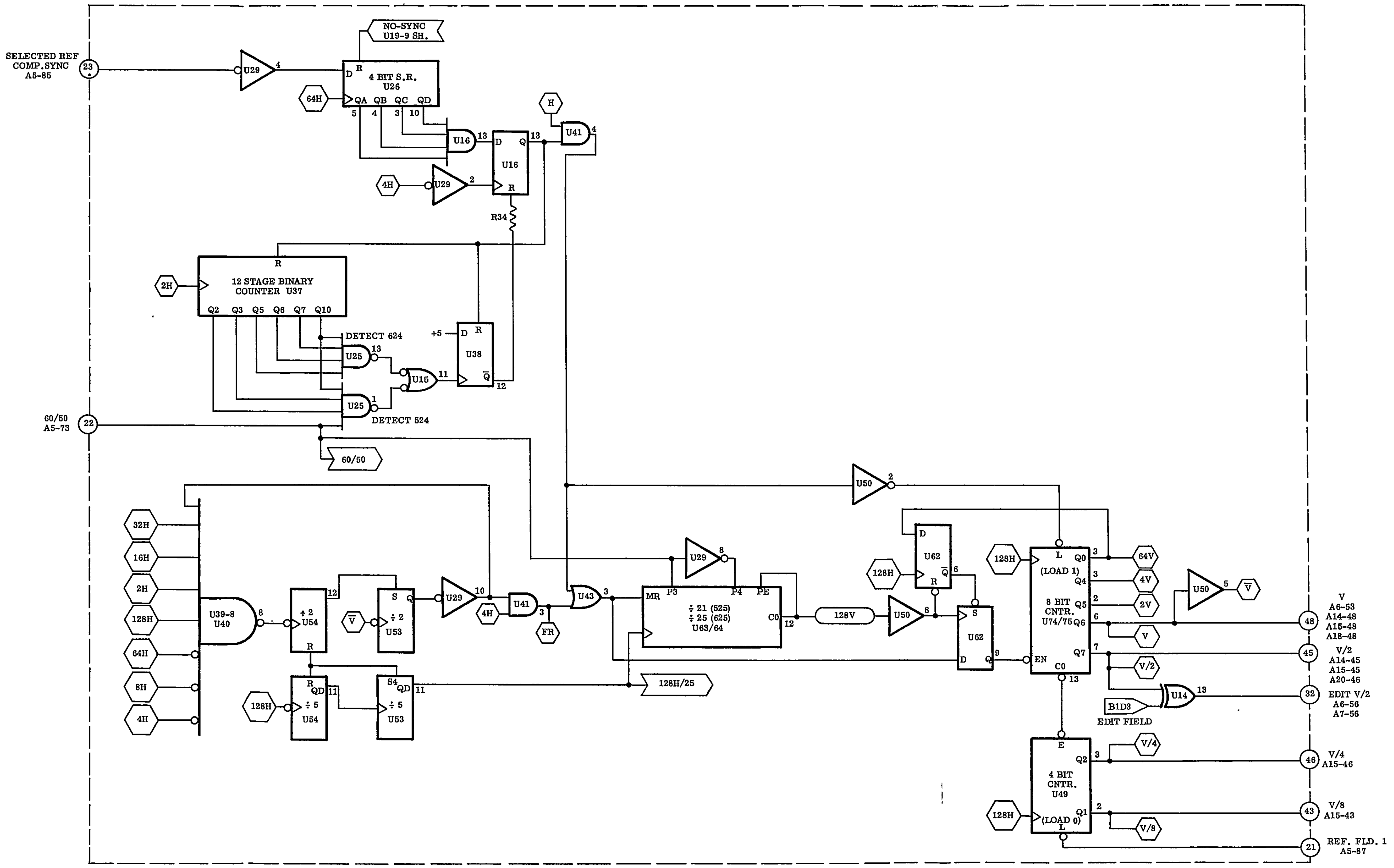
VPR-3 A16
REFERENCE PWA
TAPE REMAINING
525/625


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
118-18
PROC.TU TENSION A14-33
PROC.SU TENSION A14-34
SCNR. CURRENT A14-62
CAPST. CURRENT A14-52
SC/H ERROR A5-29/30
SC/H ZERO ADJ. J29-21
BATT. SENSE A20-13
+5V J1-8
+12V J21-18
+24V J62-10
PWR.DUMP SENSE J23-24
MAIN VOLT.SENSE J23-20
REMOTE ANAL.V. J54-6
SYNC HD.RF A3-51/52
VID. HD.RF A3-81/82
-12V J1-34
-24V J62-1
AIR SW. J23-17
SYSTEM ADDRESS BUS
BUS EN
4 BIT COMP U96 (BX)
DECODER U85
DECODER U86
DIAGNOSTIC PROBE
DIAG.IN
DIAG.OUT
DIAG. ANALOGUE
DIAG. PROBE
SEE NOTE
ANALOG MUX. U41
ANALOGUE MUX. U20
ANALOGUE MUX. U30
PLL ERROR U7-1
DATA LATCH U52 ADDR. B6
ANALOGUE SELECT.
DIRECTION
A/D CONVERTER U60
2.45V AT U60-12
A16 REFERENCE
SYSTEM DATA BUS
SYSTEM DATA BUS DØ-D7
60/50 A5-73/74
4/8 FLD. A5-91
WRONG FR. INDICATOR A5-81
SU DIR.CHANGE
DIAG.PROBE
TACH PRES.
SU/TU RATIO
DIAG.IN
BUFFER U63
BUFFER U61
BCD TO DEC. DECODE U40
D/A CONV. U56, U17
D/A CONV. U62, U17
A/D CONV. U74, U17
VLC VOLTAGE LEVEL CONVERTER
TYPICAL CIRCUIT RESISTORS SCALED FOR CORRECT CONVERSION
SYNC REC. LEVEL CNTRL. A1-51/52
VIDEO REC. LEVEL CNTRL. A1-43/44
SC/H Ø A5-55/56
VPR-3 A16-REFERENCE PWA DIAGNOSTICS INPUT
525/625
9-7

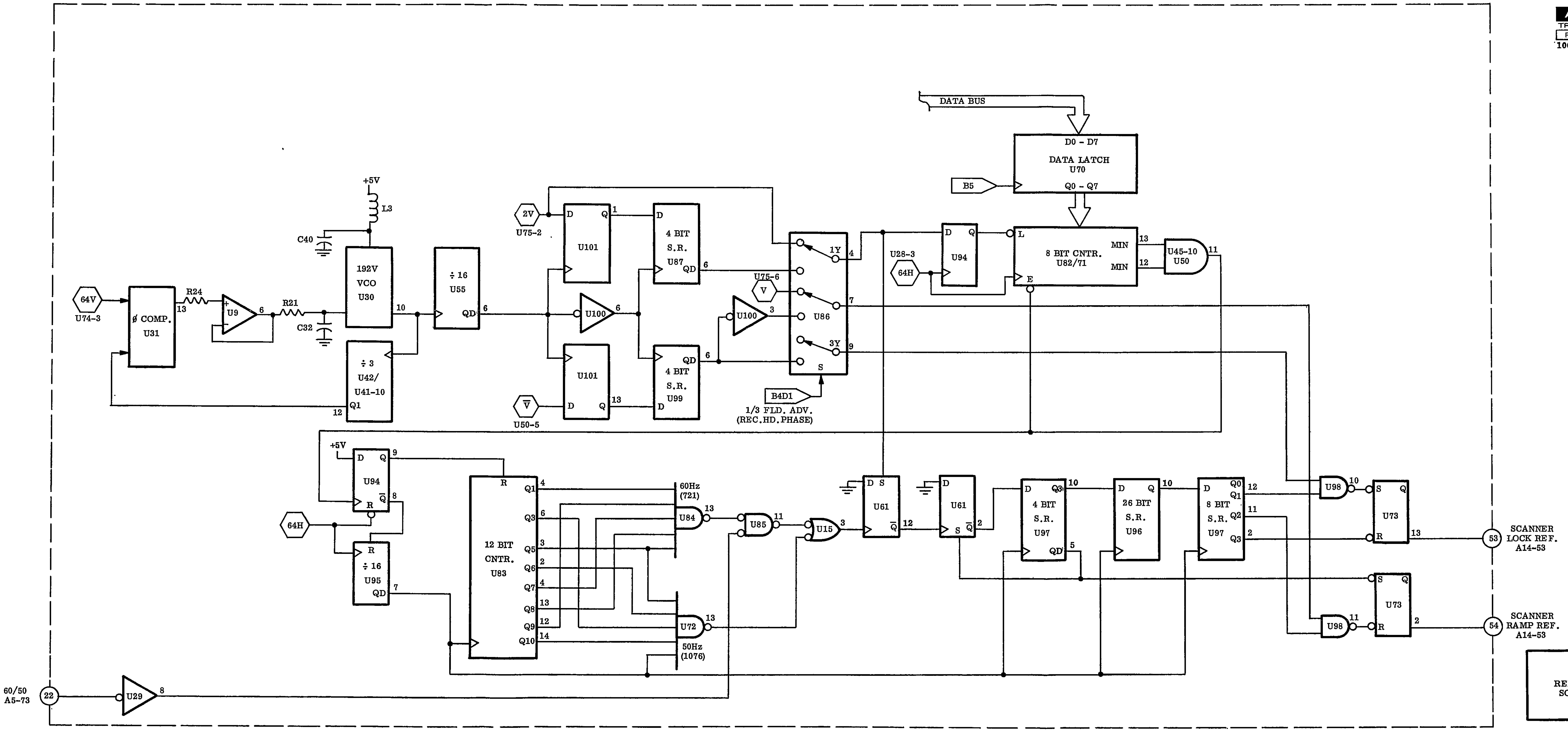


VPR-3 A16-1/5
REFERENCE PWA
(EARLY)
128H OSC. & HORIZ.
DIVIDER

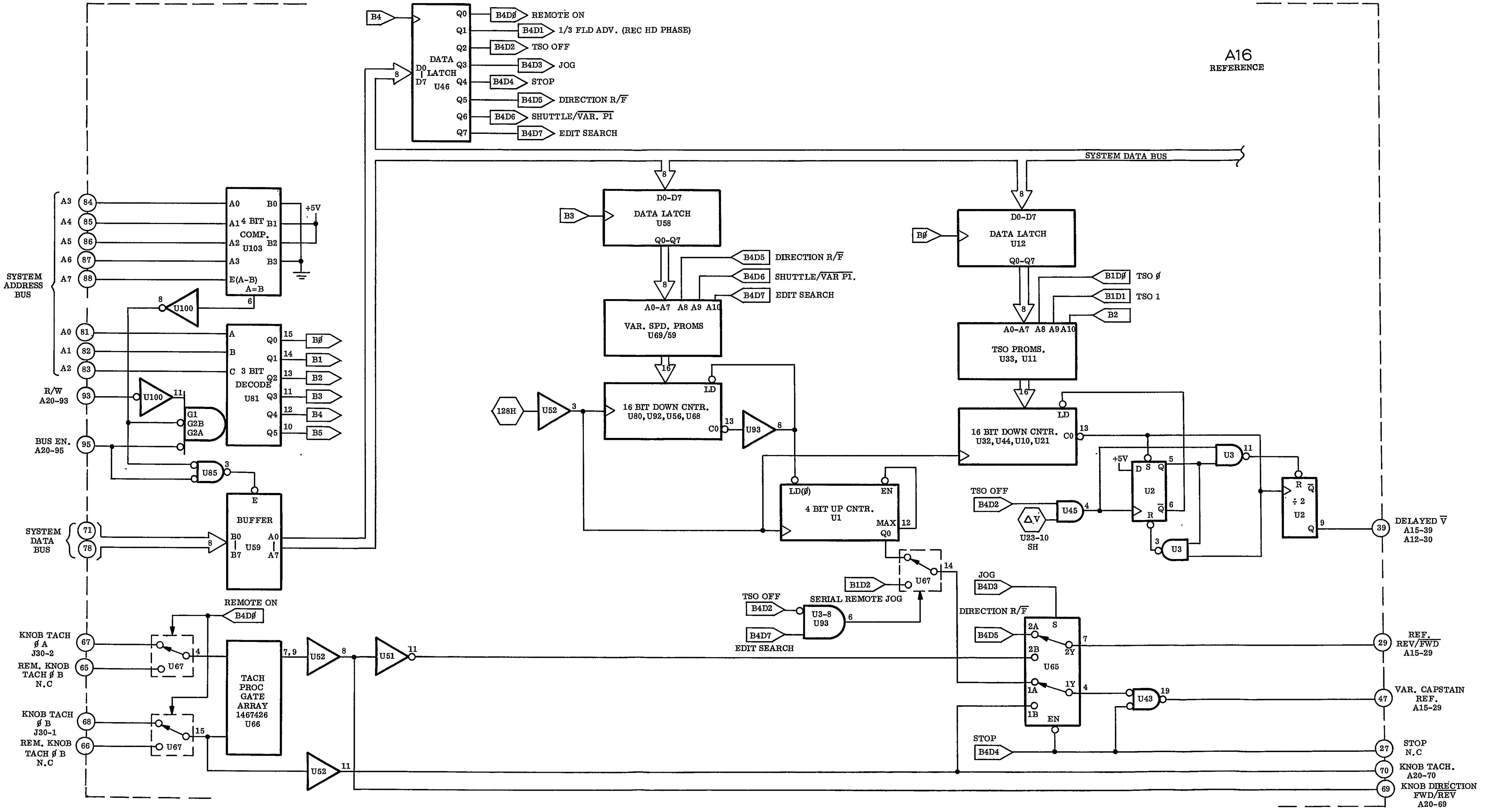
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 108-26



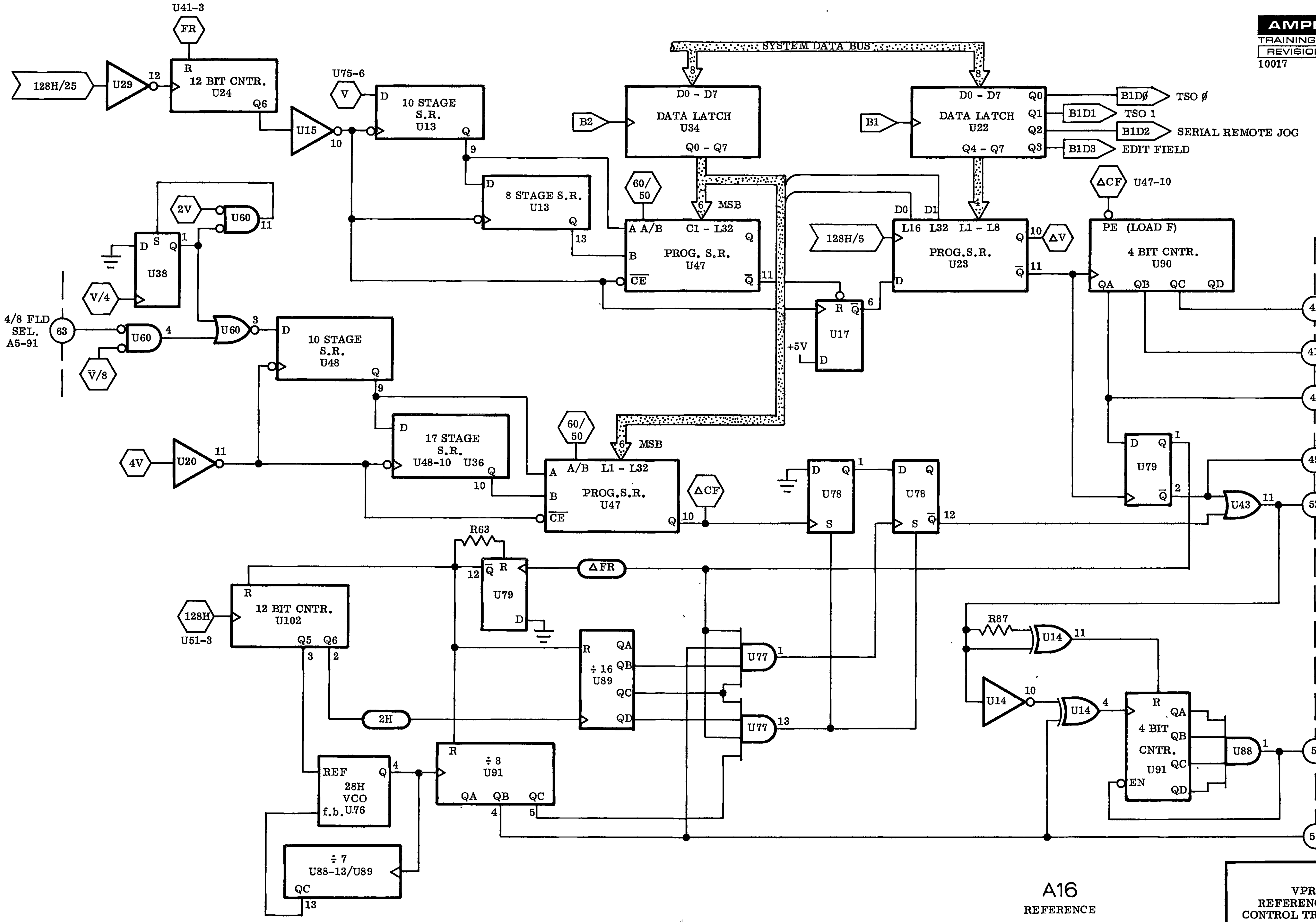
VPR-3 A16- 2/5
REFERENCE PWA (EARLY)
VERTICAL DIVIDERS
525/625



VPR-3 A16-3/5
REFERENCE PWA (EARLY)
SCANNER REFERENCES
525/625

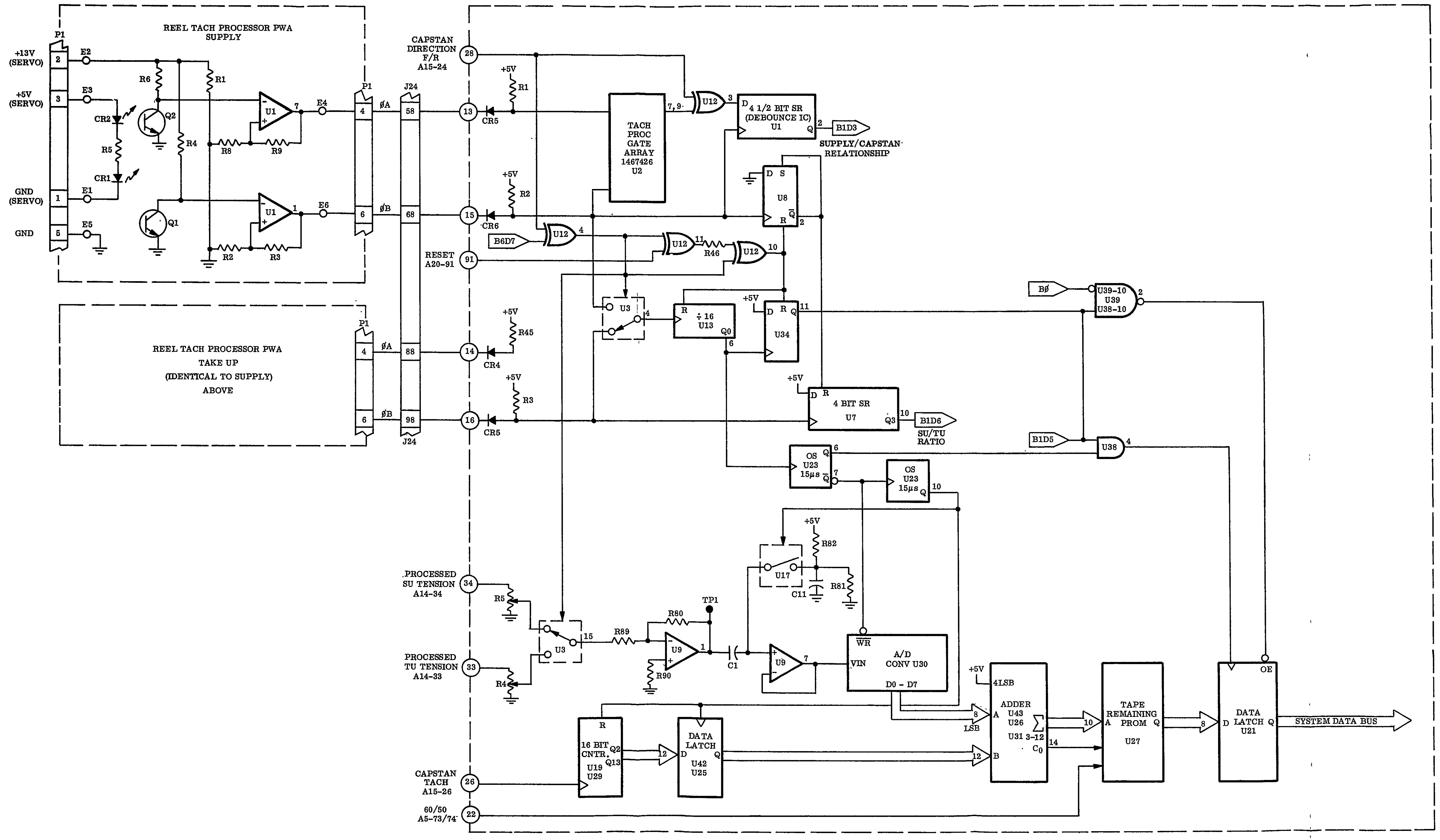


VPR-3 A16-4/5
REFERENCE PWA (EARLY)
CAPSTAN REFERENCES
525/625

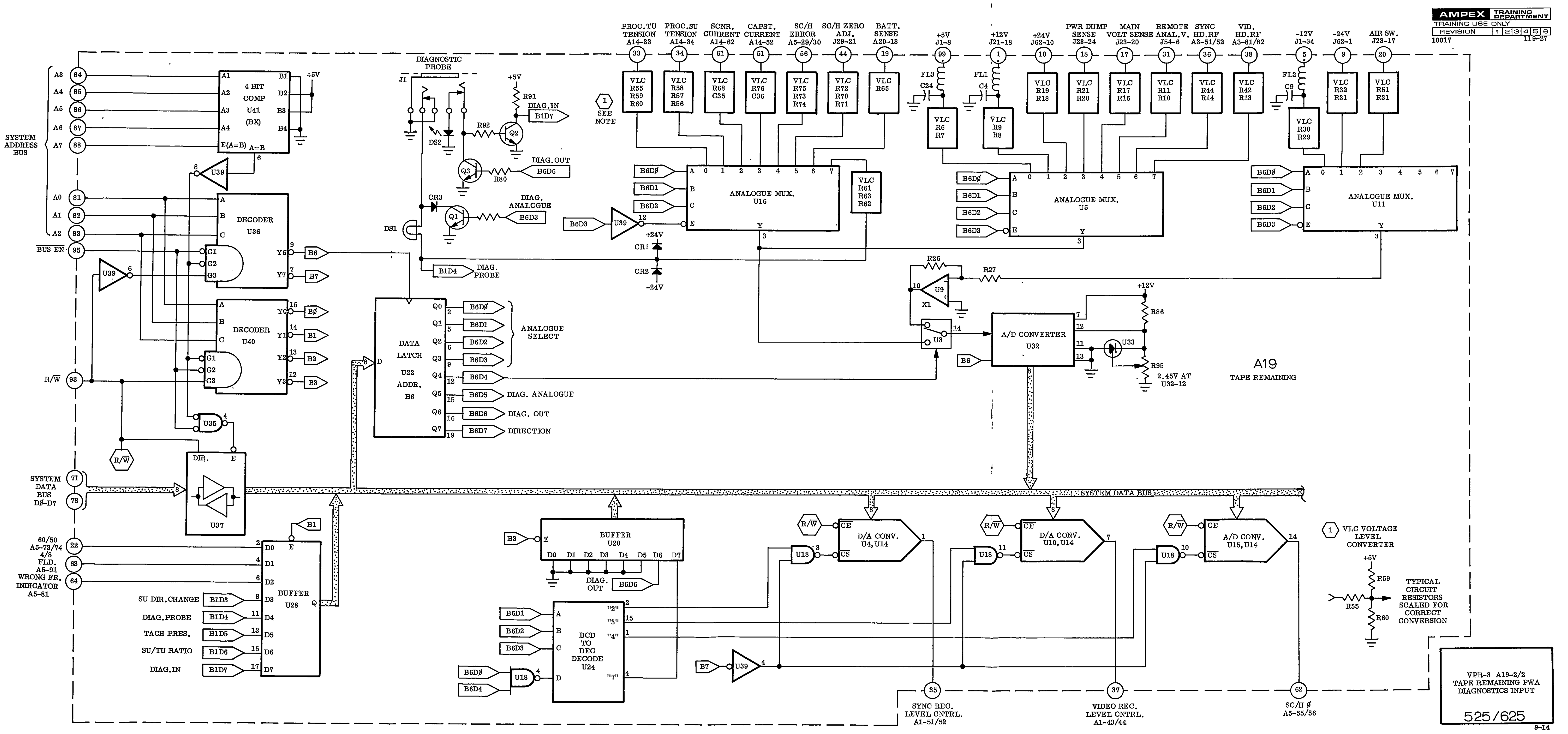


A16
REFERENCE

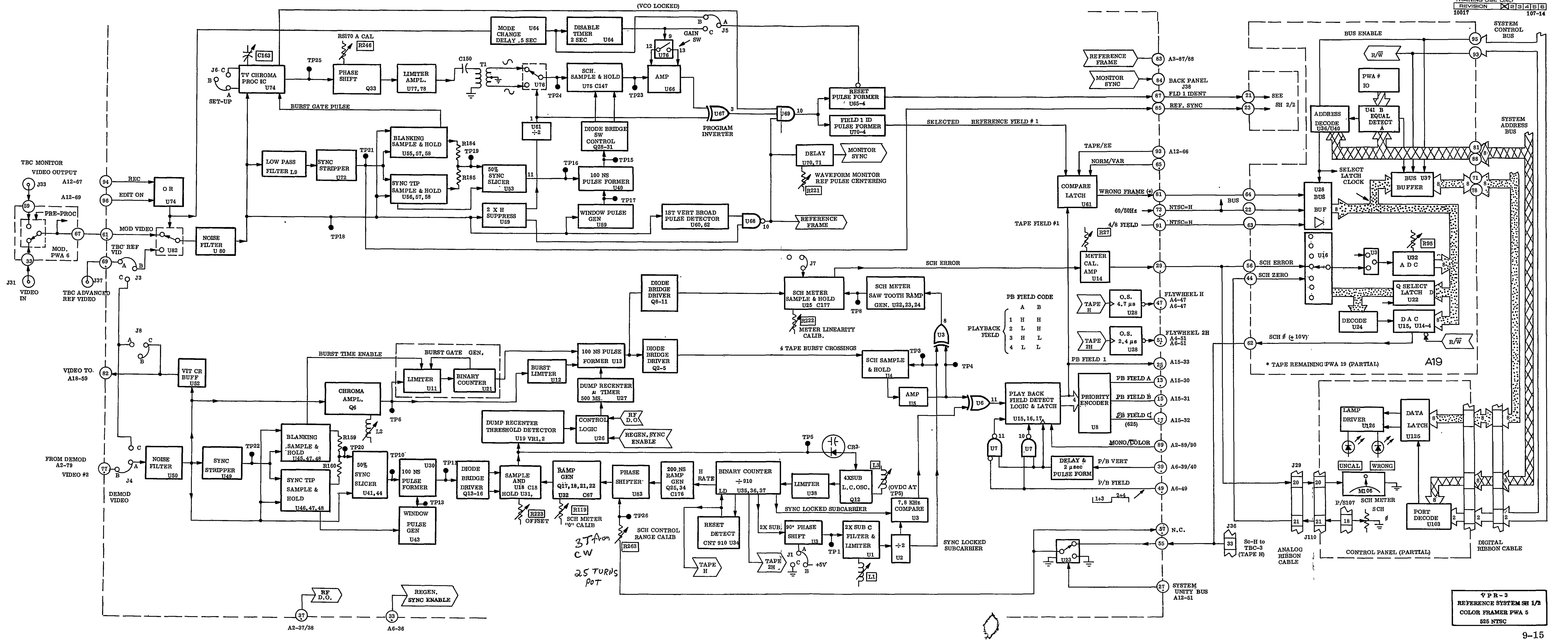
VPR-3 A16-4/5
REFERENCE PWA (EARLY)
CONTROL TRACK REFERENCES
525/625



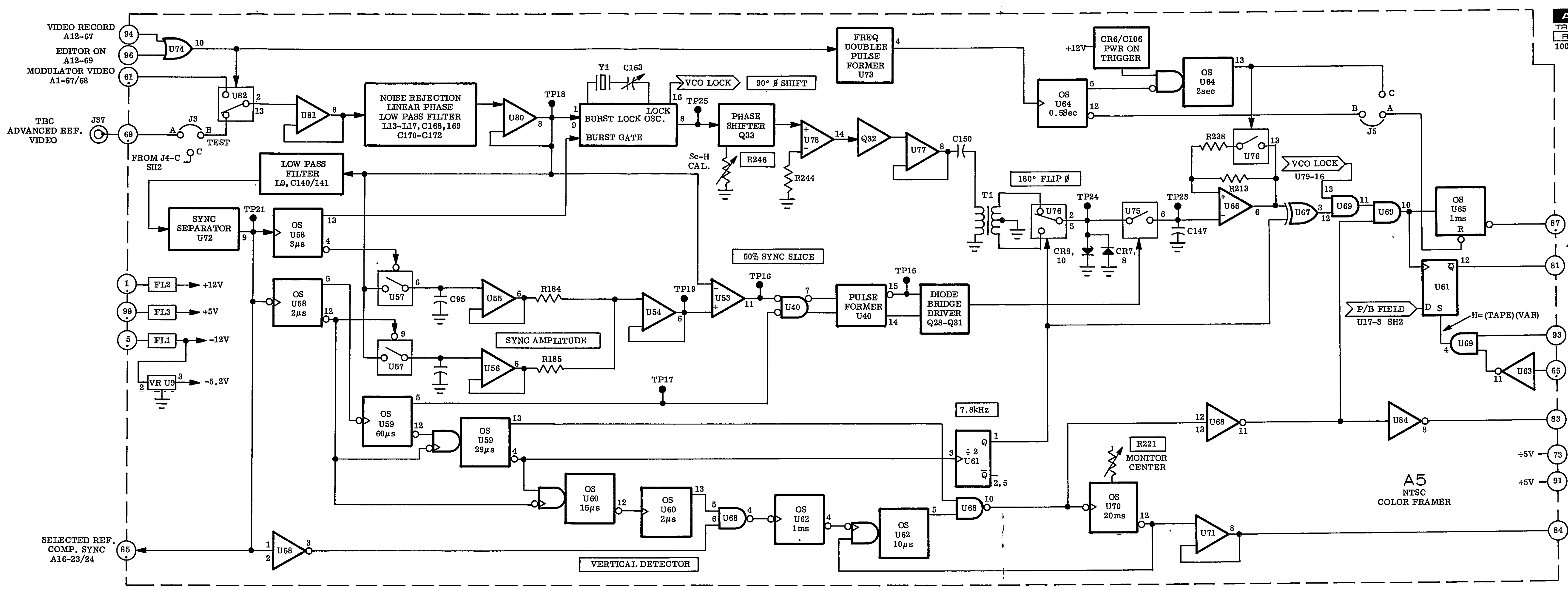
VPR-3 A19-1/2
TAPE REMAINING PWA
PACK DIAM. MEASURE
525/625

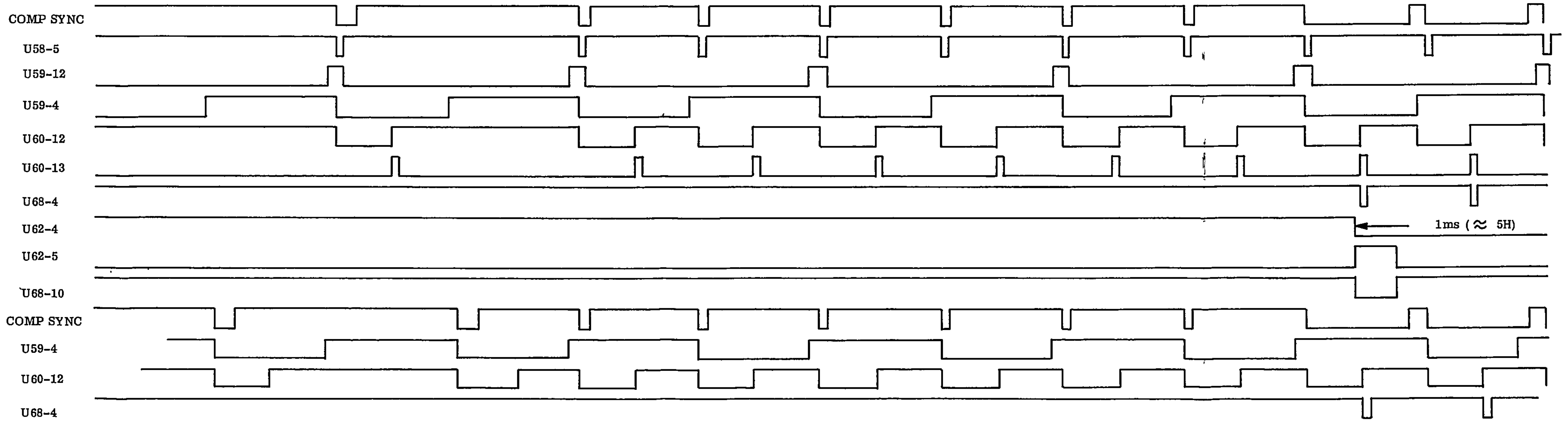


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
119-27
PROC.TU TENSION A14-33
PROC.SU TENSION A14-34
SCNR. CURRENT A14-62
CAPST. CURRENT A14-52
SC/H ERROR A5-29/30
SC/H ZERO ADJ. J29-21
BATT. SENSE A20-13
+5V J1-8
+12V J21-18
+24V J62-10
PWR DUMP SENSE J23-24
MAIN VOLT SENSE J23-20
REMOTE ANAL.V. J54-6
SYNC HD.RF A3-51/52
VID. HD.RF A3-81/82
-12V J1-34
-24V J62-1
AIR SW. J23-17
DIAGNOSTIC PROBE
SEE NOTE
SYSTEM ADDRESS BUS
4 BIT COMP U41 (BX)
DECODER U36
DECODER U40
ANALOGUE MUX. U16
ANALOGUE MUX. U5
ANALOGUE MUX. U11
DIAG.IN
DIAG.OUT
DIAG. ANALOGUE
DIAG. PROBE
BUS EN
DATA LATCH U22 ADDR. B6
ANALOGUE SELECT
DIAG. ANALOGUE
DIAG. OUT
DIRECTION
A/D CONVERTER U32
2.45V AT U32-12
A19
TAPE REMAINING
SYSTEM DATA BUS DØ-D7
SYSTEM DATA BUS
60/50 A5-73/74
4/8 FLD. A5-91
WRONG FR. INDICATOR A5-81
SU DIR.CHANGE
DIAG.PROBE
TACH PRES.
SU/TU RATIO
DIAG.IN
BUFFER U28
BUFFER U20
BCD TO DEC DECODE U24
D/A CONV. U4,U14
D/A CONV. U10,U14
A/D CONV. U15,U14
VLC VOLTAGE LEVEL CONVERTER
TYPICAL CIRCUIT RESISTORS SCALED FOR CORRECT CONVERSION
SYNC REC. LEVEL CNTRL. A1-51/52
VIDEO REC. LEVEL CNTRL. A1-43/44
SC/H Ø A5-55/56
VPR-3 A19-2/2 TAPE REMAINING PWA DIAGNOSTICS INPUT
525/625
9-14



VPR-3
REFERENCE SYSTEM SH 1/2
COLOR FRAMER PWA 5
525 NTSC

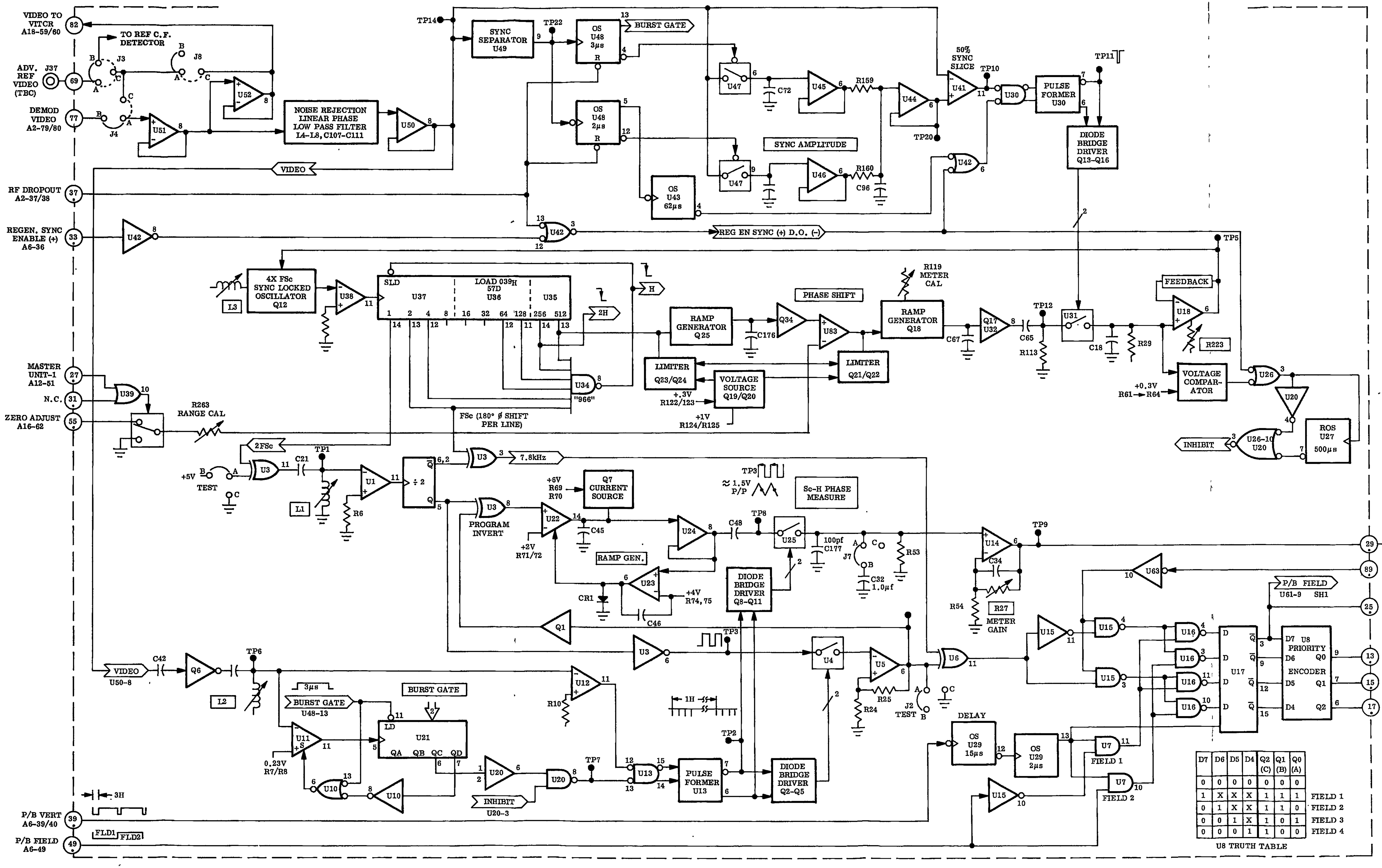




FIELD 1 PULSE TIMING

VPR-3 A5-1
COLOR FRAMER
REFERENCE
FIELD 1

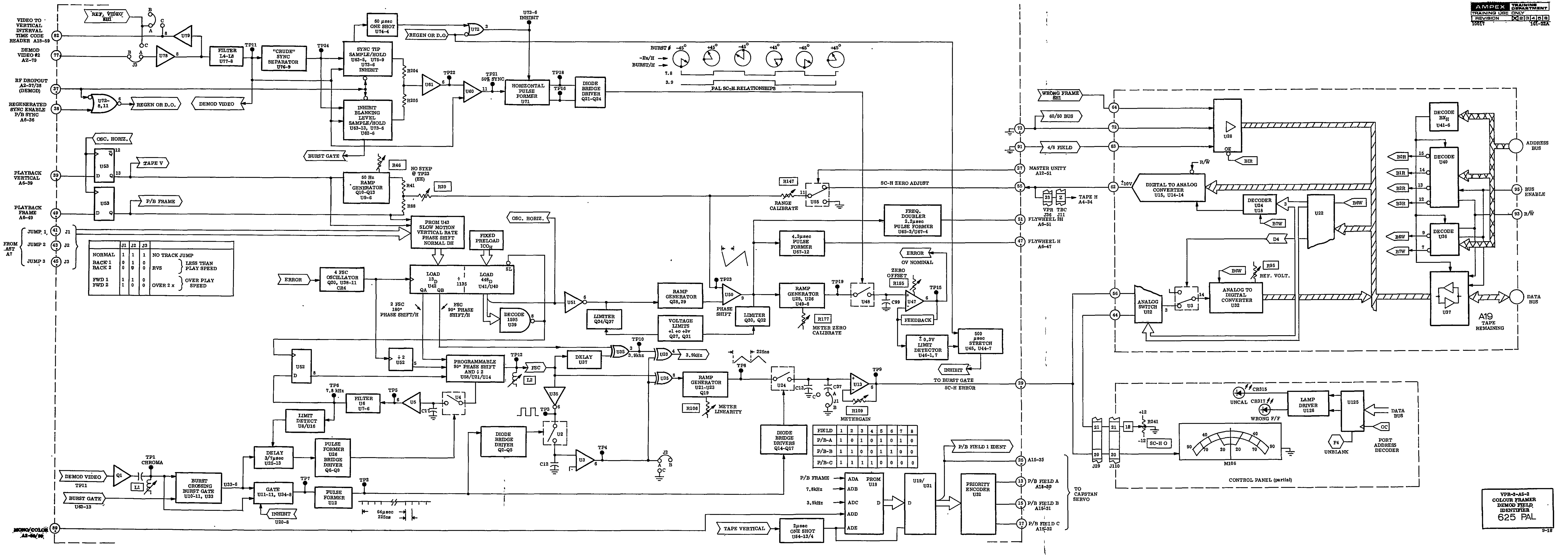
NTSC



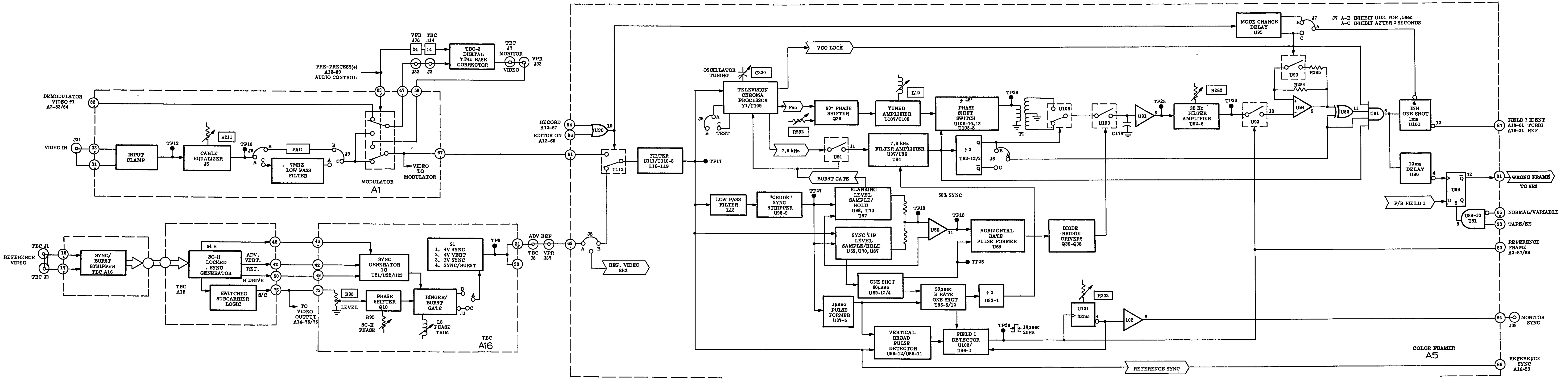
D7	D6	D5	D4	Q2 (C)	Q1 (B)	Q0 (A)	
0	0	0	0	0	0	0	
1	X	X	X	1	1	1	FIELD 1
0	1	X	X	1	1	0	FIELD 2
0	0	1	X	1	0	1	FIELD 3
0	0	0	1	1	0	0	FIELD 4

U8 TRUTH TABLE

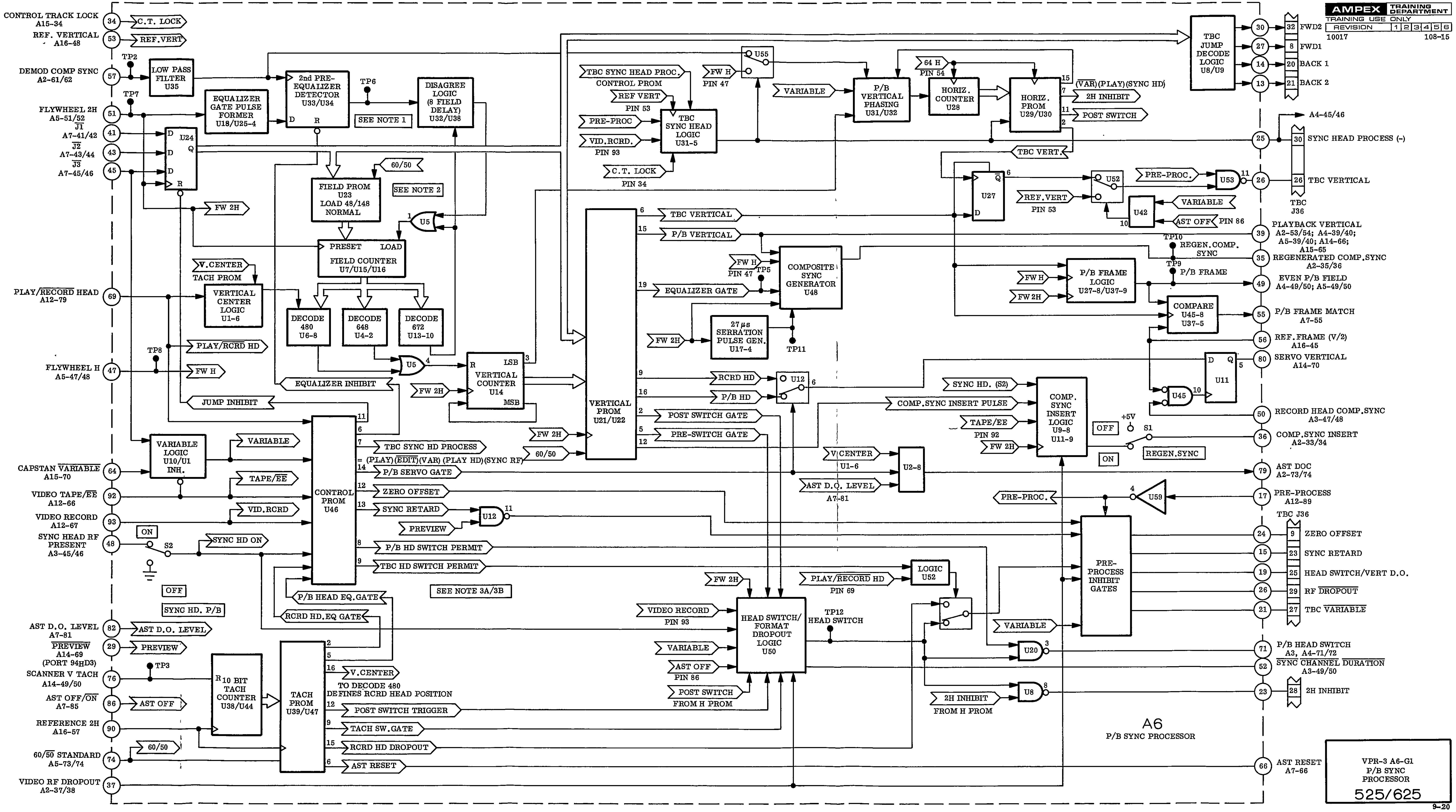
VPR-3 A5-2/2
COLOR FRAMER
DEMOD VIDEO
ScH



AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION
VIDEO TO VERTICAL INTERVAL TIME CODE READER A18-59
DEMOD VIDEO #2 A2-79
RF DROPOUT A2-37/38 (DEMOD)
REGENERATED SYNC ENABLE P/B SYNC A6-36
PLAYBACK VERTICAL A6-39
PLAYBACK FRAME A6-49
FROM AST A7
JUMP 1
JUMP 2
JUMP 3
REF. VIDEO
FILTER L4-L8 U77-8
"CRUDE" SYNC SEPARATOR U76-9
SYNC TIP SAMPLE/HOLD
INHIBIT BLANKING LEVEL SAMPLE/HOLD
60 µsec ONE SHOT U74-4
REGEN OR D.O.
DEMOD VIDEO
BURST GATE
U73-6 INHIBIT
HORIZONTAL PULSE FORMER U71
DIODE BRIDGE DRIVER Q21-Q24
PAL SC-H RELATIONSHIPS
OSC. HORIZ.
TAPE V
P/B FRAME
50 Hz RAMP GENERATOR Q10-Q13 U9-6
NO STEP @ TP23 (EE)
PROM U43 SLOW MOTION VERTICAL RATE PHASE SHIFT NORMAL DH
FIXED PRELOAD ICOH
NORMAL
BACK 1
BACK 2
NO TRACK JUMP
RVS
LESS THAN PLAY SPEED
FWD 1
FWD 2
OVER 2 x
OVER PLAY SPEED
ERROR
4 FSC OSCILLATOR Q20, U38-11 CR4
DECODE 1595 U39
2 FSC 180° PHASE SHIFT/H
FSC 90° PHASE SHIFT/H
PROGRAMMABLE 90° PHASE SHIFT AND ÷ 2 U58/U21/U14
DELAY U37
3.9kHz
RAMP GENERATOR U21-U23 Q19
METER LINEARITY
METERGAIN
LIMITER Q34/Q37
RAMP GENERATOR Q28, 29
VOLTAGE LIMITS +1 to +3v Q27, Q31
PHASE SHIFT
LIMITER Q30, Q32
RANGE CALIBRATE
SC-H ZERO ADJUST
FREQ. DOUBLER 2.2µsec PULSE FORMER U65-3/U67-4
4.3µsec PULSE FORMER U67-12
RAMP GENERATOR U25, U26 U49-8
METER ZERO CALIBRATE
ZERO OFFSET
ERROR
OV NOMINAL
FEEDBACK
± 0.3V LIMIT DETECTOR U46-1, 7
500 µsec STRETCH U45, U44-7
INHIBIT
TO BURST GATE
SC-H ERROR
MASTER UNITY A12-51
FLYWHEEL 2H A6-51
FLYWHEEL H A6-47
TAPE H A4-34
LIMIT DETECT U8/U16
FILTER U6 U7-6
DEMOD VIDEO
BURST GATE
BURST CROSSING BURST GATE U10-11, U33
DELAY 3/7µsec U25-13
PULSE FORMER U26 BRIDGE DRIVER Q5-Q9
GATE U11-11, U34-8
PULSE FORMER U12
DIODE BRIDGE DRIVER Q2-Q5
DIODE BRIDGE DRIVERS Q14-Q17
P/B FIELD 1 IDENT
PROM U18
PRIORITY ENCODER U32
P/B FIELD A A15-30
P/B FIELD B A15-31
P/B FIELD C A15-32
TO CAPSTAN SERVO
TAPE VERTICAL
2µsec ONE SHOT U64-13/4
MONO/COLOR
WRONG FRAME
60/50 BUS
4/8 FIELD
DIGITAL TO ANALOG CONVERTER U15, U14-14
DECODER U24 U18
ANALOG SWITCH U22
ANALOG TO DIGITAL CONVERTER U32
REF. VOLT.
DECODE BX U41-6
DECODE U40
DECODE U36
ADDRESS BUS
BUS ENABLE
R/W
DATA BUS
A19 TAPE REMAINING
UNCAL
WRONG F/F
LAMP DRIVER U126
DATA BUS
PORT ADDRESS DECODER
UNBLANK
SC-H O
CONTROL PANEL (partial)
VPR-3-A5-2 COLOUR FRAMER DEMOD FIELD IDENTIFIER 625 PAL

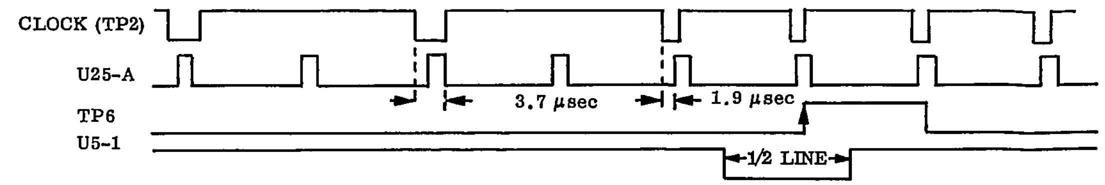


VPR 3 - A5 -1
COLOUR FRAMER
REFERENCE FIELD 1
IDENTIFIER
625 PAL


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
108-15
CONTROL TRACK LOCK A15-34
REF. VERTICAL A16-48
DEMOD COMP SYNC A2-61/62
FLYWHEEL 2H A5-51/52
J1 A7-41/42
J2 A7-43/44
J3 A7-45/46
PLAY/RECORD HEAD A12-79
FLYWHEEL H A5-47/48
CAPSTAN VARIABLE A15-70
VIDEO TAPE/EE A12-66
VIDEO RECORD A12-67
SYNC HEAD RF PRESENT A3-45/46
AST D.O. LEVEL A7-81
PREVIEW A14-69 (PORT 94HD3)
SCANNER V TACH A14-49/50
AST OFF/ON A7-85
REFERENCE 2H A16-57
60/50 STANDARD A5-73/74
VIDEO RF DROPOUT A2-37/38
C.T. LOCK
REF.VERT
TP2
LOW PASS FILTER U35
TP7
EQUALIZER GATE PULSE FORMER U18/U25-4
2nd PRE-EQUALIZER DETECTOR U33/U34
TP6
DISAGREE LOGIC (8 FIELD DELAY) U32/U38
SEE NOTE 1
U24
FIELD PROM U23 LOAD 48/148 NORMAL
60/50
SEE NOTE 2
U5
FW 2H
PRESET LOAD
FIELD COUNTER U7/U15/U16
V.CENTER
TACH PROM
VERTICAL CENTER LOGIC U1-6
DECODE 480 U6-8
DECODE 648 U4-2
DECODE 672 U13-10
PLAY/RCRD HD
TP8
FW H
LSB
VERTICAL COUNTER U14
MSB
FW 2H
EQUALIZER INHIBIT
JUMP INHIBIT
VARIABLE LOGIC U10/U1 INH.
VARIABLE
TAPE/EE
VID.RCRD
ON
S2
SYNC HD ON
OFF
SYNC HD. P/B
CONTROL PROM U46
TBC SYNC HEAD PROCESS
(PLAY)(EDIT)(VAR)(PLAY HD)(SYNC RF)
P/B SERVO GATE
ZERO OFFSET
SYNC RETARD
PREVIEW
U12
P/B HD SWITCH PERMIT
TBC HD SWITCH PERMIT
P/B HEAD EQ.GATE
RCRD HD.EQ GATE
SEE NOTE 3A/3B
AST D.O. LEVEL
PREVIEW
TP3
10 BIT TACH COUNTER U38/U44
TACH PROM U39/U47
AST OFF
60/50
V.CENTER
TO DECODE 480 DEFINES RCRD HEAD POSITION
POST SWITCH TRIGGER
TACH SW.GATE
RCRD HD DROPOUT
AST RESET
TBC SYNC HEAD PROC.
CONTROL PROM
REF VERT PIN 53
PRE-PROC
VID.RCRD. PIN 93
C.T. LOCK PIN 34
TBC SYNC HEAD LOGIC U31-5
FW H PIN 47
U55
VARIABLE
P/B VERTICAL PHASING U31/U32
64 H PIN 54
HORIZ. COUNTER U28
HORIZ. PROM U29/U30
(VAR)(PLAY)(SYNC HD)
2H INHIBIT
POST SWITCH
TBC JUMP DECODE LOGIC U8/U9
TBC VERT.
U27
REF.VERT PIN 53
U52
PRE-PROC.
U53
VARIABLE
U42
AST OFF PIN 86
TBC VERTICAL
P/B VERTICAL
FW H PIN 47
TP5
COMPOSITE SYNC GENERATOR U48
EQUALIZER GATE
FW 2H
$27\mu s$ SERRATION PULSE GEN. U17-4
TP11
VERTICAL PROM U21/U22
FW 2H
60/50
TBC HD
P/B HD
U12
POST SWITCH GATE
PRE-SWITCH GATE
TP10
REGEN.COMP. SYNC
TP9
P/B FRAME
FW H
FW 2H
P/B FRAME LOGIC U27-8/U37-9
COMPARE U45-8 U37-5
U11
U45
SYNC HD. (S2)
COMP.SYNC INSERT PULSE
TAPE/EE PIN 92
FW 2H
COMP. SYNC INSERT LOGIC U9-8 U11-9
OFF
+5V
S1
ON
REGEN.SYNC
V CENTER U1-6
U2-8
AST D.O. LEVEL A7-81
PRE-PROC.
U59
PRE-PROCESS INHIBIT GATES
FW 2H
PLAY/RECORD HD PIN 69
LOGIC U52
VIDEO RECORD PIN 93
HEAD SWITCH/ FORMAT DROPOUT LOGIC U50
TP12 HEAD SWITCH
VARIABLE
AST OFF PIN 86
POST SWITCH FROM H PROM
VARIABLE
U20
2H INHIBIT FROM H PROM
U8
A6 P/B SYNC PROCESSOR
FWD2
FWD1
BACK 1
BACK 2
A4-45/46
SYNC HEAD PROCESS (-)
TBC VERTICAL
TBC J36
PLAYBACK VERTICAL A2-53/54; A4-39/40; A5-39/40; A14-66; A15-65
REGENERATED COMP.SYNC A2-35/36
EVEN P/B FIELD A4-49/50; A5-49/50
P/B FRAME MATCH A7-55
REF.FRAME (V/2) A16-45
SERVO VERTICAL A14-70
RECORD HEAD COMP.SYNC A3-47/48
COMP.SYNC INSERT A2-33/34
AST DOC A2-73/74
PRE-PROCESS A12-89
TBC J36
ZERO OFFSET
SYNC RETARD
HEAD SWITCH/VERT D.O.
RF DROPOUT
TBC VARIABLE
P/B HEAD SWITCH A3, A4-71/72
SYNC CHANNEL DURATION A3-49/50
2H INHIBIT
AST RESET A7-66
VPR-3 A6-G1 P/B SYNC PROCESSOR
525/625
9-20

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 108-14

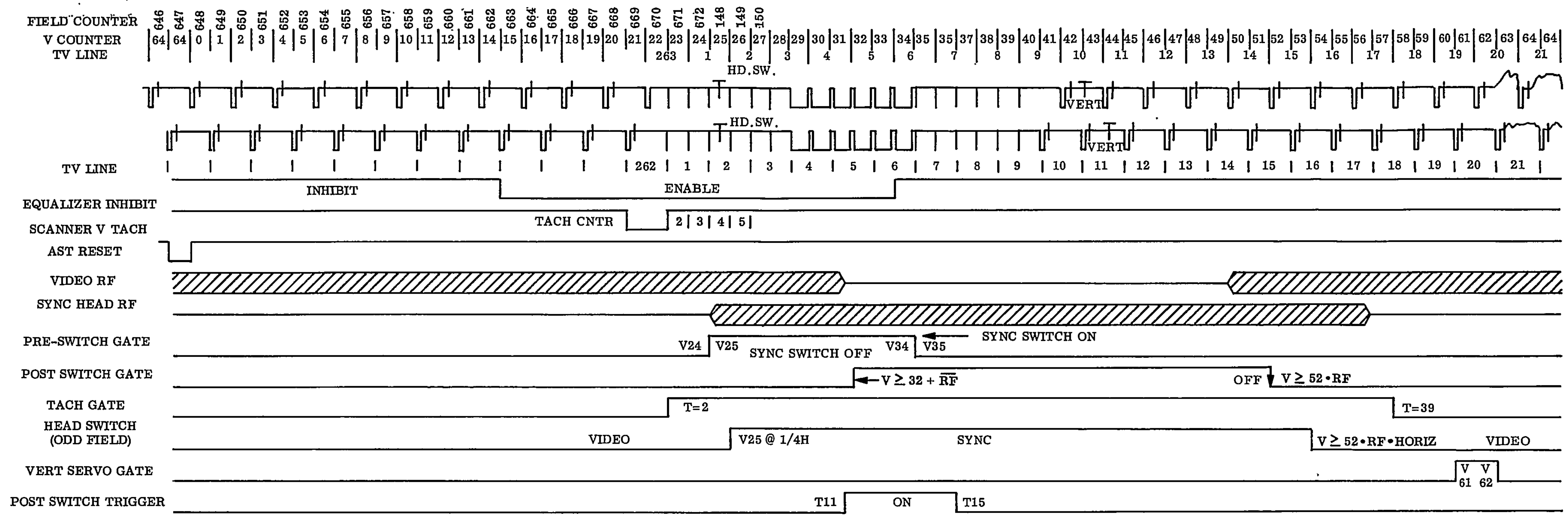
NOTE 1: 2ND EQUALIZER DETECTOR



NOTE 2: FIELD COUNTER PRESET (2H CLOCK)

	J3	J2	J1	FIELD CNTR PRESET 525	FIELD CNTR PRESET 625	DECODE 672 525	DECODE 672 625	DECODE 648 525	DECODE 648 625	TBC DEFINITIONS
NORMAL	1	1	1	148	48	524	624	500	600	NORMAL
BACK 1	0	1	0	153	55	519	617	495	593	LESS THAN PLAY SPEED
BACK 2	0	0	0	158	62	514	610	490	586	REVERSE PLAY
FWD 1	0	1	1	143	41	529	631	505	607	OVER PLAY SPEED
FWD 2	0	0	1	138	34	534	638	510	614	2X PLAY SPEED OR MORE

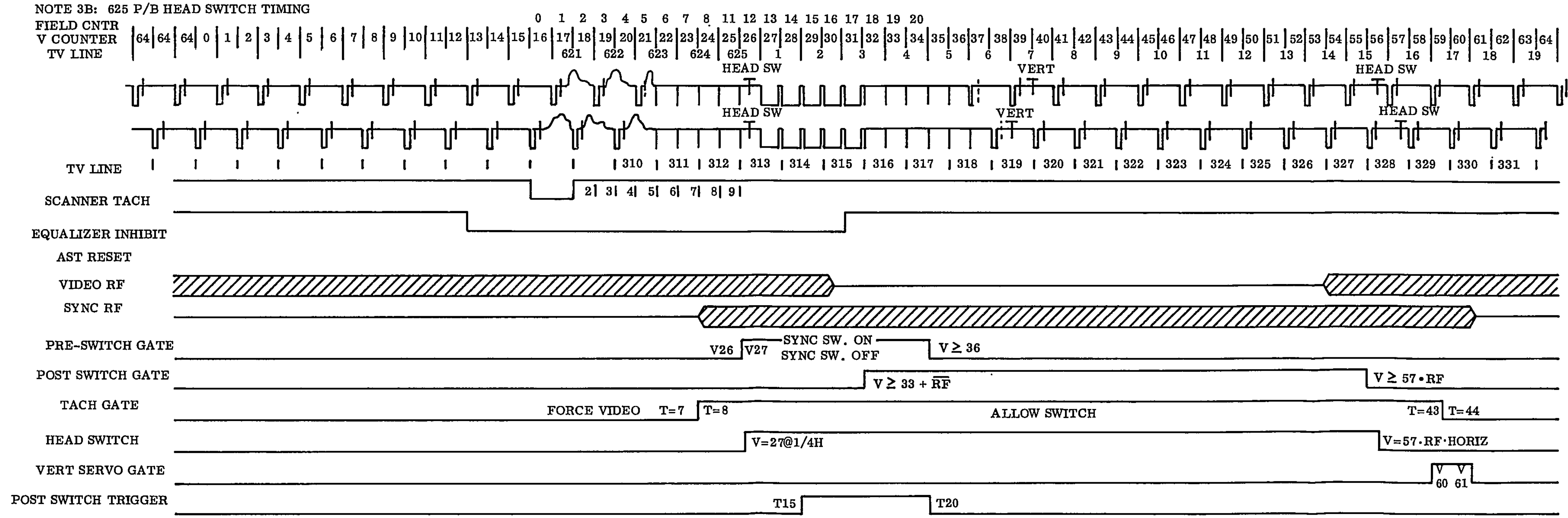
NOTE 3A: 525 P/B HEAD SWITCH TIMING
TACH IS SHOWN WITH RESPECT TO AST HEAD
VERT. SERVO GATE IS TIMED TO RECORD HEAD.



V = VERTICAL COUNTER

T= TACH COUNTER: Defines 360° rotation of the scanner in 32 μsec increments

NOTE 3B: 625 P/B HEAD SWITCH TIMING

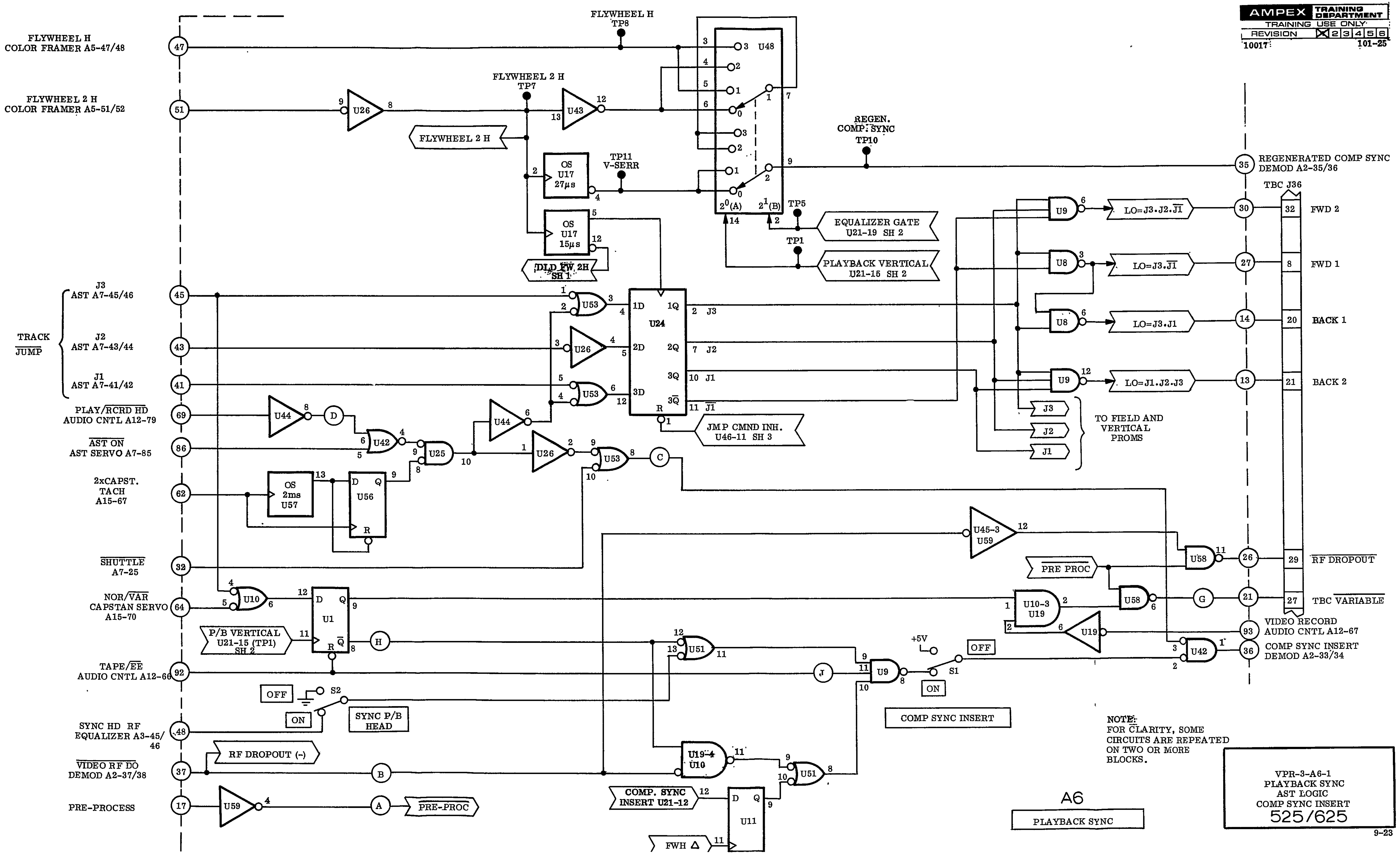


V= VERTICAL COUNTER

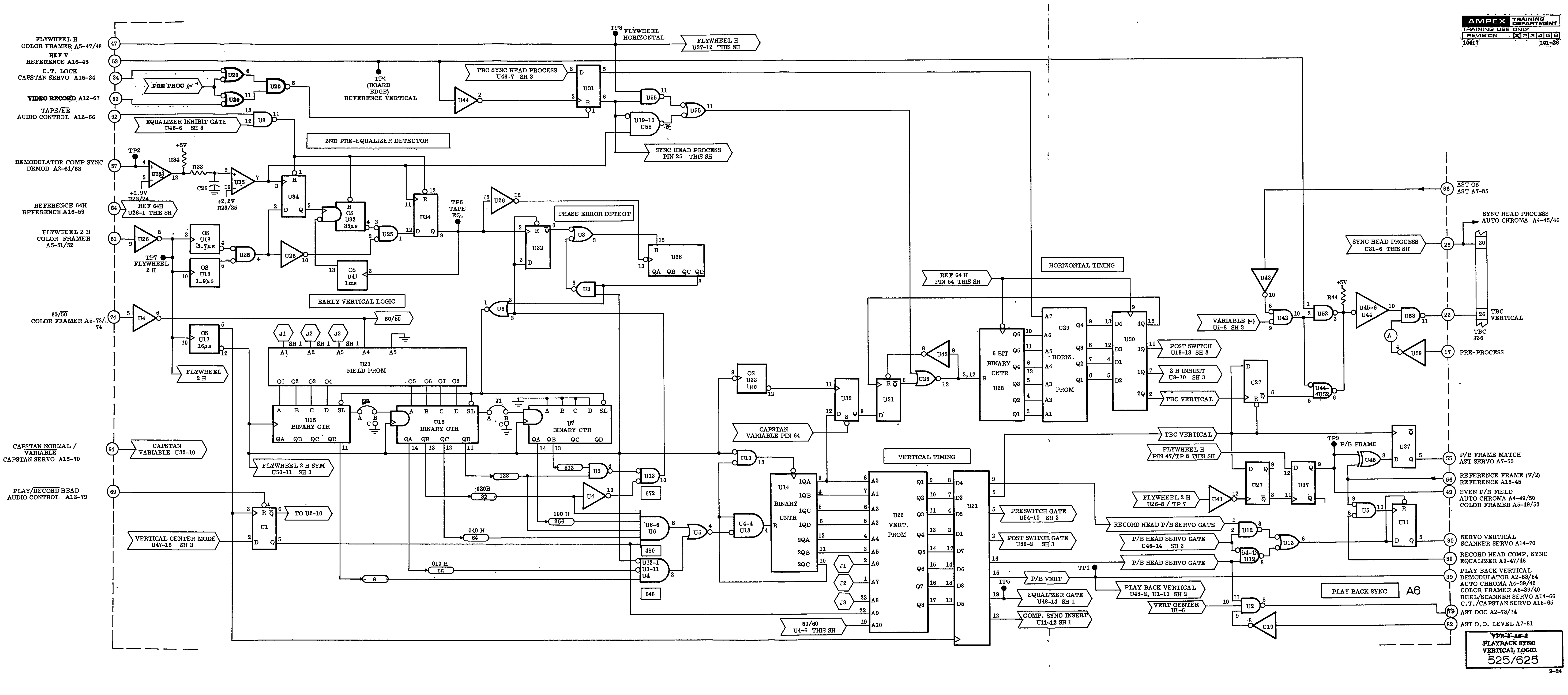
T= TACH COUNTER: Defines 360° rotation of the scanner in 32 μsec increments

VPR-3 – A6-G2
P/B SYNC
PROCESSOR
525/625

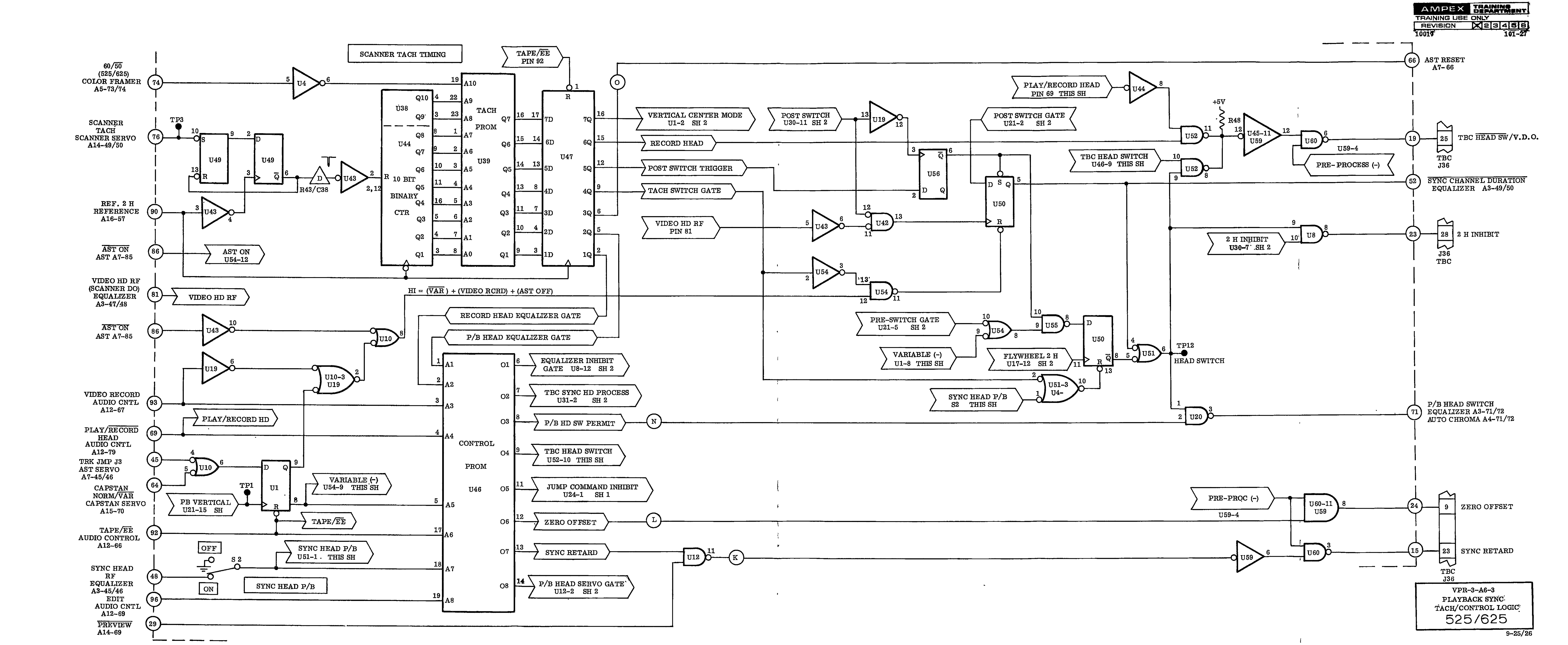
9-21/22

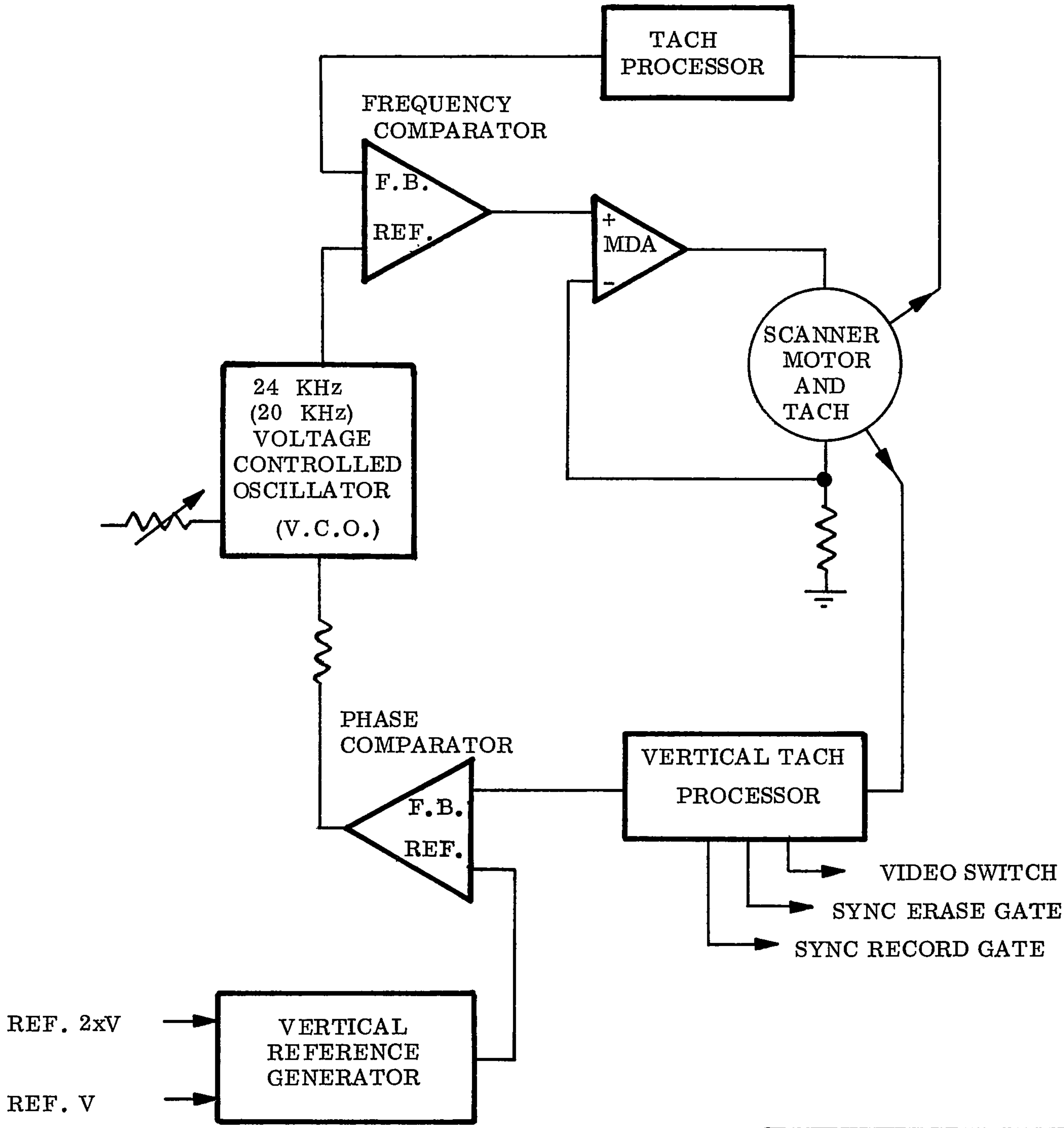


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 2 3 4 5 6
10017
101-25
FLYWHEEL H
COLOR FRAMER A5-47/48
FLYWHEEL 2 H
COLOR FRAMER A5-51/52
FLYWHEEL H TP8
FLYWHEEL 2 H TP7
FLYWHEEL 2 H
OS U17 27μs
TP11 V-SERR
OS U17 15μs
DLD FW 2H SH 1
U48
REGEN. COMP. SYNC TP10
REGENERATED COMP SYNC
DEMOD A2-35/36
TP5
EQUALIZER GATE U21-19 SH 2
TP1
PLAYBACK VERTICAL U21-16 SH 2
TBC J36
LO=J3.J2.J1
LO=J3.J1
LO=J3.J1
LO=J1.J2.J3
FWD 2
FWD 1
BACK 1
BACK 2
TRACK JUMP
J3 AST A7-45/46
J2 AST A7-43/44
J1 AST A7-41/42
U24
JMP CMND INH. U46-11 SH 3
TO FIELD AND VERTICAL PROMS
PLAY/RCRD HD
AUDIO CNTL A12-79
AST ON
AST SERVO A7-85
2xCAPST. TACH A15-67
OS 2ms U57
U56
SHUTTLE A7-25
NOR/VAR
CAPSTAN SERVO A15-70
P/B VERTICAL U21-15 (TP1) SH 2
TAPE/EE
AUDIO CNTL A12-66
OFF
ON
S2
SYNC P/B HEAD
SYNC HD RF
EQUALIZER A3-45/46
RF DROPOUT (-)
VIDEO RF DO
DEMOD A2-37/38
PRE-PROCESS
PRE-PROC
COMP. SYNC INSERT U21-12
FWH
U45-3 U59
PRE PROC
RF DROPOUT
TBC VARIABLE
U10-3 U19
VIDEO RECORD
AUDIO CNTL A12-67
COMP SYNC INSERT
DEMOD A2-33/34
+5V
S1
COMP SYNC INSERT
NOTE:
FOR CLARITY, SOME CIRCUITS ARE REPEATED ON TWO OR MORE BLOCKS.
A6
PLAYBACK SYNC
VPR-3-A6-1
PLAYBACK SYNC
AST LOGIC
COMP SYNC INSERT
525/625
9-23

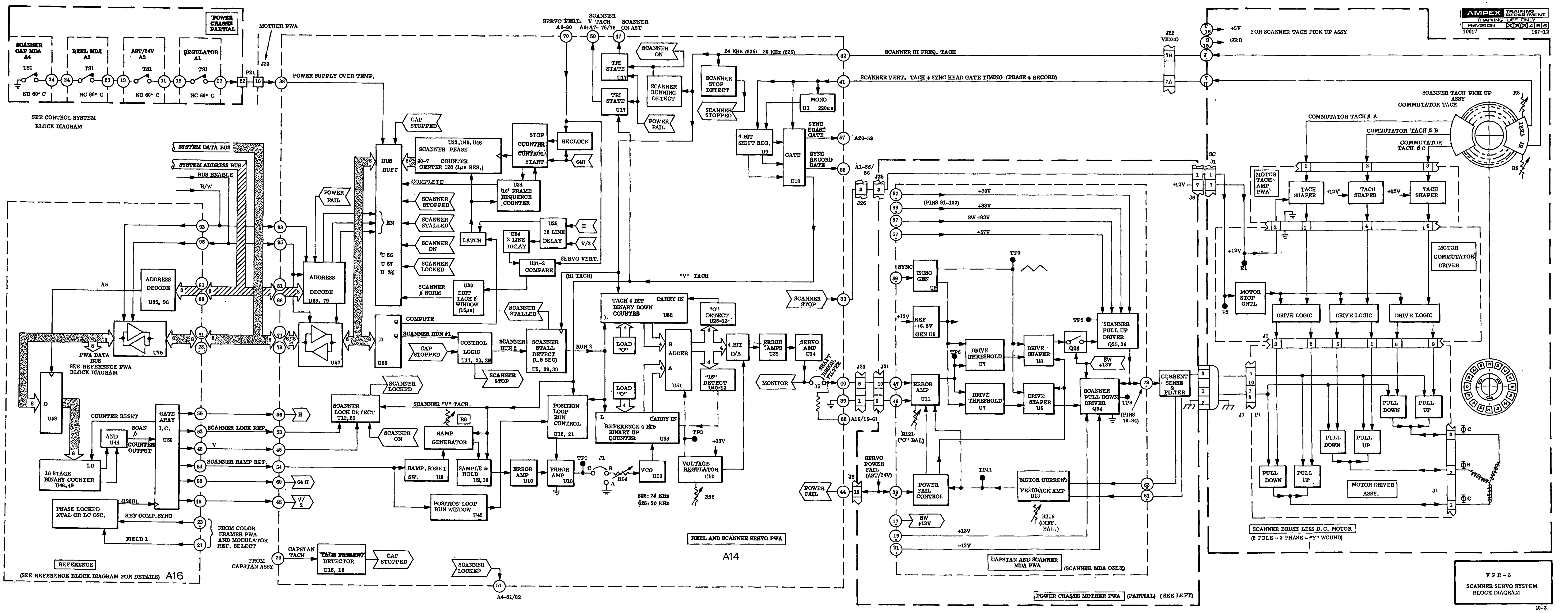


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION
10017
101-26
FLYWHEEL H COLOR FRAMER A5-47/48
REF V REFERENCE A16-48
C.T. LOCK CAPSTAN SERVO A15-34
VIDEO RECORD A12-67
TAPE/EE AUDIO CONTROL A12-66
DEMODULATOR COMP SYNC DEMOD A2-61/62
REFERENCE 64H REFERENCE A16-59
FLYWHEEL 2 H COLOR FRAMER A5-51/52
60/50 COLOR FRAMER A5-73/74
CAPSTAN NORMAL / VARIABLE CAPSTAN SERVO A15-70
PLAY/RECORD HEAD AUDIO CONTROL A12-79
TP8 FLYWHEEL HORIZONTAL
FLYWHEEL H U37-12 THIS SH
TBC SYNC HEAD PROCESS U46-7 SH 3
TP4 (BOARD EDGE) REFERENCE VERTICAL
PRE PROC
EQUALIZER INHIBIT GATE U46-6 SH 3
2ND PRE-EQUALIZER DETECTOR
SYNC HEAD PROCESS PIN 25 THIS SH
REF 64H U28-1 THIS SH
TP6 TAPE EQ.
PHASE ERROR DETECT
EARLY VERTICAL LOGIC
TP7 FLYWHEEL 2 H
U23 FIELD PROM
U15 BINARY CTR
U16 BINARY CTR
U7 BINARY CTR
FLYWHEEL 2 H
CAPSTAN VARIABLE U32-10
FLYWHEEL 2 H SYM U50-11 SH 3
TO U2-10
VERTICAL CENTER MODE U47-16 SH 3
CAPSTAN VARIABLE PIN 64
VERTICAL TIMING
U14 BINARY CNTR
U22 VERT. PROM
50/60 U4-6 THIS SH
REF 64 H PIN 54 THIS SH
HORIZONTAL TIMING
6 BIT BINARY CNTR U28
U29 HORIZ. PROM
U30
POST SWITCH U19-13 SH 3
2 H INHIBIT U8-10 SH 3
TBC VERTICAL
FLYWHEEL H PIN 47/TP 8 THIS SH
FLYWHEEL 2 H U26-8 / TP 7
PRESWITCH GATE U54-10 SH 3
POST SWITCH GATE U50-2 SH 3
RECORD HEAD P/B SERVO GATE
P/B HEAD SERVO GATE U46-14 SH 3
P/B HEAD SERVO GATE
TP1
P/B VERT
TP5
EQUALIZER GATE U48-14 SH 1
COMP. SYNC INSERT U11-12 SH 1
PLAY BACK VERTICAL U48-2, U1-11 SH 2
VERT CENTER U1-6
TP9 P/B FRAME
PLAY BACK SYNC
A6
VARIABLE (-) U1-8 SH 3
SYNC HEAD PROCESS U31-6 THIS SH
AST ON AST A7-85
SYNC HEAD PROCESS AUTO CHROMA A4-45/46
TBC VERTICAL
TBC J36
PRE-PROCESS
P/B FRAME MATCH AST SERVO A7-55
REFERENCE FRAME (V/2) REFERENCE A16-45
EVEN P/B FIELD AUTO CHROMA A4-49/50 COLOR FRAMER A5-49/50
SERVO VERTICAL SCANNER SERVO A14-70
RECORD HEAD COMP. SYNC EQUALIZER A3-47/48
PLAY BACK VERTICAL DEMODULATOR A2-53/54 AUTO CHROMA A4-39/40 COLOR FRAMER A5-39/40 REEL/SCANNER SERVO A14-66 C.T./CAPSTAN SERVO A15-65
AST DOC A2-73/74
AST D.O. LEVEL A7-81
VPR-3-AF-2
PLAYBACK SYNC VERTICAL LOGIC
525/625
9-24

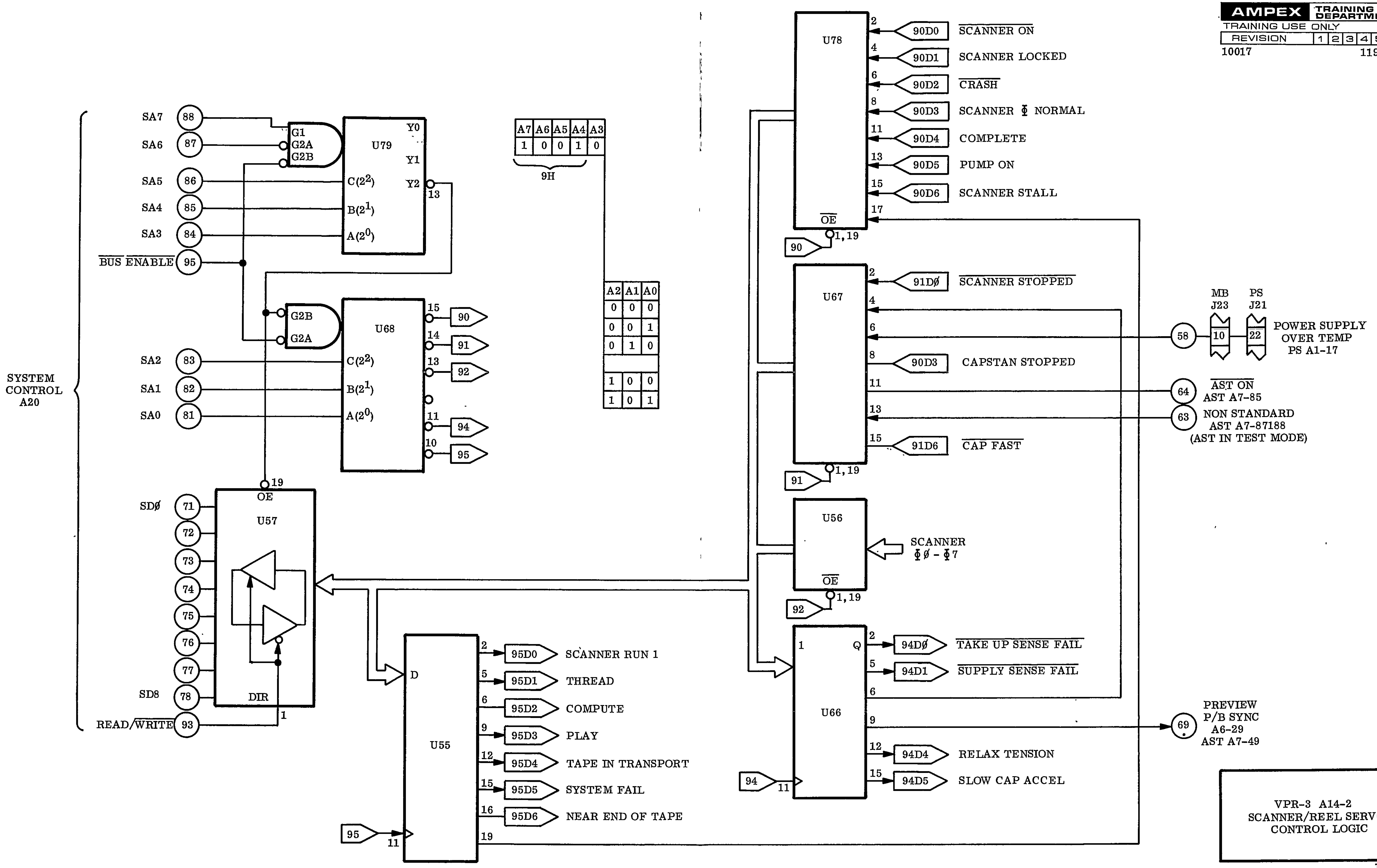

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 2 3 4 5 6
10019 101-27
SCANNER TACH TIMING
60/50 (525/625) COLOR FRAMER A5-73/74
SCANNER TACH SCANNER SERVO A14-49/50
TP3
REF. 2 H REFERENCE A16-57
AST ON AST A7-85
AST ON U54-12
VIDEO HD RF (SCANNER DO) EQUALIZER A3-47/48
VIDEO HD RF
AST ON AST A7-85
VIDEO RECORD AUDIO CNTL A12-67
PLAY/RECORD HEAD AUDIO CNTL A12-79
PLAY/RECORD HD
TRK JMP J3 AST SERVO A7-45/46
CAPSTAN NORM/VAR CAPSTAN SERVO A15-70
PB VERTICAL U21-15 SH
TP1
VARIABLE (-) U54-9 THIS SH
TAPE/EE
TAPE/EE AUDIO CONTROL A12-66
SYNC HEAD P/B U51-1 THIS SH
OFF
ON
S 2
SYNC HEAD P/B
SYNC HEAD RF EQUALIZER A3-45/46
EDIT AUDIO CNTL A12-69
PREVIEW A14-69
R43/C38
10 BIT BINARY CTR
U38
U44
TACH PROM U39
TAPE/EE PIN 92
U47
HI = (VAR) + (VIDEO RCRD) + (AST OFF)
RECORD HEAD EQUALIZER GATE
P/B HEAD EQUALIZER GATE
CONTROL PROM U46
EQUALIZER INHIBIT GATE U8-12 SH 2
TBC SYNC HD PROCESS U31-2 SH 2
P/B HD SW PERMIT
TBC HEAD SWITCH U52-10 THIS SH
JUMP COMMAND INHIBIT U24-1 SH 1
ZERO OFFSET
SYNC RETARD
P/B HEAD SERVO GATE U12-2 SH 2
VERTICAL CENTER MODE U1-2 SH 2
RECORD HEAD
POST SWITCH TRIGGER
TACH SWITCH GATE
VIDEO HD RF PIN 81
POST SWITCH U30-11 SH 2
POST SWITCH GATE U21-2 SH 2
PLAY/RECORD HEAD PIN 69 THIS SH
TBC HEAD SWITCH U46-9 THIS SH
+5V
R48
PRE-PROCESS (-)
U59-4
PRE-SWITCH GATE U21-5 SH 2
VARIABLE (-) U1-8 THIS SH
FLYWHEEL 2 H U17-12 SH 2
SYNC HEAD P/B S2 THIS SH
TP12
HEAD SWITCH
2 H INHIBIT U30-7 SH 2
PRE-PROC (-)
U59-4
AST RESET A7-66
TBC HEAD SW/V.D.O.
TBC J36
SYNC CHANNEL DURATION EQUALIZER A3-49/50
2 H INHIBIT
J36 TBC
P/B HEAD SWITCH EQUALIZER A3-71/72 AUTO CHROMA A4-71/72
ZERO OFFSET
SYNC RETARD
TBC J36
VPR-3-A6-3
PLAYBACK SYNC TACH/CONTROL LOGIC
525/625
9-25/26



VPR-3 G
SCANNER SERVO

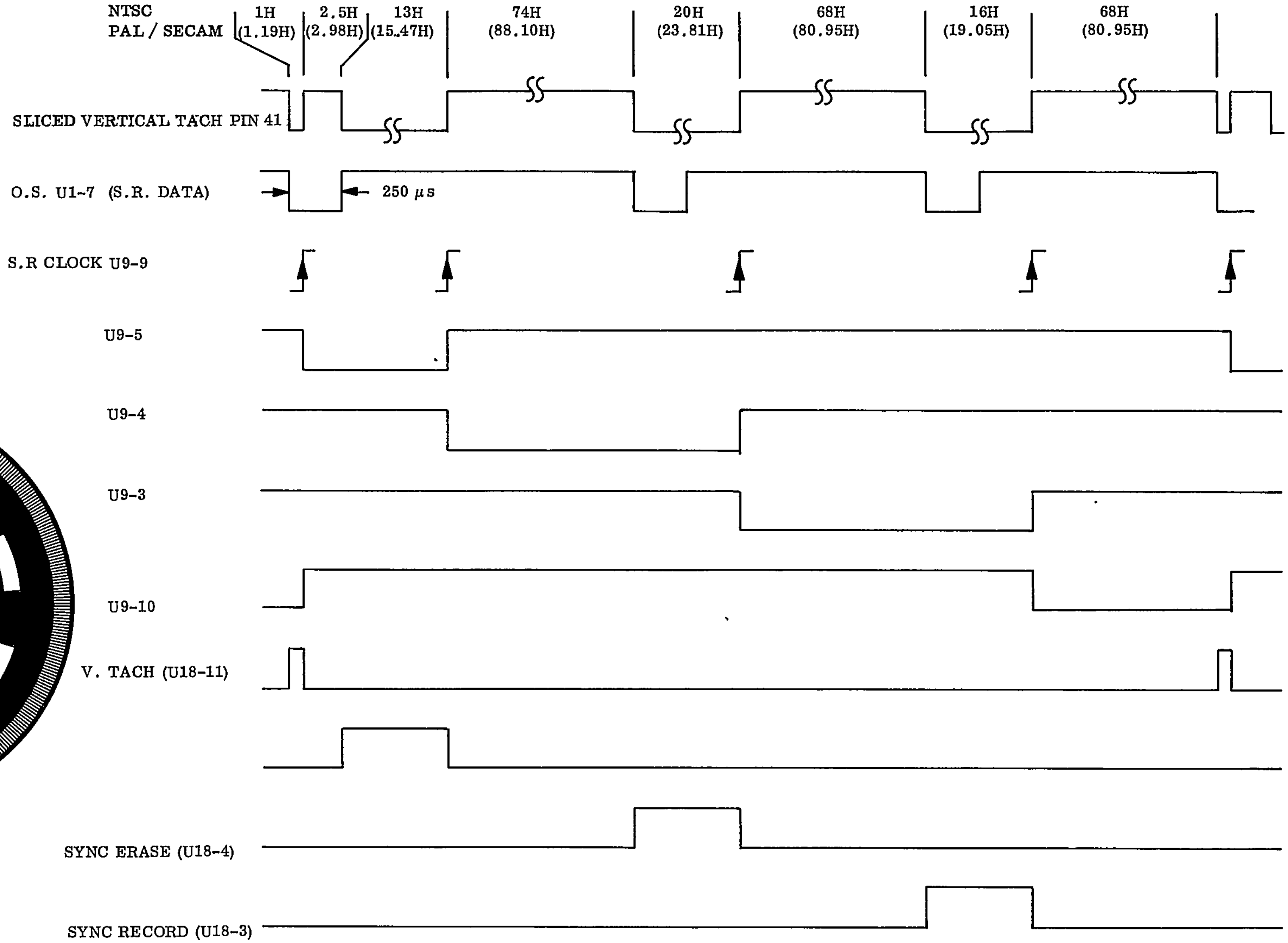


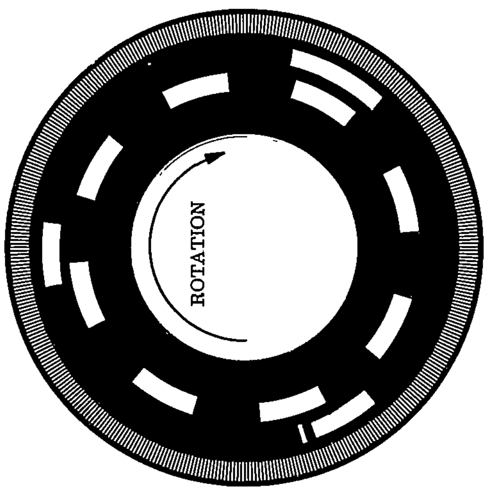
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
10017 107-12
SCANNER CAP MDA A4
REEL MDA A3
AST/24V A2
REGULATOR A1
POWER CHASSIS PARTIAL
MOTHER PWA
NC 60° C
POWER SUPPLY OVER TEMP.
SEE CONTROL SYSTEM BLOCK DIAGRAM
SYSTEM DATA BUS
SYSTEM ADDRESS BUS
BUS ENABLE
R/W
ADDRESS DECODE U85, 96
PWA DATA BUS
SEE REFERENCE PWA BLOCK DIAGRAM
COUNTER RESET
SCAN Ø
AND U44
COUNTER OUTPUT
GATE ARRAY I.C. U50
16 STAGE BINARY COUNTER U48, 49
PHASE LOCKED XTAL OR LC OSC.
REF COMP. SYNC
FIELD 1
REFERENCE
(SEE REFERENCE BLOCK DIAGRAM FOR DETAILS) A16
FROM COLOR FRAMER PWA AND MODULATOR REF. SELECT
ADDRESS DECODE U68, 79
BUS BUFF
SCANNER PHASE
COUNTER CENTER 128 (1µs RES.)
STOP COUNTER CONTROL/START
RECLOCK
U34 '16' FRAME SEQUENCE COUNTER
SCANNER STOPPED
SCANNER STALLED
SCANNER ON
SCANNER LOCKED
LATCH
U24 2 LINE DELAY
U25 15 LINE DELAY
U31-3 COMPARE
SERVO VERT.
U30 EDIT TACH Ø WINDOW (15µs)
COMPUTE
SCANNER RUN #1
CONTROL LOGIC U11, 20, 23
SCANNER STALL DETECT (1.5 SEC) U3, 29, 30
SCANNER STOP
SCANNER LOCK DETECT U12, 21
SCANNER "V" TACH.
RAMP GENERATOR
RAMP. RESET SW. U2
SAMPLE & HOLD U2, 10
POSITION LOOP RUN WINDOW U42
ERROR AMP U10
POSITION LOOP RUN CONTROL U12, 21
VCO U19
525: 24 KHz
625: 20 KHz
FROM CAPSTAN ASSY
CAPSTAN TACH
TACH PRESENT DETECTOR U15, 16
CAP STOPPED
TRI STATE U17
SCANNER RUNNING DETECT
SCANNER STOP DETECT
POWER FAIL
4 BIT SHIFT REG. U9
GATE U18
MONO U1 220µs
SYNC ERASE GATE
SYNC RECORD GATE
SCANNER HI FREQ. TACH
SCANNER VERT. TACH + SYNC HEAD GATE TIMING (ERASE + RECORD)
TACH 4 BIT BINARY DOWN COUNTER U52
"V" TACH
LOAD "O"
ADDER U51
"O" DETECT U28-13
"15" DETECT U40-13
REFERENCE 4 BIT BINARY UP COUNTER U53
CARRY IN
4 BIT D/A
ERROR AMPS U39
SERVO AMP U34
VOLTAGE REGULATOR U50
MONITOR
SHAFT RESON. FILTER
REEL AND SCANNER SERVO PWA
A14
POWER FAIL
SERVO POWER FAIL (AST/24V)
ISOSC GEN U9
REF +6.5V GEN U9
ERROR AMP U11
R121 ("O" BAL)
DRIVE THRESHOLD U7
DRIVE SHAPER U8
DRIVE SHAPER U6
SCANNER PULL UP DRIVER Q35, 36
SCANNER PULL DOWN DRIVER Q34
POWER FAIL CONTROL
MOTOR CURRENT FEEDBACK AMP U13
R115 (DIFF. BAL.)
CAPSTAN AND SCANNER MDA PWA
(SCANNER MDA ONLY)
POWER CHASSIS MOTHER PWA (PARTIAL) (SEE LEFT)
CURRENT SENSE & FILTER
FOR SCANNER TACH PICK UP ASSY
SCANNER TACH PICK UP ASSY
COMMUTATOR TACH
COMMUTATOR TACH Ø A
COMMUTATOR TACH Ø B
COMMUTATOR TACH Ø C
MOTOR TACH AMP PWA
TACH SHAPER
MOTOR COMMUTATOR DRIVER
MOTOR STOP CNTL
DRIVE LOGIC
PULL DOWN
PULL UP
MOTOR DRIVER ASSY.
SCANNER BRUSH LESS D.C. MOTOR
(8 POLE - 3 PHASE - "Y" WOUND)
VPR-3
SCANNER SERVO SYSTEM BLOCK DIAGRAM
10-3



VPR-3 A14-2
SCANNER/REEL SERVO
CONTROL LOGIC

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 2 3 4 5 6
10017 111-13



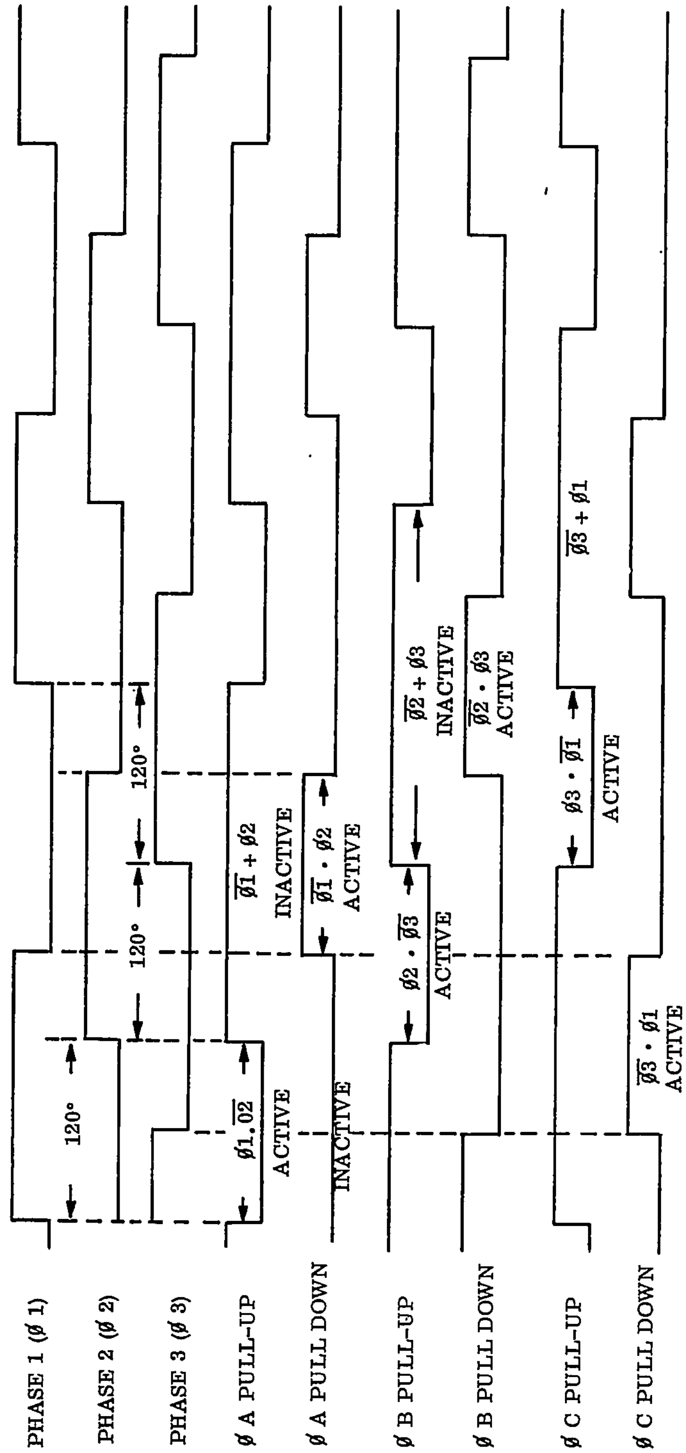


SCANNER TACH DISC

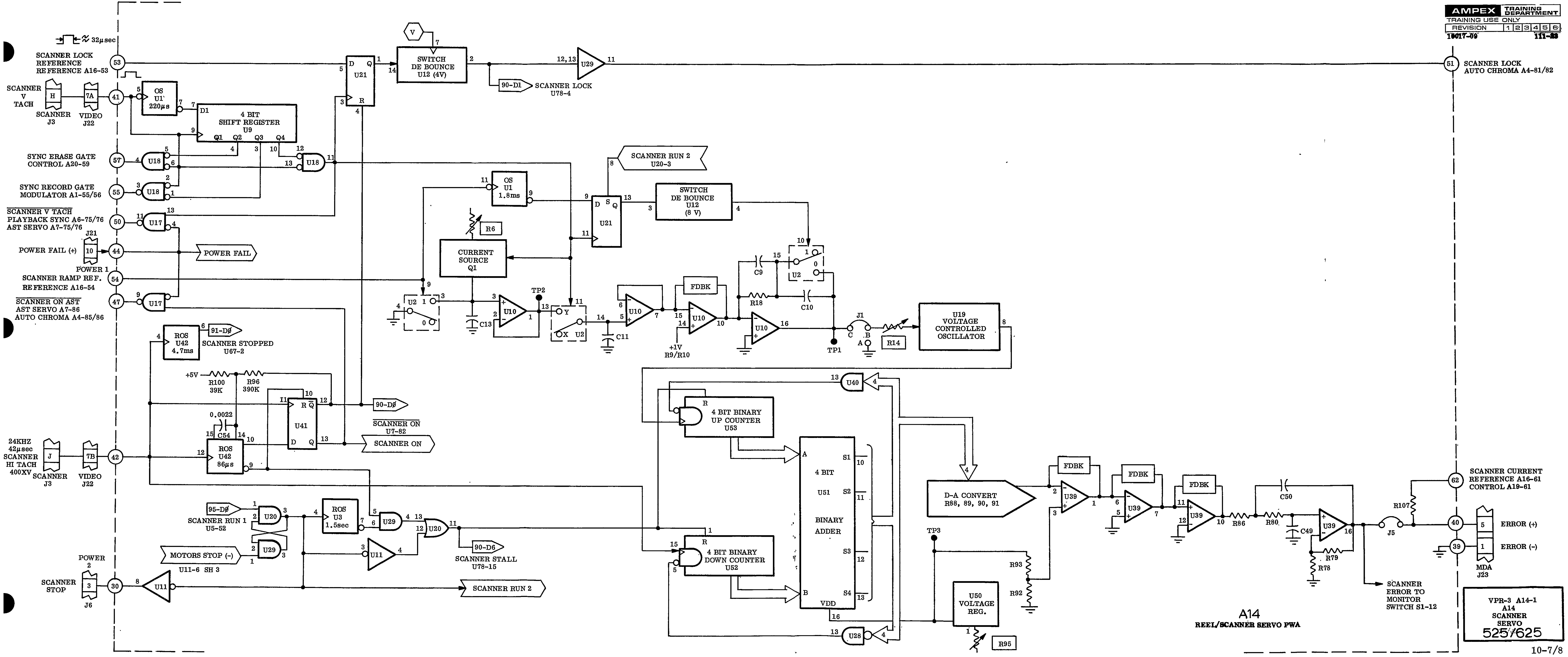
- DRAWING NOT TO SCALE

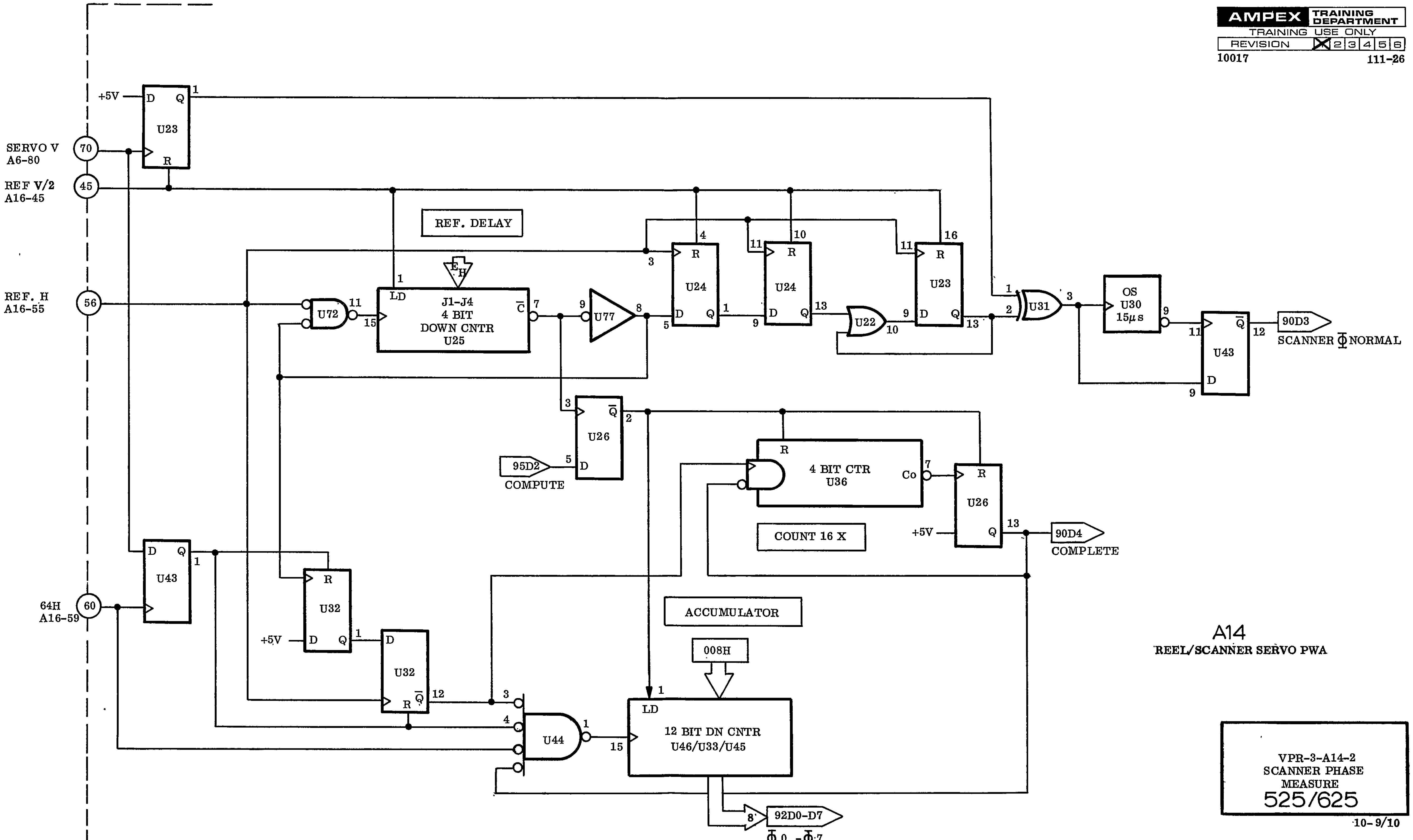
VPR-3 SCANNER SERVO
VERTICAL TACH PROCESSING

525/625

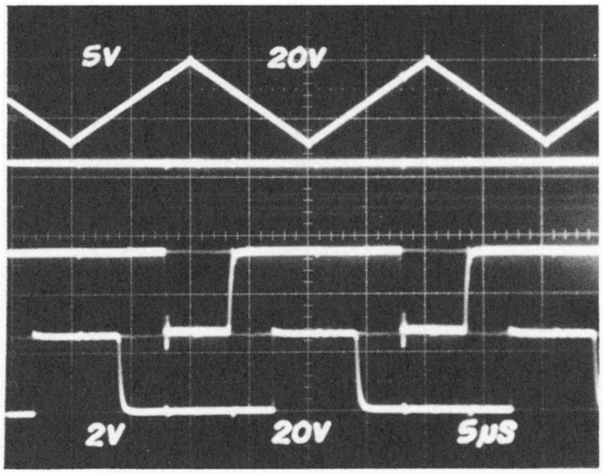


VPR 3 SCANNER MOTOR TIMING DIAGRAM, BRUSHLESS MOTOR COMMUTATION (SCHEMATIC 1468633)


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
SCANNER LOCK REFERENCE REFERENCE A16-53
SCANNER V TACH
SCANNER J3
VIDEO J22
4 BIT SHIFT REGISTER U9
SWITCH DE BOUNCE U12 (4V)
SCANNER LOCK U78-4
SCANNER LOCK AUTO CHROMA A4-81/82
SYNC ERASE GATE CONTROL A20-59
SYNC RECORD GATE MODULATOR A1-55/56
SCANNER V TACH PLAYBACK SYNC A6-75/76 AST SERVO A7-75/76
POWER FAIL (+)
POWER 1
POWER FAIL
SCANNER RAMP REF. REFERENCE A16-54
SCANNER ON AST AST SERVO A7-86 AUTO CHROMA A4-85/86
SCANNER RUN 2 U20-3
SWITCH DE BOUNCE U12 (8 V)
CURRENT SOURCE Q1
U19 VOLTAGE CONTROLLED OSCILLATOR
ROS U42 4.7ms
SCANNER STOPPED U67-2
SCANNER ON U7-82
SCANNER ON
24KHZ 42µsec SCANNER HI TACH 400XV
4 BIT BINARY UP COUNTER U53
4 BIT U51 BINARY ADDER
D-A CONVERT R88, 89, 90, 91
SCANNER CURRENT REFERENCE A16-61 CONTROL A19-61
ERROR (+)
ERROR (-)
MDA J23
SCANNER RUN 1 U5-52
MOTORS STOP (-)
U11-6 SH 3
SCANNER STALL U78-15
4 BIT BINARY DOWN COUNTER U52
POWER 2
SCANNER STOP
SCANNER RUN 2
U50 VOLTAGE REG.
SCANNER ERROR TO MONITOR SWITCH S1-12
A14
REEL/SCANNER SERVO PWA
VPR-3 A14-1 A14 SCANNER SERVO
525/625



AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 2 3 4 5 6
10017
111-26
SERVO V A6-80
REF V/2 A16-45
REF. H A16-55
64H A16-59
REF. DELAY
J1-J4 4 BIT DOWN CNTR U25
COUNT 16 X
4 BIT CTR U36
OS U30 15μs
SCANNER Φ NORMAL
95D2 COMPUTE
90D3
90D4 COMPLETE
ACCUMULATOR
008H
12 BIT DN CNTR U46/U33/U45
92D0-D7
Φ0 - Φ7
A14
REEL/SCANNER SERVO PWA
VPR-3-A14-2
SCANNER PHASE MEASURE
525/625
10-9/10

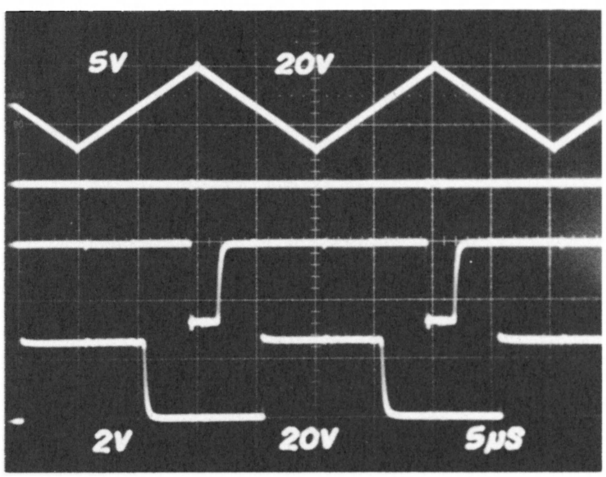


WF1 TP3: Reference Ramp

WF2 TP6: Scanner Error +8.4 V DC

WF3 TP9: Pull up driver

WF4 TP8: Pull down driver
Scanner coming up to
READY speed

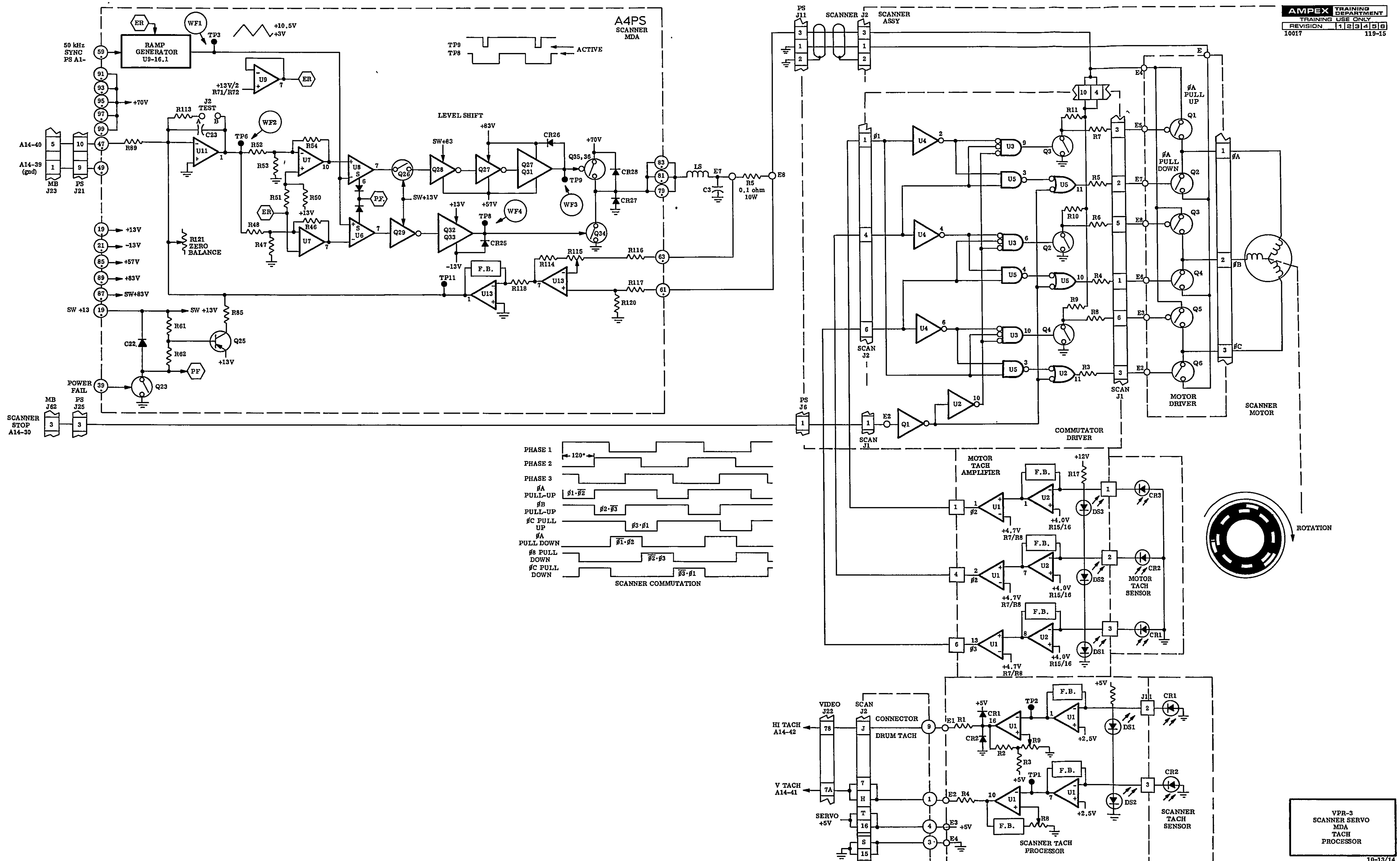


WF1 TP3: Reference Ramp

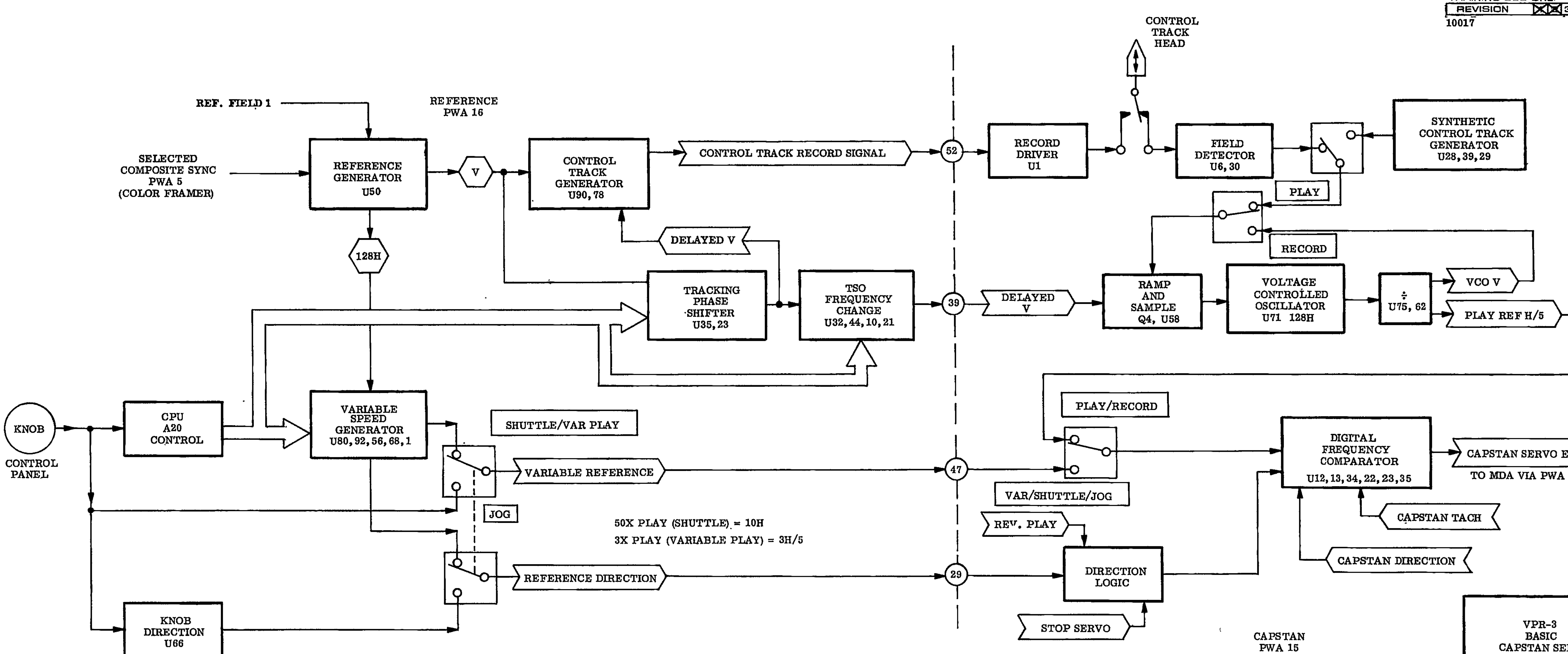
WF2 TP6: Scanner error +7.75 V DC

WF3 TP9: Pull Up drive

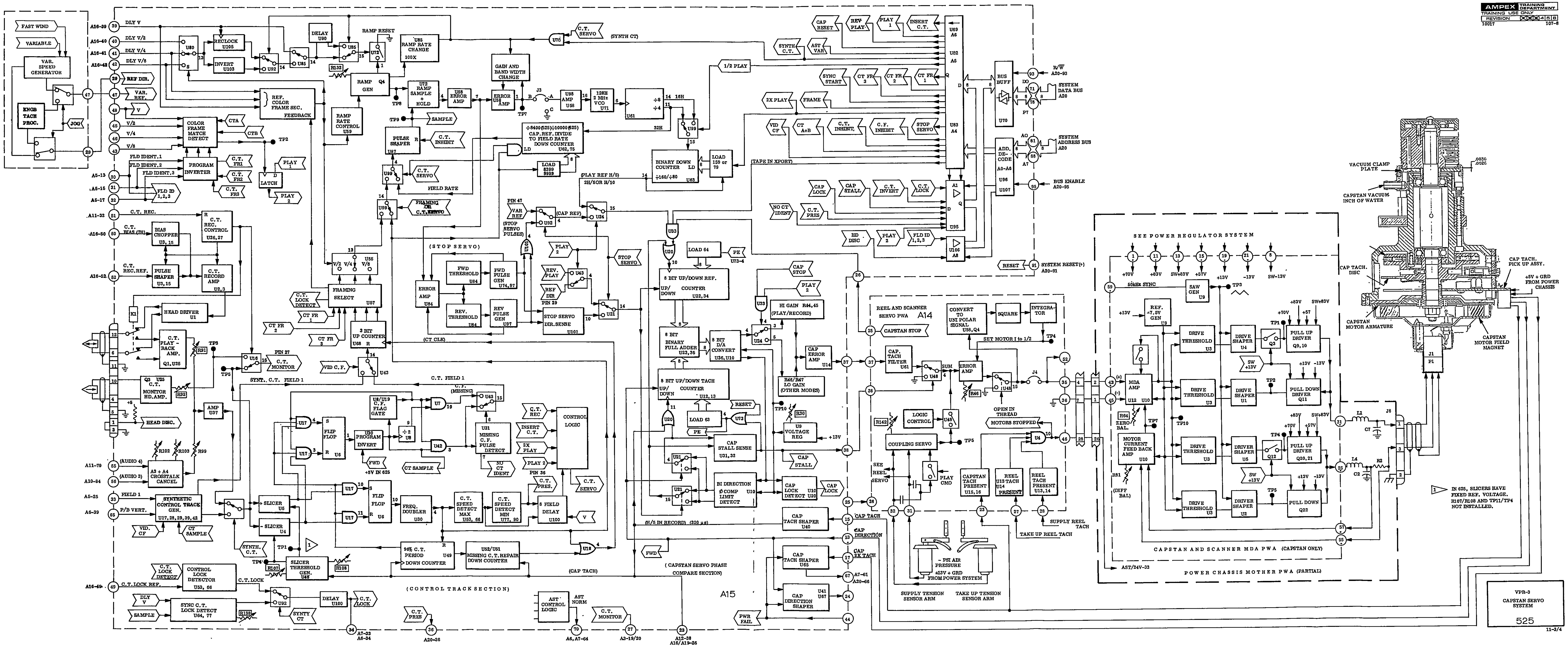
WF4 TP8: Pull down Drive
VPR-3 in normal PLAY



VPR-3
SCANNER SERVO
MDA
TACH
PROCESSOR



VPR-3 BASIC CAPSTAN SERVO



AMPEX TRAINING DEPARTMENT
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REVISION
10217
107-8
FAST WIND
VARIABLE
VAR. SPEED GENERATOR
KNOB TACH PROC.
JOG
REF. COLOR FRAME SEC.
FEEDBACK
COLOR FRAME MATCH DETECT
PROGRAM INVERTER
RECLOCK U105
INVERT U103
DELAY U90
RAMP RESET
U85 RAMP RATE CHANGE 100X
RAMP GEN
RAMP RATE CONTROL U59
U72 RAMP SAMPLE + HOLD
U58 ERROR AMP
GAIN AND BAND WIDTH CHANGE
ERROR U58 AMP
U98 AMP U58
128H 2 MHz VCO U71
1/2 PLAY
PULSE SHAPER U87
LATCH
(SYNTH CT)
C.T. SERVO
C.T. INHIBIT
FIELD RATE
BINARY DOWN COUNTER
(TAPE IN XPORT)
(PLAY REF H/S)
(STOP SERVO)
FWD THRESHOLD U84
FWD PULSE GEN U74, 97
REV. THRESHOLD U84
REV PULSE GEN U97
ERROR AMP U84
STOP SERVO DIR. SENSE U101
FRAMING SELECT U57
3 BIT UP COUNTER U68
(CT CLK)
C.T. REC.
BIAS CHOPPER U3, 15
C.T. REC. CONTROL U26, 27
PULSE SHAPER U3, 15
C.T. RECORD AMP U2, 3
HEAD DRIVER U1
C.T. PLAY-BACK AMP. Q1, U25
C.T. MONITOR
C.T. MONITOR HD. AMP.
AMP U37
HEAD DISC.
A3 + A4 CROSSTALK CANCEL
SYNTHETIC CONTROL TRACK GEN. U17, 28, 29, 39, 42
SLICER U5
SLICER U4
SLICER THRESHOLD GEN. U45
FLIP FLOP U6
U30 PROGRAM INVERT
U8/U19 C.F. FLAG GATE
U31 MISSING C.F. PULSE DETECT
CONTROL LOGIC
CT SAMPLE
FREQ. DOUBLER U30
C.T. SPEED DETECT MAX U53, 66
C.T. SPEED DETECT MIN U77, 90
8 FIELD DELAY U100
96% C.T. PERIOD DOWN COUNTER U49
U52/U51 MISSING C.T. REPAIR DOWN COUNTER
(CAP TACH)
C.T. LOCK DETECT
CONTROL LOCK DETECTOR U53, 66
C.T. LOCK REF.
SYNC C.T. LOCK DETECT U64, 77
DELAY U100
C.T. LOCK
(CONTROL TRACK SECTION)
AST CONTROL LOGIC
AST NORM
C.T. MONITOR
A15
PWR FAIL
8 BIT UP/DOWN REF. COUNTER U22, 34
8 BIT BINARY FULL ADDER U23, 35
8 BIT D/A CONVERT U36, U10
8 BIT UP/DOWN TACH COUNTER U12, 13
HI GAIN R44, 45 (PLAY/RECORD)
R46/R47 LO GAIN (OTHER MODES)
CAP ERROR AMP U14
U9 VOLTAGE REG
CAP STALL SENSE U31, 32
BI DIRECTION Ø COMP LIMIT DETECT U10
CAP LOCK DETECT U20
CAP TACH SHAPER U40
CAP TACH SHAPER U65
CAP DIRECTION SHAPER U41 U67
(CAPSTAN SERVO PHASE COMPARE SECTION)
REEL AND SCANNER SERVO PWA A14
CAPSTAN STOP
CAP. TACH FILTER U61
CONVERT TO UNI POLAR SIGNAL U58, Q4
SQUARE
INTEGRATOR
SET MOTOR I to 1/2
ERROR AMP
LOGIC CONTROL
COUPLING SERVO
MOTORS STOPPED
CAPSTAN TACH PRESENT U15, 16
REEL U13 TACH U14 PRESENT
REEL TACH PRESENT U13, 14
SUPPLY REEL TACH
TAKE UP REEL TACH
SUPPLY TENSION SENSOR ARM
TAKE UP TENSION SENSOR ARM
+13V + GRD FROM POWER SYSTEM
SEE POWER REGULATOR SYSTEM
50kHz SYNC
SAW GEN U9
REF. +7.5V GEN U9
MDA AMP U12 U10
MOTOR CURRENT FEED BACK AMP U10
DRIVE THRESHOLD U3
DRIVE SHAPER U3
DRIVE SHAPER U1
DRIVER SHAPER U5
DRIVER SHAPER U2
PULL UP DRIVER Q9, 10
PULL DOWN DRIVER Q11
PULL UP DRIVER Q20, 21
PULL DOWN Q22
CAPSTAN AND SCANNER MDA PWA (CAPSTAN ONLY)
POWER CHASSIS MOTHER PWA (PARTIAL)
VACUUM CLAMP PLATE
CAPSTAN VACUUM INCH OF WATER
CAP TACH. DISC
CAPSTAN MOTOR ARMATURE
CAPSTAN MOTOR FIELD MAGNET
CAP TACH. PICK UP ASSY.
+5V + GRD FROM POWER CHASSIS
SYSTEM DATA BUS A20
SYSTEM ADDRESS BUS A20
BUS ENABLE A20-95
SYSTEM RESET(+) A20-91
BUS BUFF U70
ADD. DE-CODE A0-A6 U96 U107
IN 625, SLICERS HAVE FIXED REF. VOLTAGE. R107/R108 AND TP11/TP4 NOT INSTALLED.
VPR-3 CAPSTAN SERVO SYSTEM
525
11-3/4

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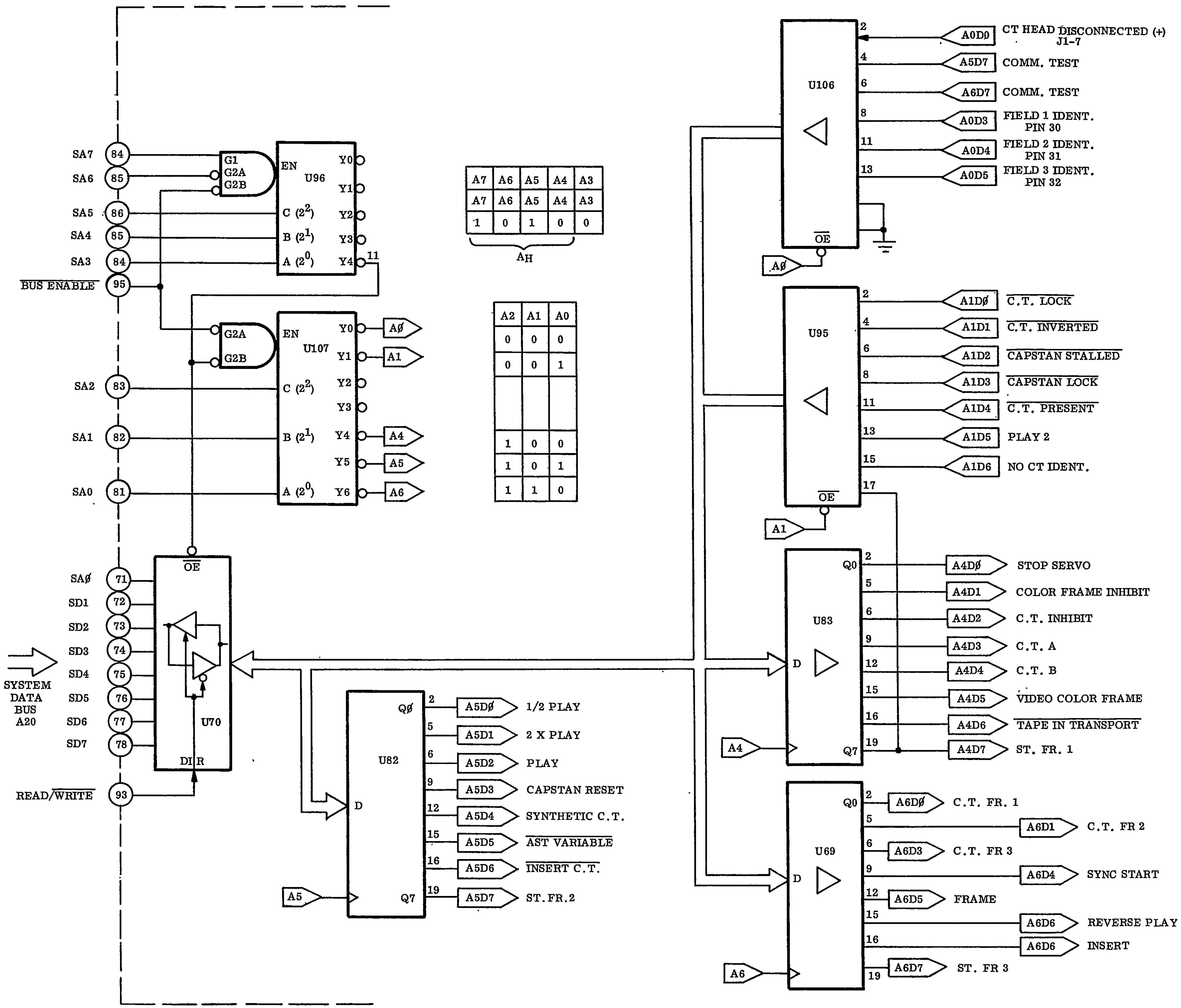
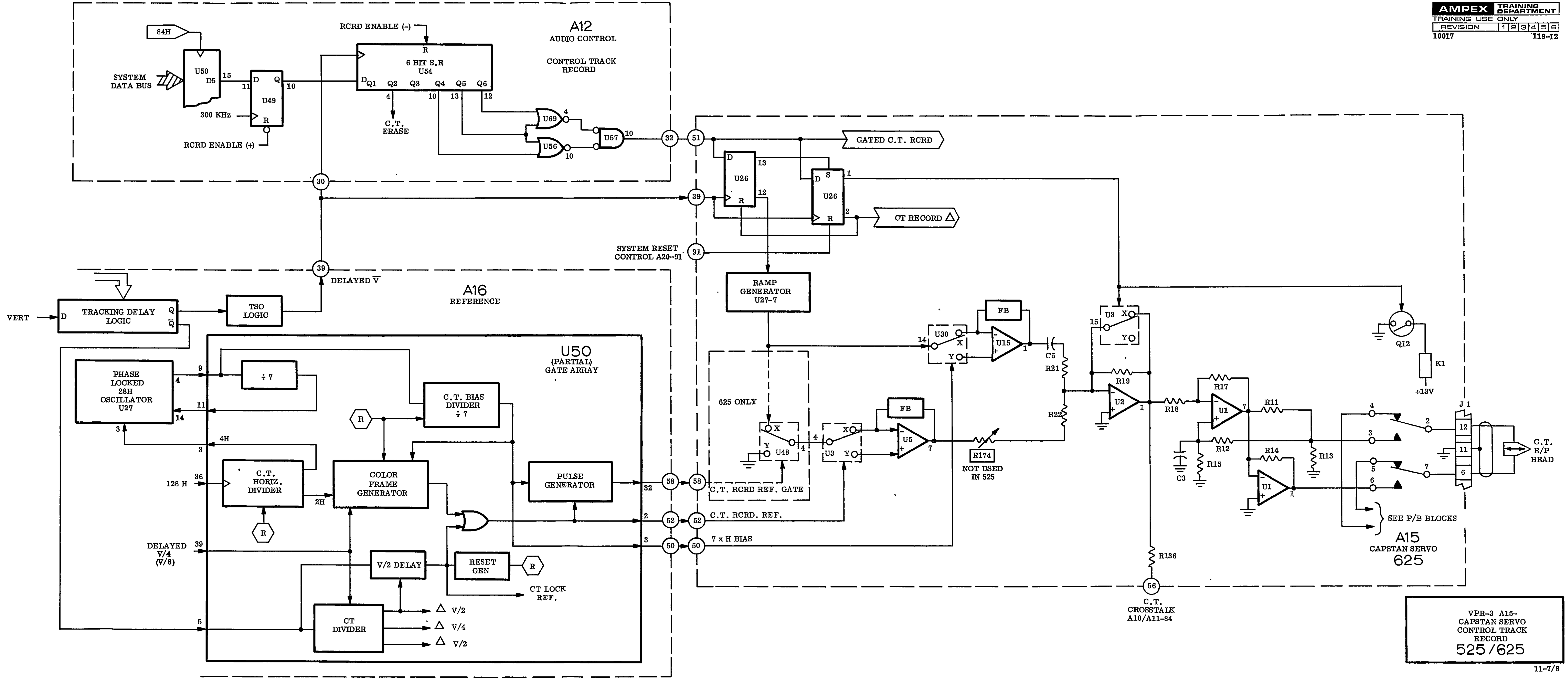
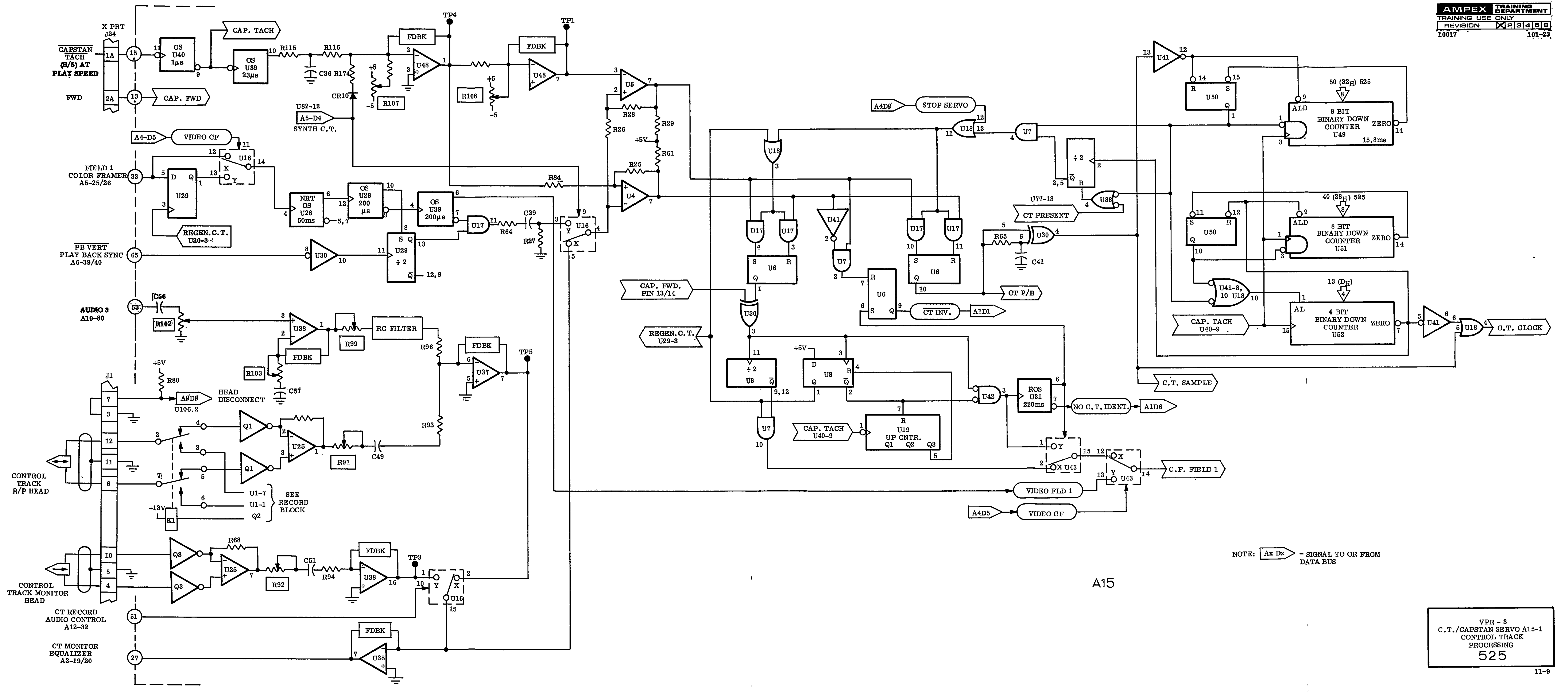
10017 119-10

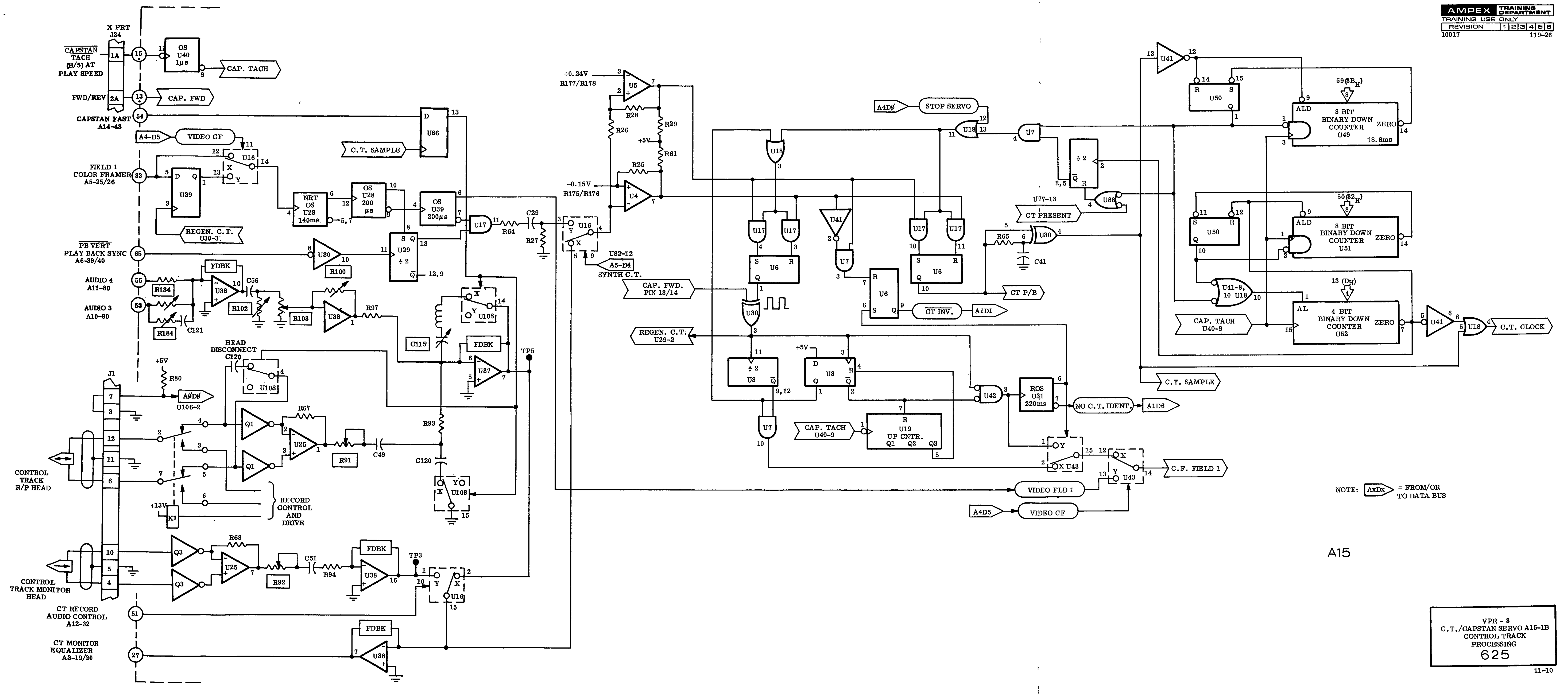


VPR-3 A15-Ø
C.T./CAPSTAN SERVO
SYSTEM CONTROL
525/625



VPR-3 A15-
CAPSTAN SERVO
CONTROL TRACK
RECORD
525/625

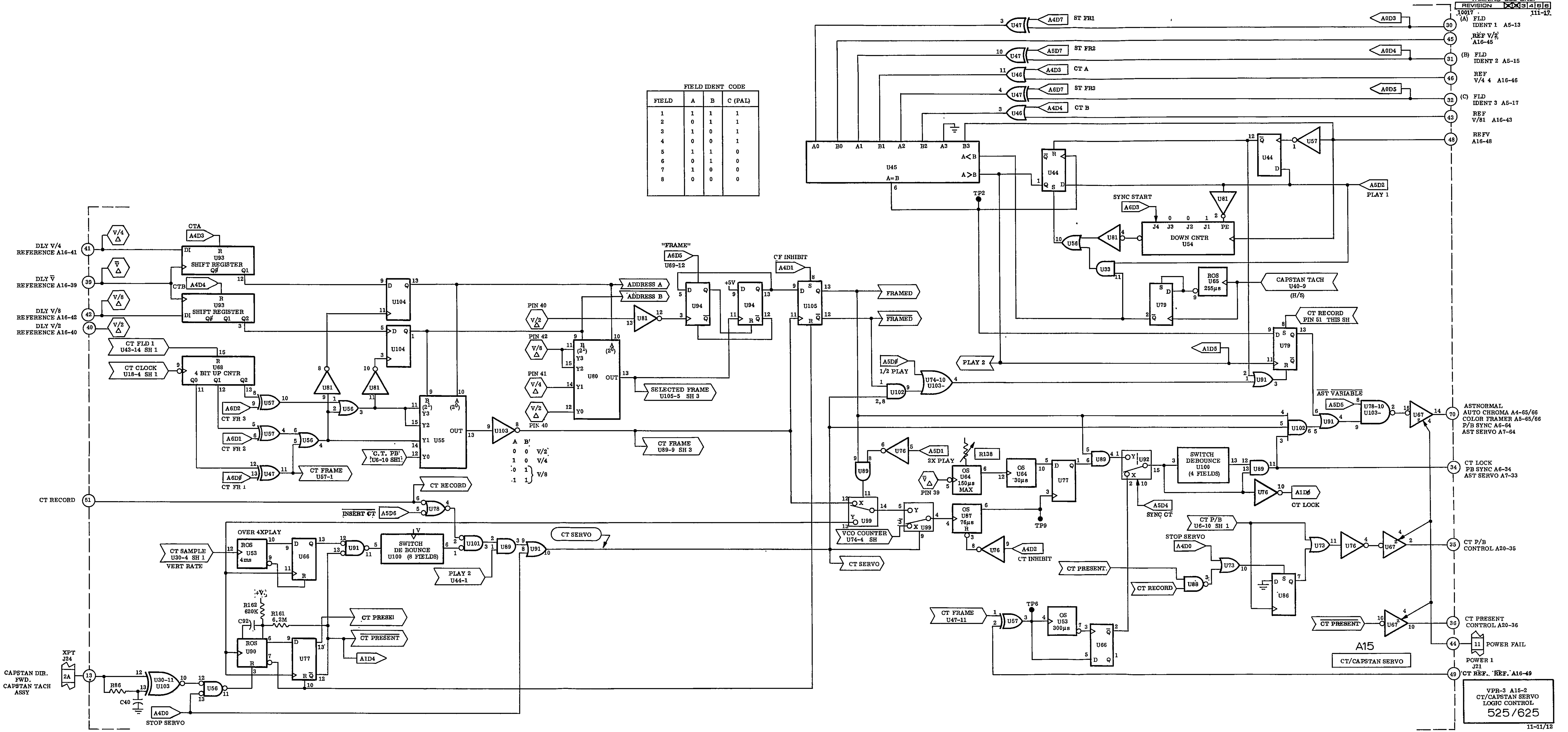

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 2 3 4 5 6
10017
101-23
X PRT J24
CAPSTAN TACH (H/5) AT PLAY SPEED
FWD
CAP. TACH
CAP. FWD
OS U40 1µs
OS U39 23µs
R115
R116
C36
R174
CR10
U82-12
A5-D4
SYNTH C.T.
TP4
TP1
FDBK
U48
R107
R108
U5
R28
R26
R29
+5V
R61
R25
R84
U4
A4-D5
VIDEO CF
FIELD 1 COLOR FRAMER A5-25/26
U29
U16
REGEN. C.T. U30-3
NRT OS U28 50ms
OS U28 200 µs
OS U39 200µs
U17
R64
C29
R27
PB VERT PLAY BACK SYNC A6-39/40
U30
÷ 2
AUDIO 3 A10-80
C56
R102
U38
R99
RC FILTER
R96
R103
C57
U37
TP5
J1
+5V
R80
AØDØ
U106.2
HEAD DISCONNECT
Q1
U25
R91
C49
R93
CONTROL TRACK R/P HEAD
U1-7
U1-1
Q2
SEE RECORD BLOCK
+13V
K1
R68
Q3
R92
C51
R94
TP3
CONTROL TRACK MONITOR HEAD
CT RECORD AUDIO CONTROL A12-32
CT MONITOR EQUALIZER A3-19/20
A4DØ
STOP SERVO
U18
U7
U17
U41
U6
CAP. FWD. PIN 13/14
REGEN. C.T. U29-3
U8
CAP. TACH U40-9
R U19 UP CNTR. Q1 Q2 Q3
U42
ROS U31 220ms
NO C.T. IDENT.
A1D6
U77-13
CT PRESENT
U88
R65
C41
CT P/B
CT INV.
A1D1
U43
C.F. FIELD 1
VIDEO FLD 1
A4D5
VIDEO CF
U50
50 (32H) 525
8 BIT BINARY DOWN COUNTER U49
ALD
ZERO
15.8ms
40 (28H) 525
8 BIT BINARY DOWN COUNTER U51
13 (DH)
U41-8, 10 U18
CAP. TACH U40-9
AL
4 BIT BINARY DOWN COUNTER U52
C.T. CLOCK
C.T. SAMPLE
NOTE: Ax Dx = SIGNAL TO OR FROM DATA BUS
A15
VPR - 3
C.T./CAPSTAN SERVO A15-1
CONTROL TRACK PROCESSING
525
11-9



VPR - 3
C.T./CAPSTAN SERVO A15-1B
CONTROL TRACK
PROCESSING
625

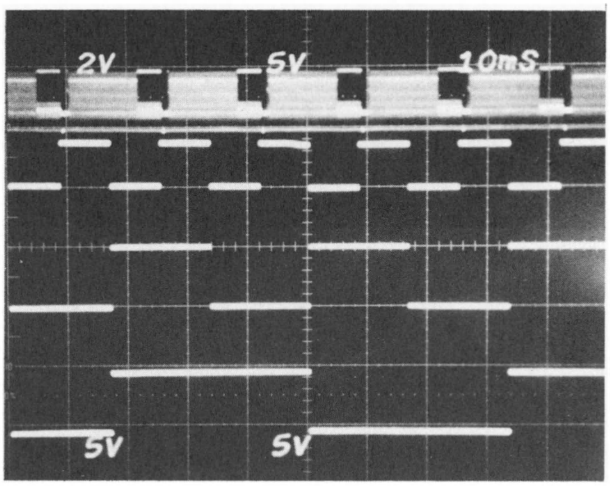
FIELD IDENT CODE

FIELD	A	B	C (PAL)
1	1	1	1
2	0	1	1
3	1	0	1
4	0	0	1
5	1	1	0
6	0	1	0
7	1	0	0
8	0	0	0



VPR-3 A15-2
CT/CAPSTAN SERVO
LOGIC CONTROL
525/625

VPR-3 CAPSTAN SERVO

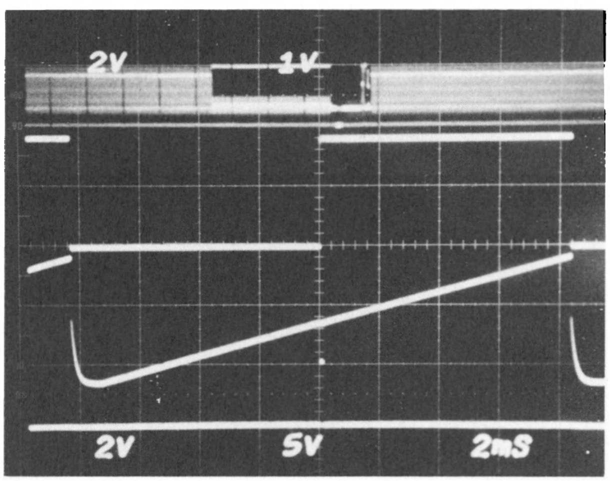


Ref Video in

WF1 PIN 39: Delayed "V"

WF2 PIN 40: Delayed "V/2"

WF3 PIN 41: Delayed "V/4"
VPR-3 in STOP/EE

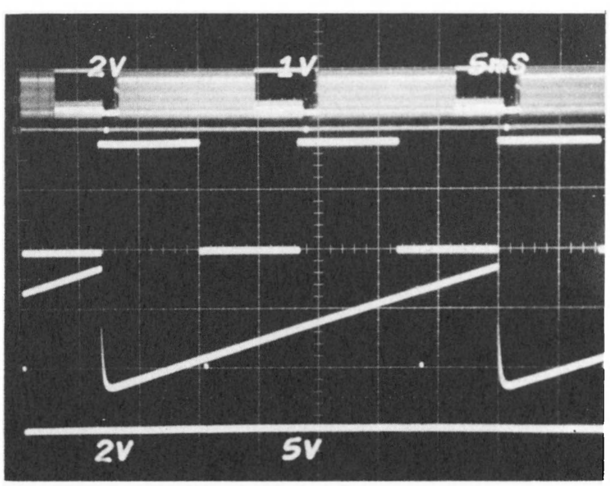


Ref Video in

WF1 PIN 39: Delayed "V"

WF2 TP8: "Ramp"

WF3 TP9: Sample
VPR-3 in STOP/EE

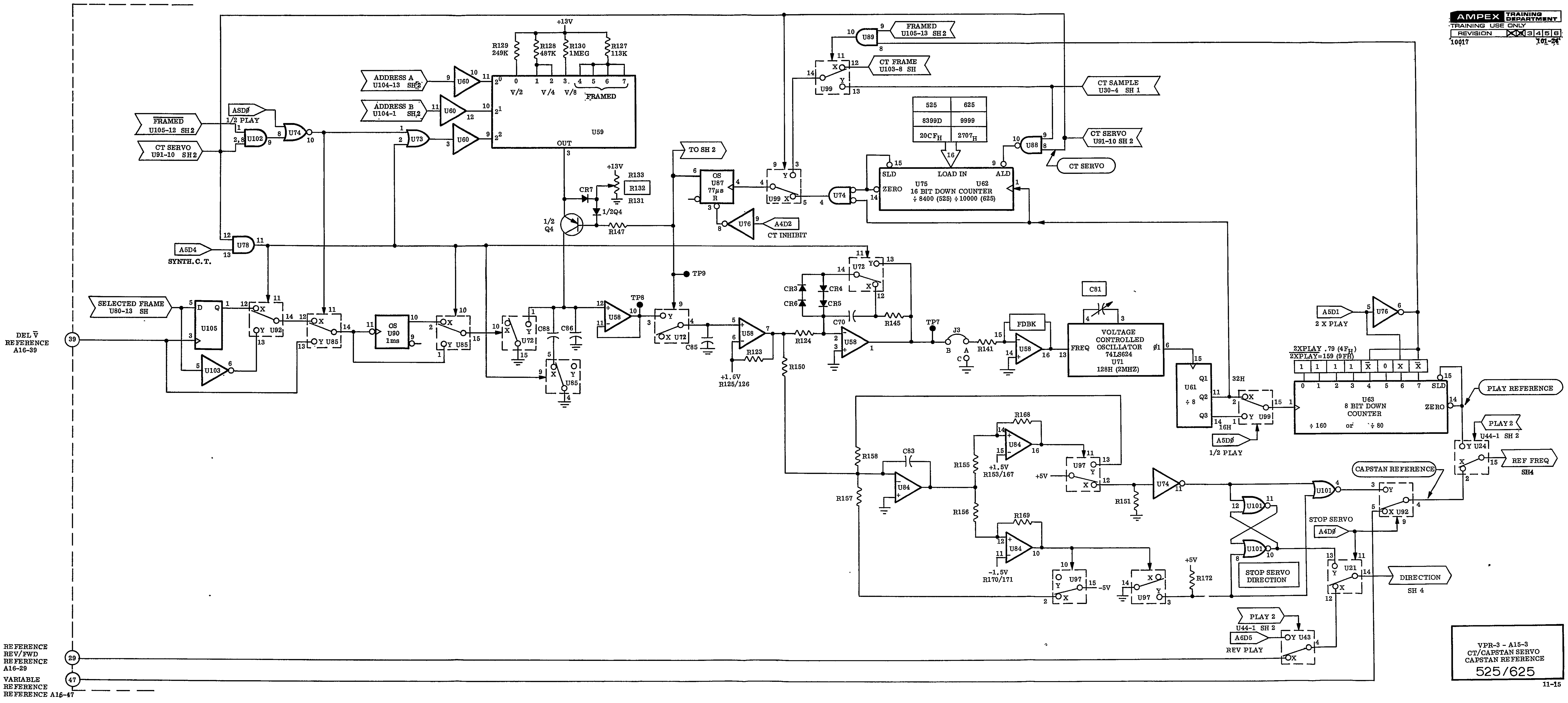


Ref Video in

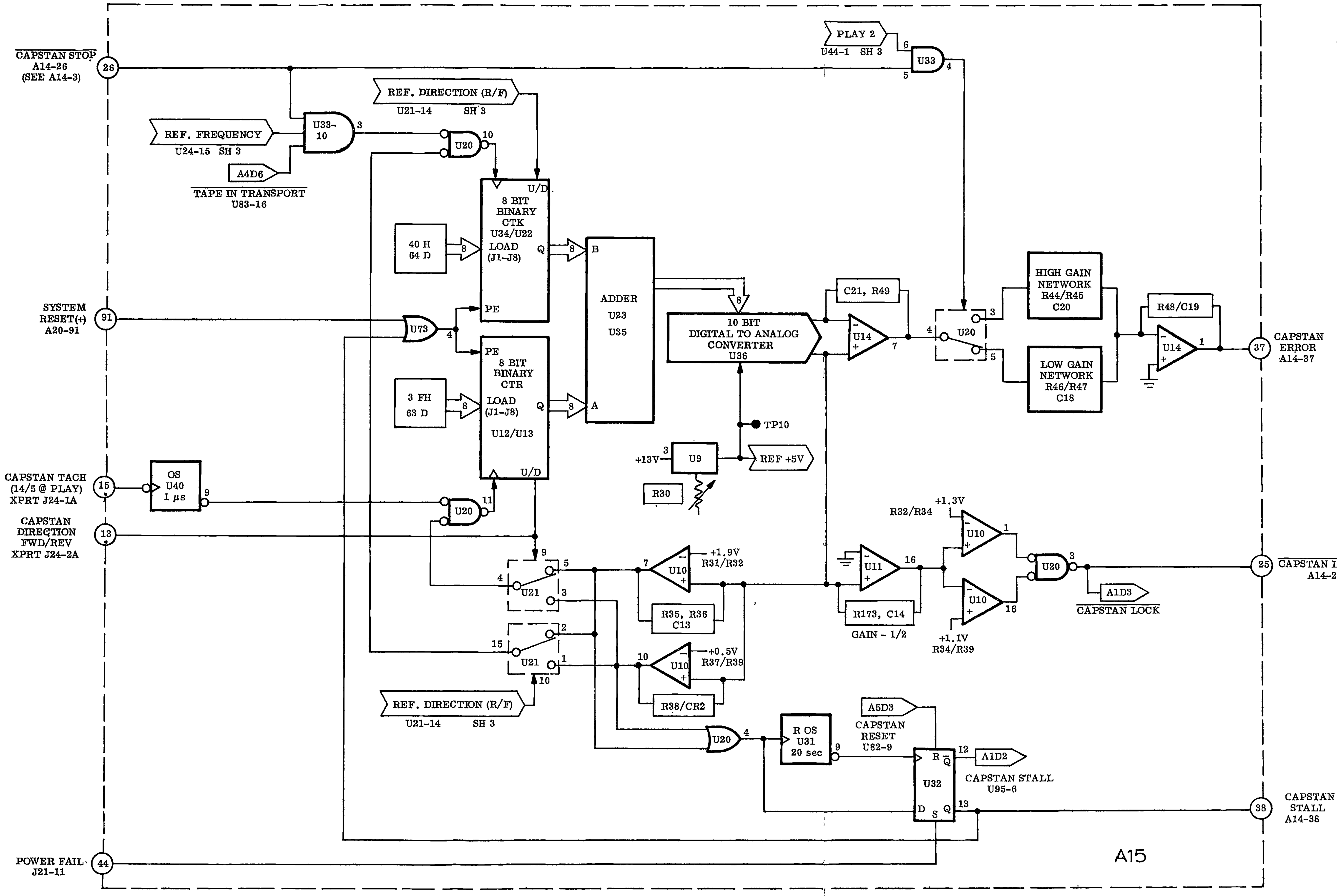
WF1 PIN 39: Delayed "V"

WF2 TP8: "Ramp"

WF3 TP9: Sample
VPR-3 in 1/2 Speed/C.T.
Locked Play



VPR-3 - A15-3
CT/CAPSTAN SERVO
CAPSTAN REFERENCE
525/625



VPR-3 A15-4
CAPSTAN SERVO
CAPSTAN ERROR

AMPEX TRAINING DEPARTMENT
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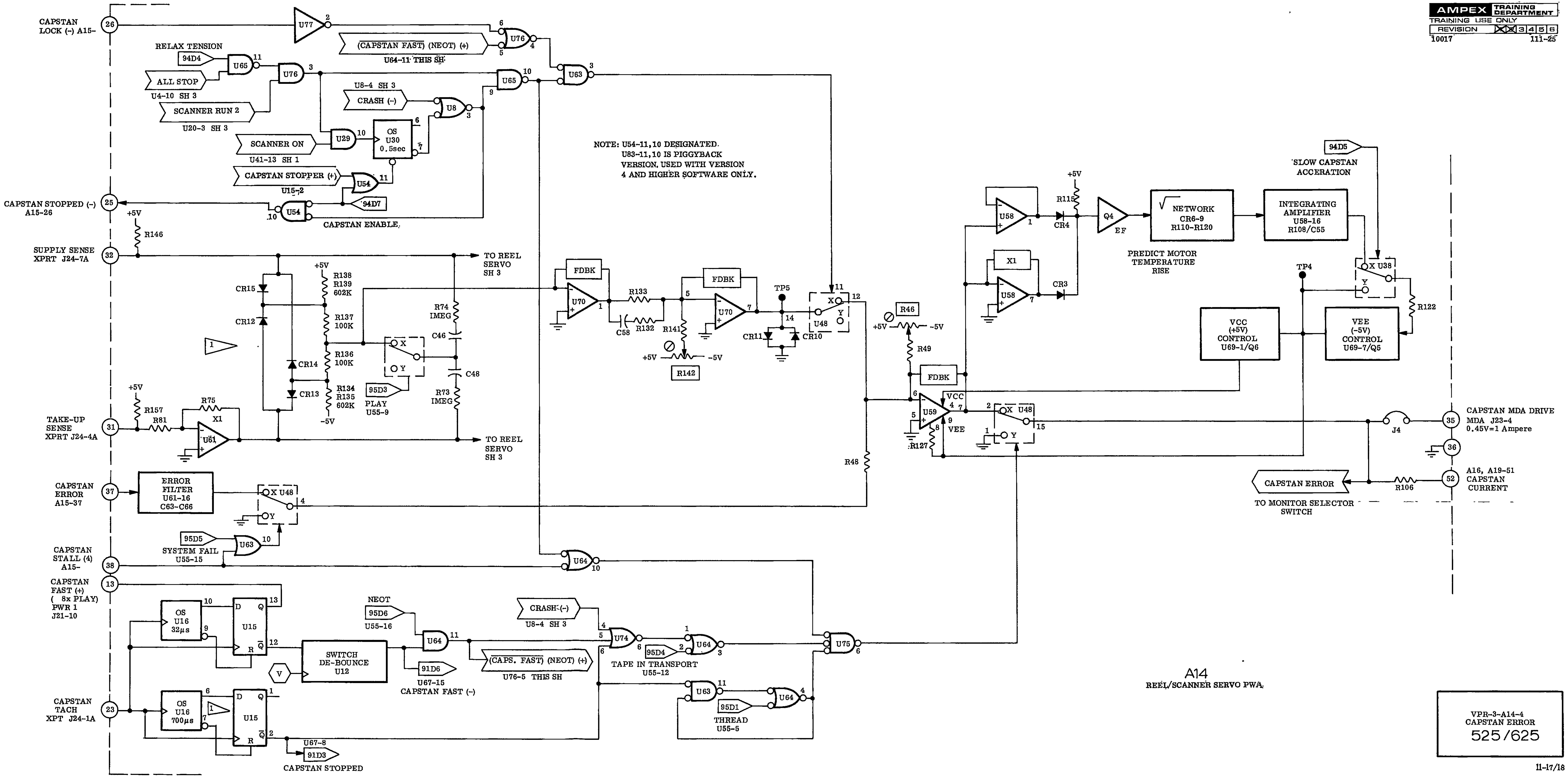
10017 111-25

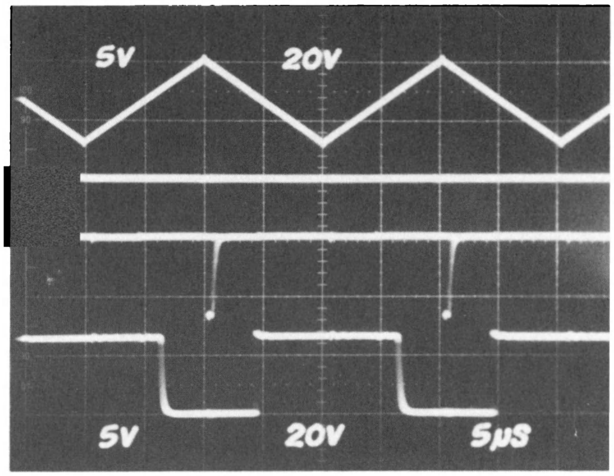


A14
REEL/SCANNER SERVO PWA

VPR-3-A14-4
CAPSTAN ERROR
525/625

11-17/18

VPR-3 CAPSTAN MDA

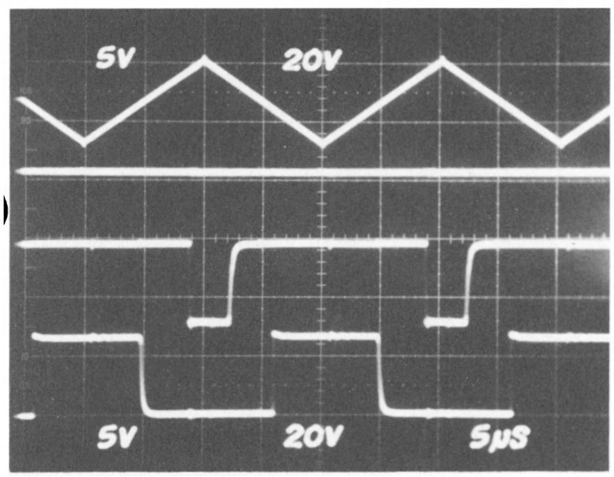


WF1 TP3 REFERENCE RAMP

WF2 TP10 CAPSTAN ERROR +7V DC

WF3 TP4 PULL UP DRIVE

WF4 TP5 PULL-DOWN DRIVE
NORMAL PLAY

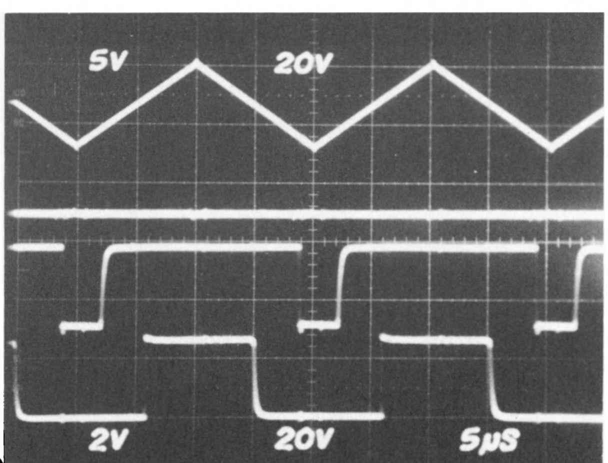


WF1 TP3 REFERENCE RAMP

WF2 TP10 CAPSTAN ERROR +8V DC

WF3 TP4 PULL UP DRIVE

WF4 TP5 PULL DOWN DRIVE
500 ips FORWARD SHUTTLE

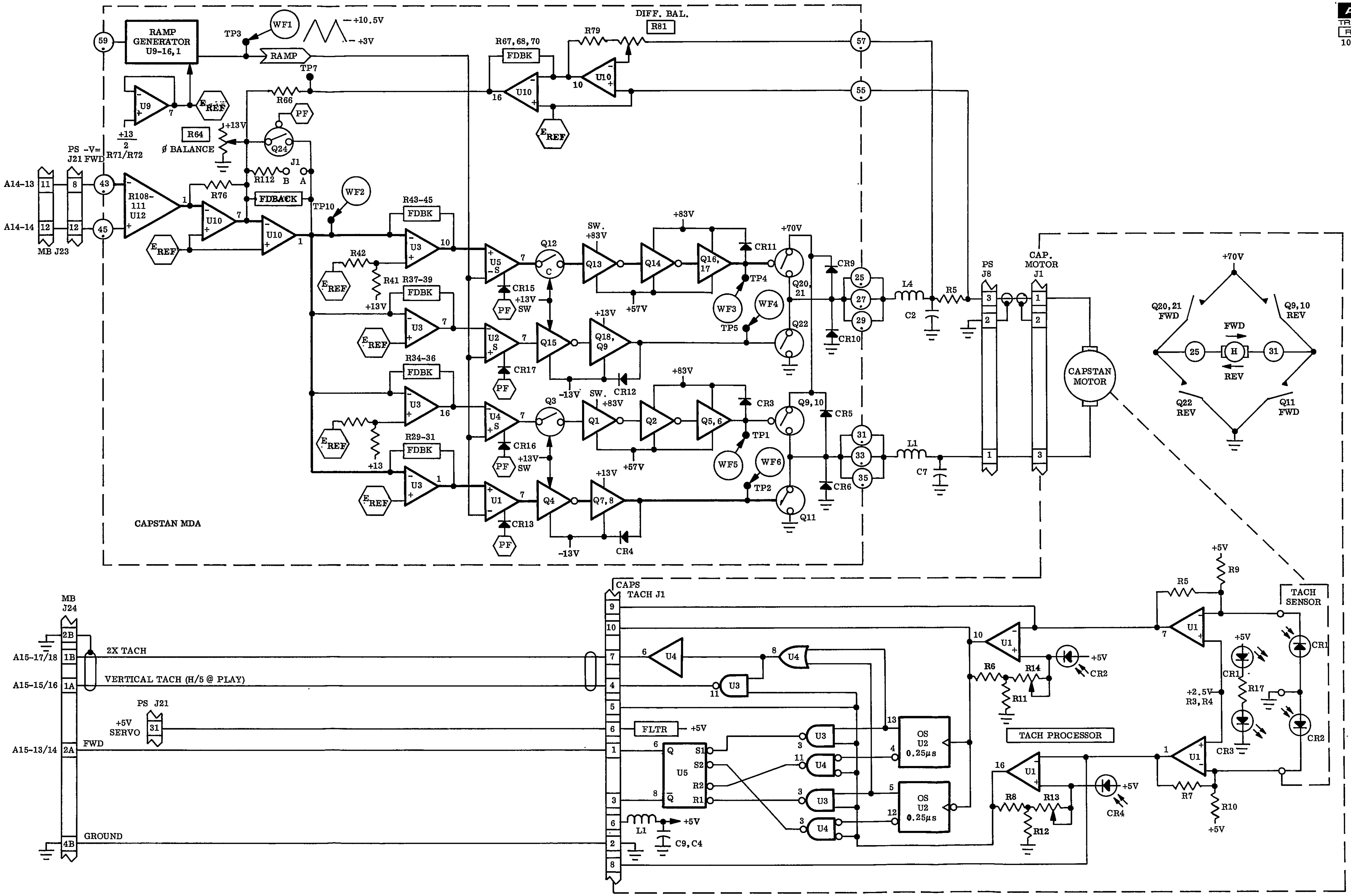


WF1 TP3 REFERENCE RAMP

WF2 TP10 CAPSTAN ERROR +4.8V DC

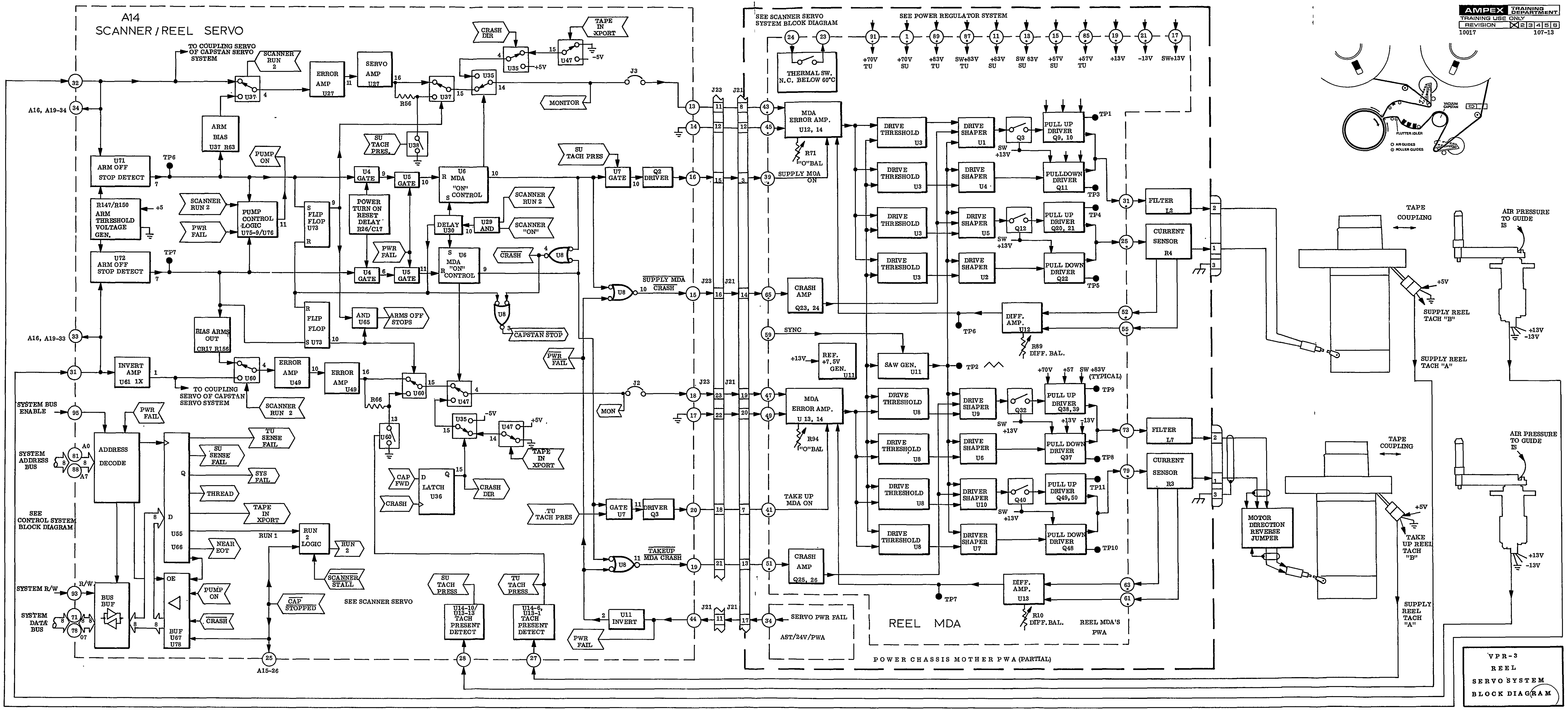
WF5 TP1 PULL UP DRIVE

WF6 TP2 PULL DOWN DRIVE



VPR-3
CAPSTAN SERVO
MDA
TACH PROCESSOR

11-21/22


AMPEX TRAINING DEPARTMENT
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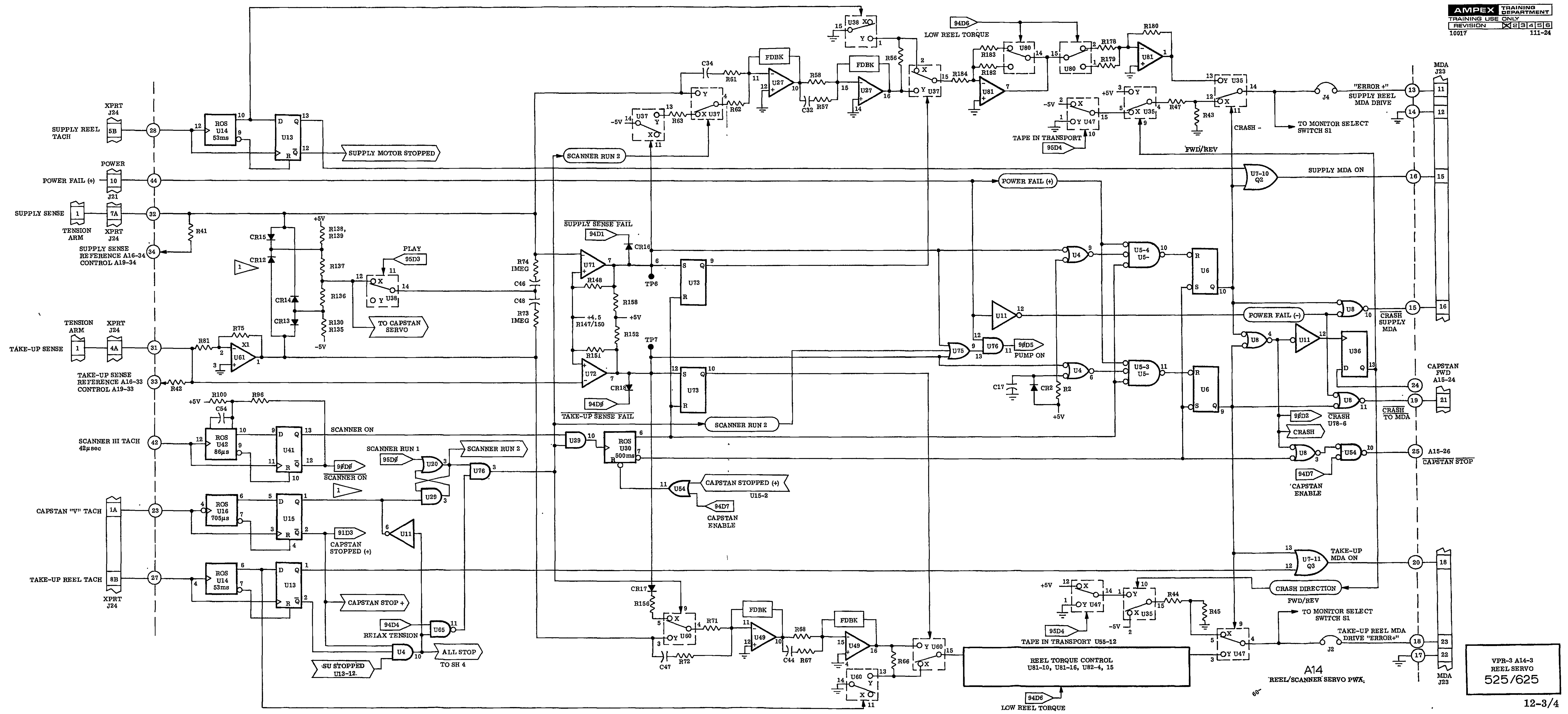
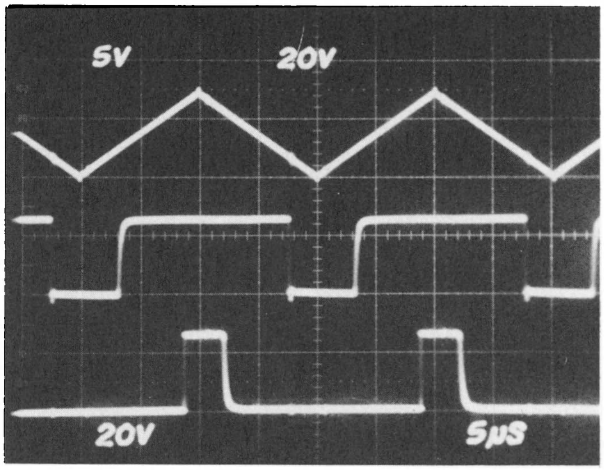
10017
107-13
A14
SCANNER / REEL SERVO
TO COUPLING SERVO OF CAPSTAN SERVO SYSTEM
SCANNER RUN 2
ERROR AMP U27
SERVO AMP U27
CRASH DIR
TAPE IN XPORT
MONITOR
A16, A19-34
A16, A19-33
U71 ARM OFF STOP DETECT
U72 ARM OFF STOP DETECT
R147/R150 ARM THRESHOLD VOLTAGE GEN.
ARM BIAS U37 R63
PUMP ON
PUMP CONTROL LOGIC U75-9/U76
SCANNER RUN 2
PWR FAIL
S FLIP FLOP U73
R FLIP FLOP S U73
SU TACH PRES.
POWER TURN ON RESET DELAY R26/C17
U6 MDA "ON" CONTROL
DELAY U30
U29 AND
SCANNER RUN 2
SCANNER "ON"
SU TACH PRES
U7 GATE
Q2 DRIVER
CRASH
SUPPLY MDA CRASH
TAKEUP MDA CRASH
CAPSTAN STOP
AND U65
ARMS OFF STOPS
BIAS ARMS OUT CR17 R156
INVERT AMP U61 1X
TO COUPLING SERVO OF CAPSTAN SERVO SYSTEM
ERROR AMP U49
SCANNER RUN 2
MON
SYSTEM BUS ENABLE
SYSTEM ADDRESS BUS
ADDRESS DECODE
TU SENSE FAIL
SU SENSE FAIL
SYS FAIL
THREAD
TAPE IN XPORT
NEAR EOT
RUN 2 LOGIC
RUN 2
SCANNER STALL
SEE CONTROL SYSTEM BLOCK DIAGRAM
SYSTEM R/W
SYSTEM DATA BUS
BUS BUF
BUF U67 U78
CAP STOPPED
SEE SCANNER SERVO
CAP FWD
LATCH U36
CRASH DIR
.TU TACH PRES
GATE U7
DRIVER Q3
SU TACH PRESS
TU TACH PRESS
U14-10/U13-13 TACH PRESENT DETECT
U14-6, U13-1 TACH PRESENT DETECT
U11 INVERT
PWR FAIL
A15-26
SEE SCANNER SERVO SYSTEM BLOCK DIAGRAM
SEE POWER REGULATOR SYSTEM
THERMAL SW. N.C. BELOW 60°C
+70V TU
+70V SU
+83V TU
SW+83V TU
+83V SU
SW 83V SU
+57V SU
+57V TU
+13V
-13V
SW+13V
MDA ERROR AMP. U12, 14
R71 "O" BAL
SUPPLY MDA ON
CRASH AMP Q23, 24
SYNC
REF. +7.5V GEN. U11
SAW GEN. U11
MDA ERROR AMP. U 13, 14
R94 "O" BAL
TAKE UP MDA ON
CRASH AMP Q25, 26
SERVO PWR FAIL
AST/24V/PWA
REEL MDA
DRIVE THRESHOLD U3
DRIVE THRESHOLD U8
DRIVE SHAPER U1
DRIVE SHAPER U4
DRIVE SHAPER U5
DRIVE SHAPER U2
DRIVE SHAPER U9
DRIVE SHAPER U6
DRIVER SHAPER U10
DRIVER SHAPER U7
PULL UP DRIVER Q9, 10
PULLDOWN DRIVER Q11
PULL UP DRIVER Q20, 21
PULL DOWN DRIVER Q22
PULL UP DRIVER Q38, 39
PULL DOWN DRIVER Q37
PULL UP DRIVER Q49, 50
PULL DOWN DRIVER Q48
+70V +57 SW +83V (TYPICAL)
DIFF. AMP. U12
R89 DIFF. BAL.
DIFF. AMP. U13
R10 DIFF. BAL.
FILTER L2
FILTER L7
CURRENT SENSOR R4
CURRENT SENSOR R3
REEL MDA'S PWA
POWER CHASSIS MOTHER PWA (PARTIAL)
TAPE COUPLING
AIR PRESSURE TO GUIDE IS
SUPPLY REEL TACH "B"
SUPPLY REEL TACH "A"
MOTOR DIRECTION REVERSE JUMPER
TAKE UP REEL TACH "B"
SUPPLY REEL TACH "A"
VACUUM CAPSTAN
FLUTTER IDLER
AIR GUIDES
ROLLER GUIDES
VPR-3 REEL SERVO SYSTEM BLOCK DIAGRAM



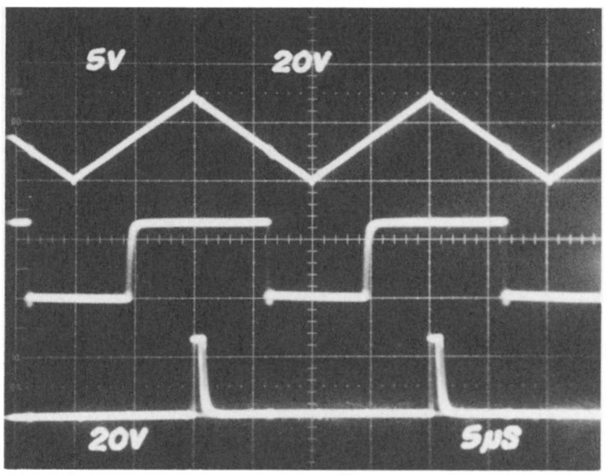
VPR-3 A14-3
REEL SERVO
525/625



WF1 TP2: Reference Ramp

WF2 TP1: Pull Up drive

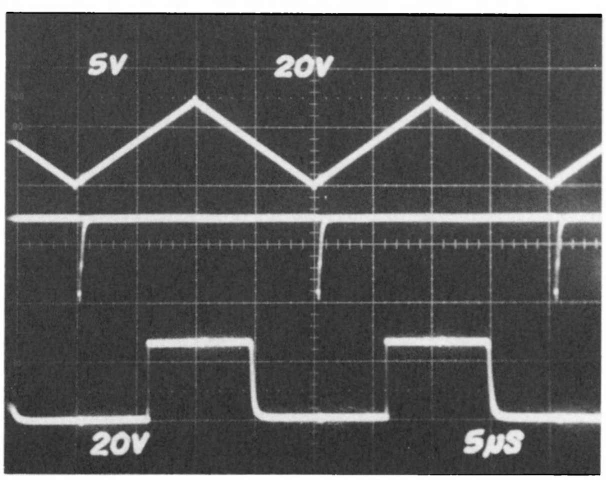
WF3 TP3: Pull down Drive
300 ips rewind



WF1 TP2: Reference Ramp

WF2 TP1: Pull up drive

WF3 TP3: Pull down drive
500 ips Rewind SHUTTLE

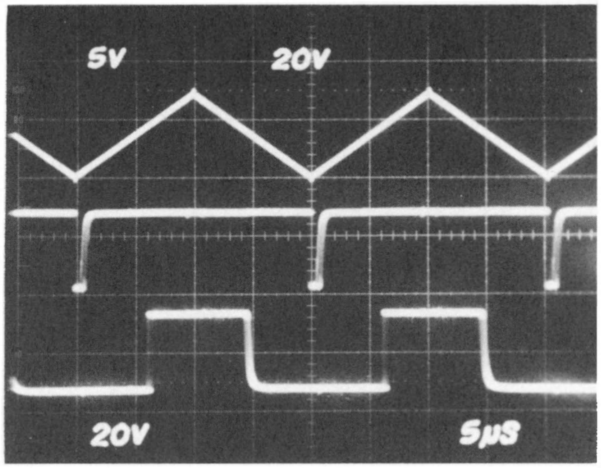


WF1 TP2: Reference Ramp

WF2 TP1: Pull up Drive

WF3 TP3: Pull down Drive
Shuttle STOP

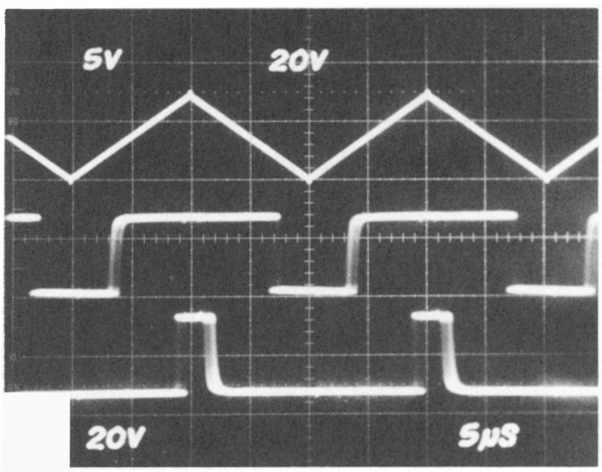
VPR-3 TAKE UP MDA



WF1 TP2: 150 Triangle Ref.

WF2 TP9: Pull up Drive

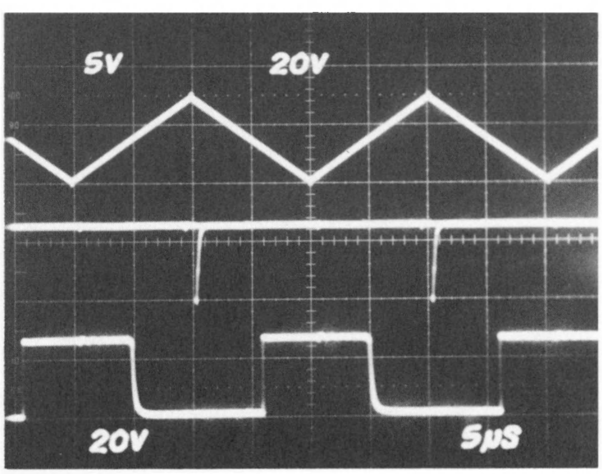
WF3 TP8: Pull down Drive
VPR-3 in 300 ips Rewind



WF1 TP2: 150 Triangle Ref.

WF2 TP9: Pull up Drive

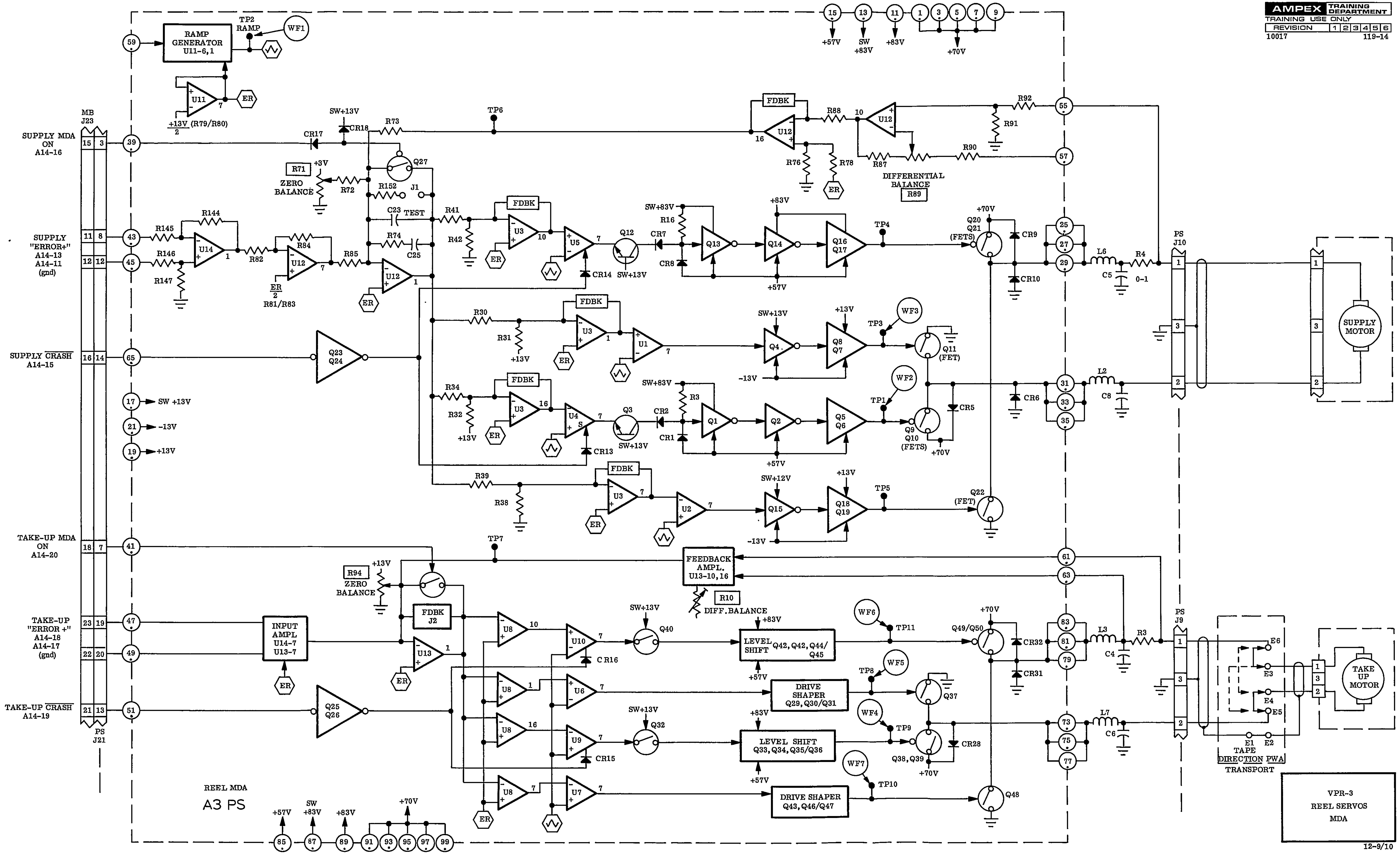
WF3 TP8: Pull down Drive
VPR-3 in 300 ips Rewind



WF1 TP2: 150 Triangle Ref.

WF2 TP11: Pull up Drive

WF3 TP10: Pull down Drive
VPR-3 in Shuttle STOP



VPR-3
REEL SERVOS
MDA

AMPEX TRAINING DEPARTMENT
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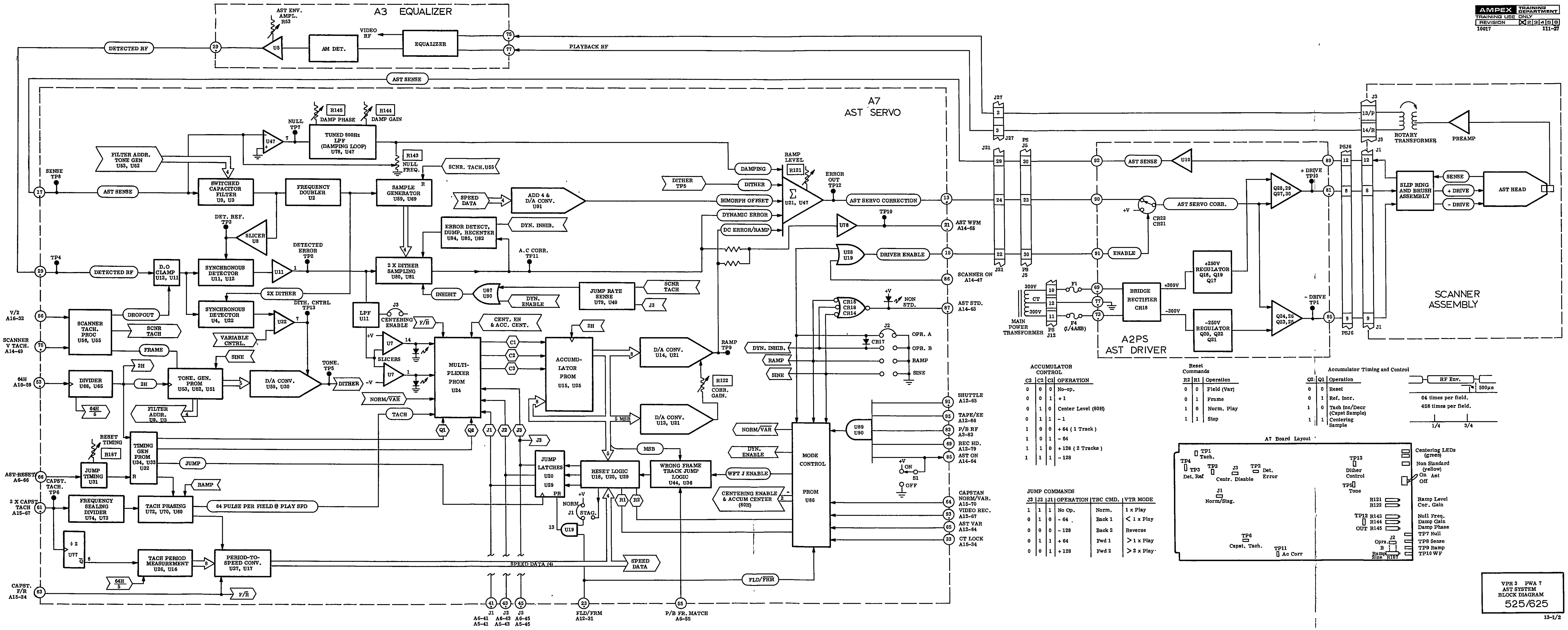
10017 111-27



ACCUMULATOR CONTROL

C3	C2	C1	OPERATION
0	0	0	No-op.
0	0	1	+ 1
0	1	0	Center Level (80H)
0	1	1	- 1
1	0	0	+ 64 (1 Track)
1	0	1	- 64
1	1	0	+ 128 (2 Tracks)
1	1	1	- 128

JUMP COMMANDS

J3	J2	J1	OPERATION	TBC CMD.	VTR MODE
1	1	1	No Op.	Norm.	1 x Play
0	1	0	- 64	Back 1	< 1 x Play
0	0	0	- 128	Back 2	Reverse
0	1	1	+ 64	Fwd 1	> 1 x Play
0	0	1	+ 128	Fwd 2	> 2 x Play

Reset Commands

R2	R1	Operation
0	0	Field (Var)
0	1	Frame
1	0	Norm. Play
1	1	Stop

Accumulator Timing and Control

Q2	Q1	Operation
0	0	Reset
0	1	Ref. Incr.
1	0	Tach Inc/Decr (Capst Sample)
1	1	Centering Sample

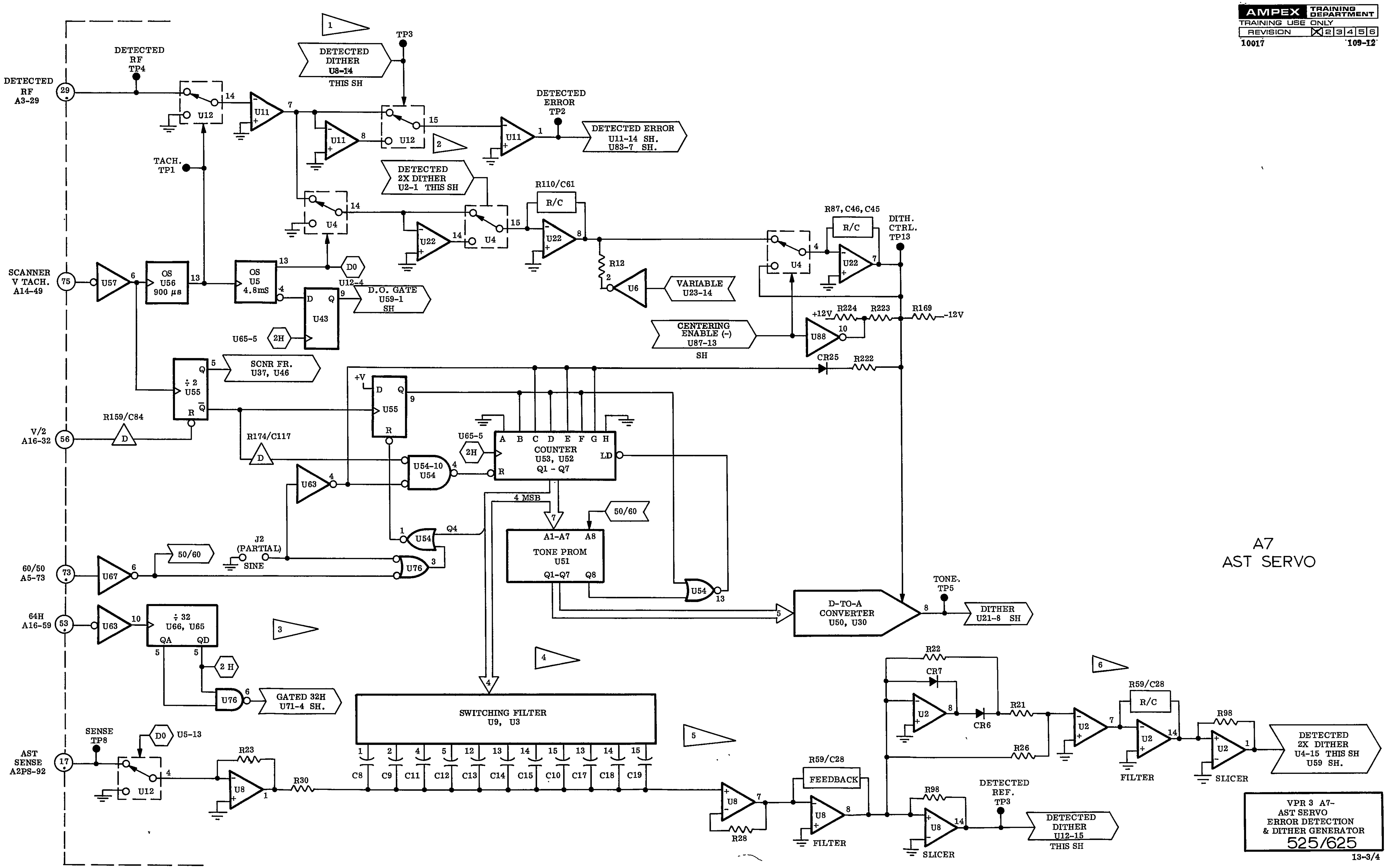
RF Env.
500μs
64 times per field.
458 times per field.
1/4 3/4

A7 Board Layout

TP1 Tach.
TP4
TP3 Det. Ref
TP3
J3 Centr. Disable
TP2 Det. Error
J1 Norm/Stag.
TP13 Dither Control
TP5 Tone
TP6 Capst. Tach.
TP11 Ac Corr
R121 R122
TP12 R143 R144 OUT R145
J2 Opra. B Ramp Sine R187
Centering LEDs (green)
Non Standard (yellow)
On Ast Off
Ramp Level
Cor. Gain
Null Freq.
Damp Gain
Damp Phase
TP7 Null
TP8 Sense
TP9 Ramp
TP10 WF

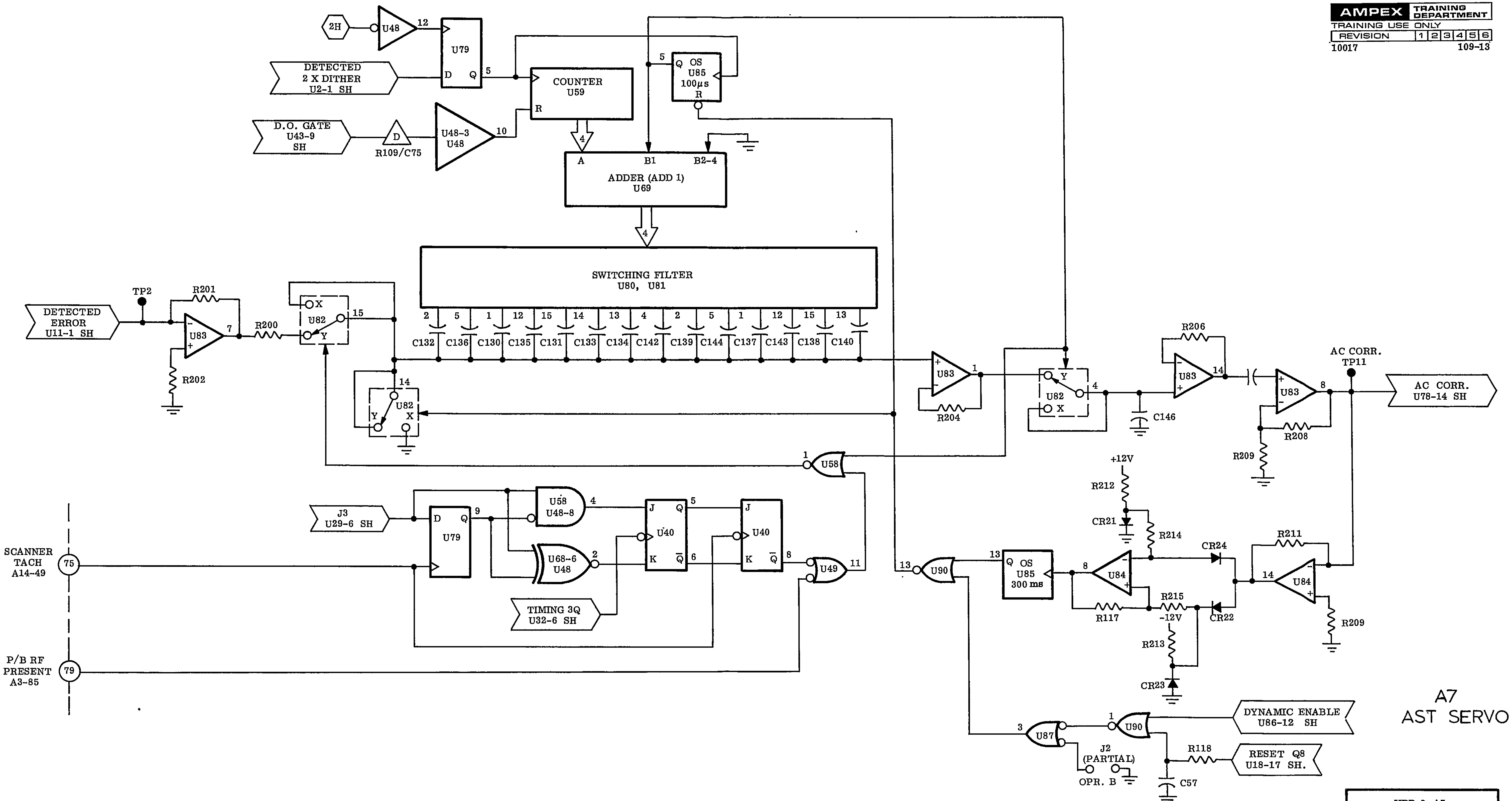
VPR 3 PWA 7
AST SYSTEM
BLOCK DIAGRAM
525/625

13-1/2



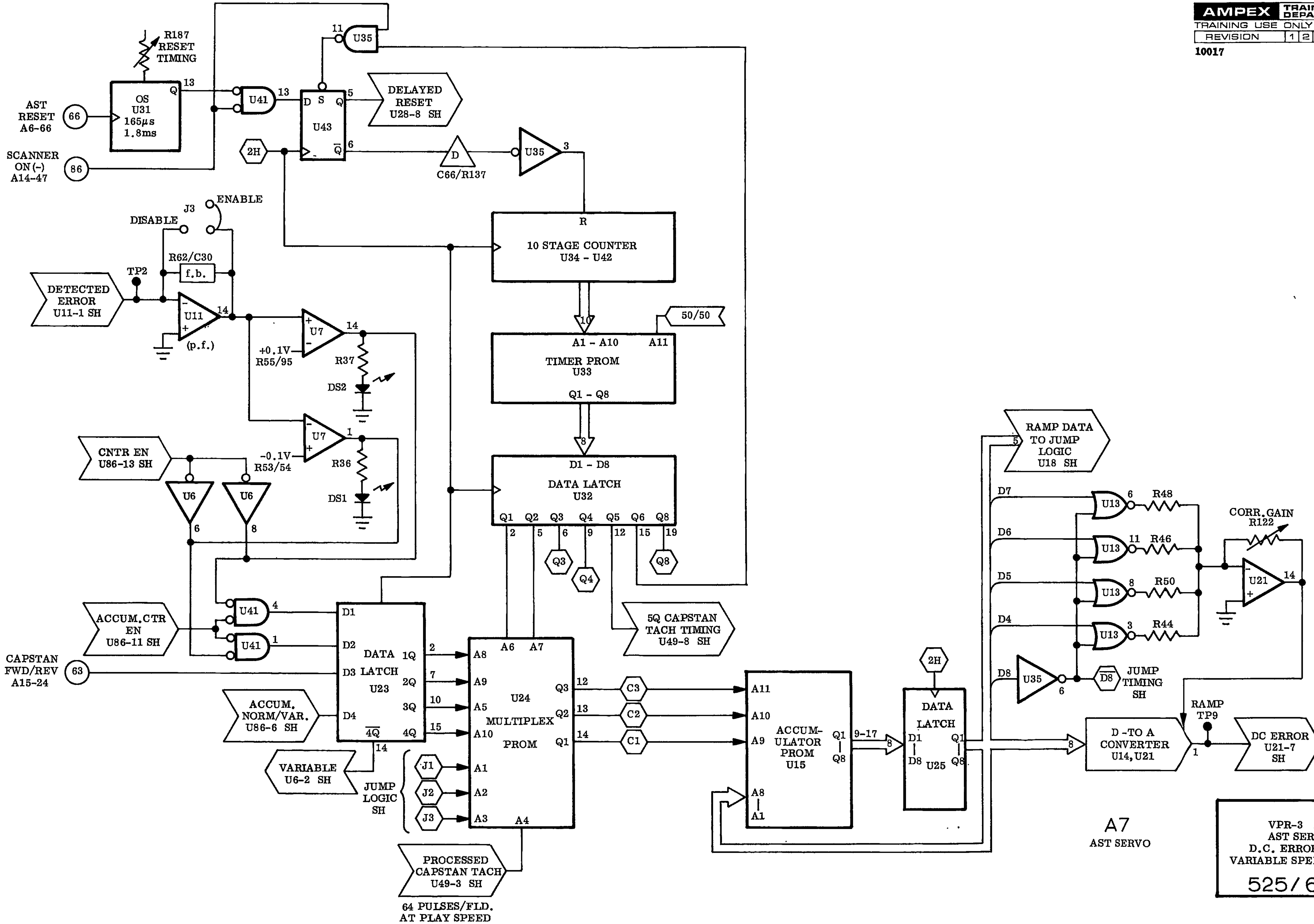
A7
AST SERVO

VPR 3 A7-
AST SERVO
ERROR DETECTION
& DITHER GENERATOR
525/625



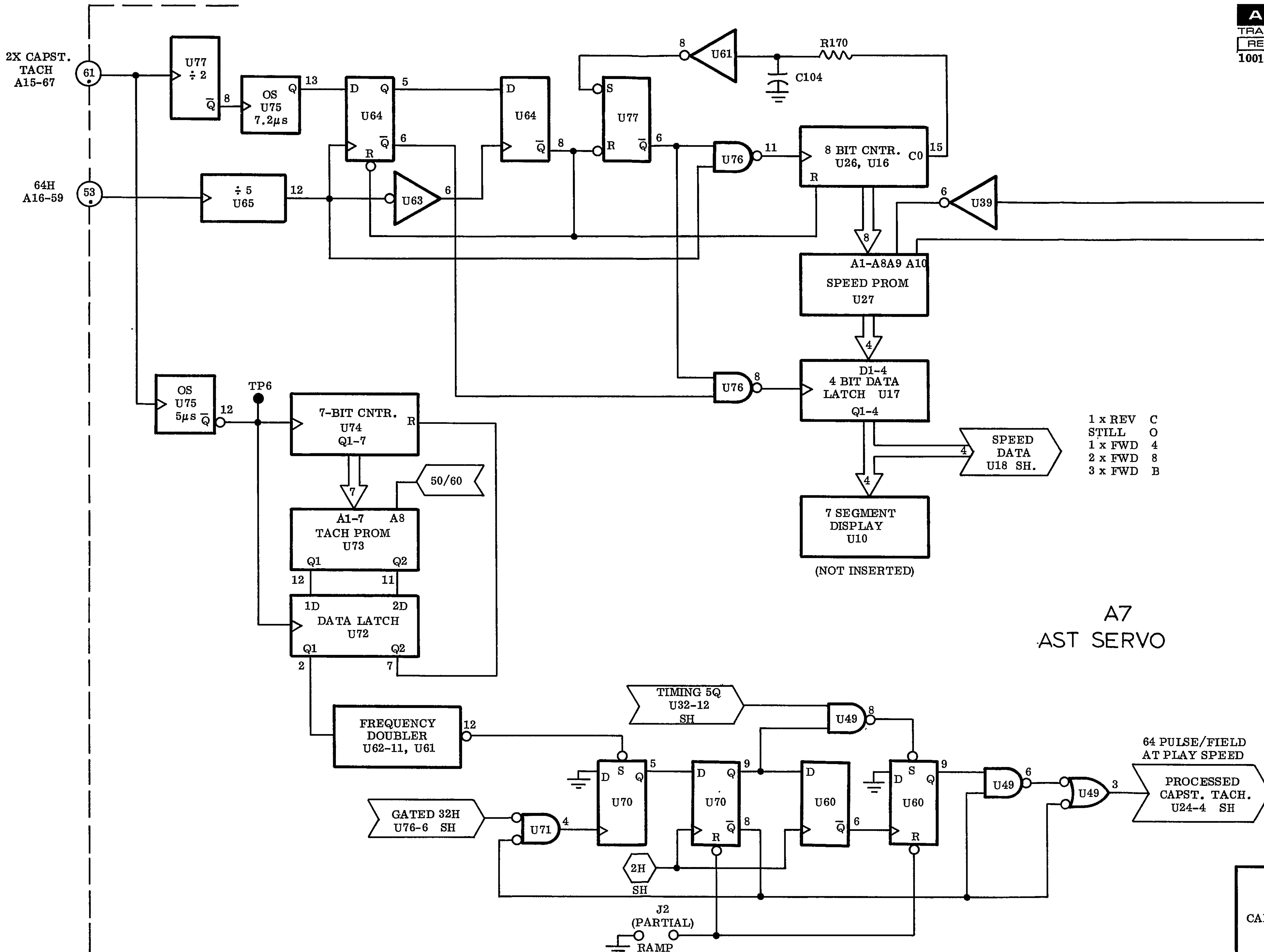
A7
AST SERVO

VPR-3 A7-
AST SERVO
DYNAMIC ERROR
DETECTION
525/625



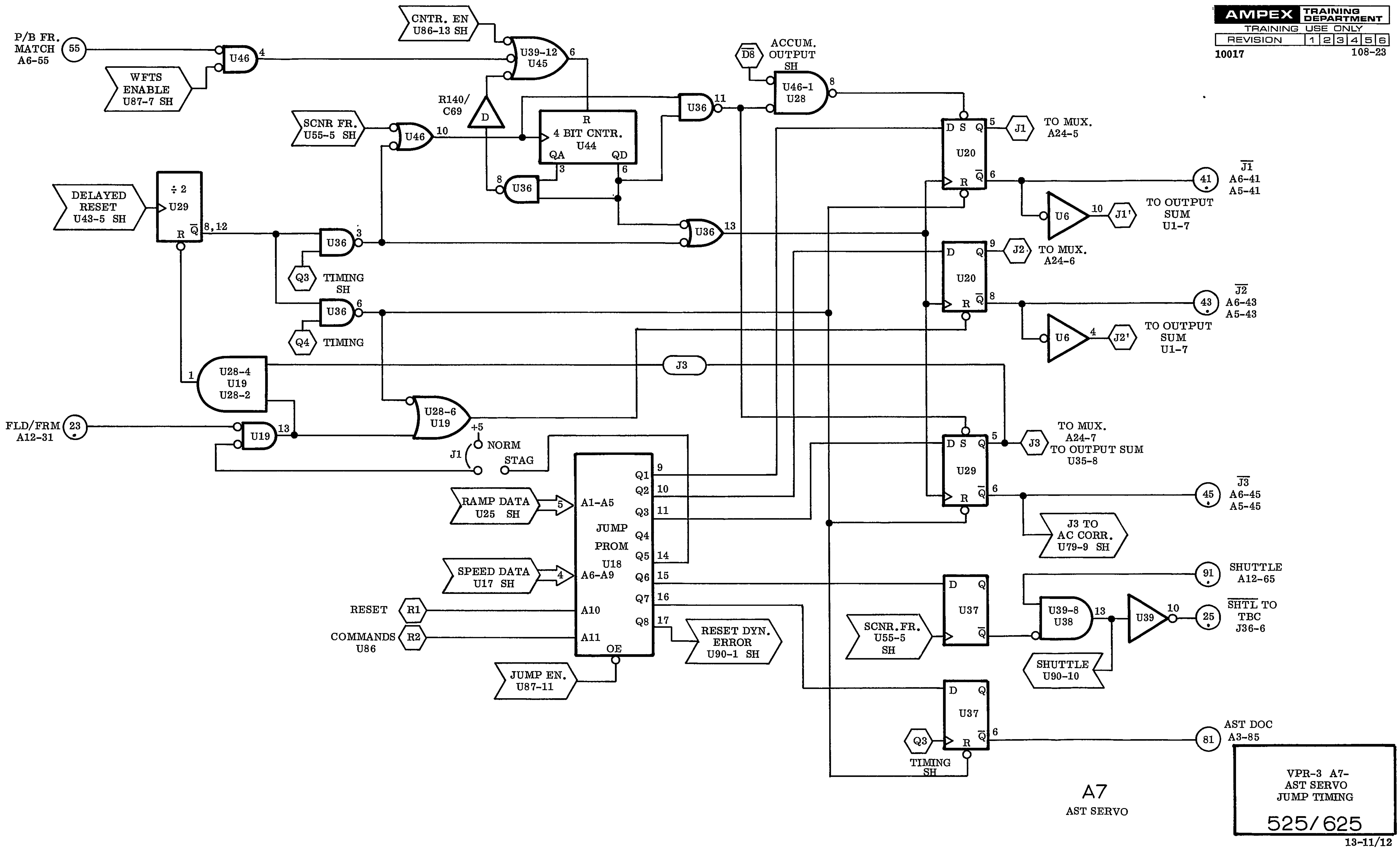
VPR-3 A7-
AST SERVO
D.C. ERROR AND
VARIABLE SPEED RAMP

525/625

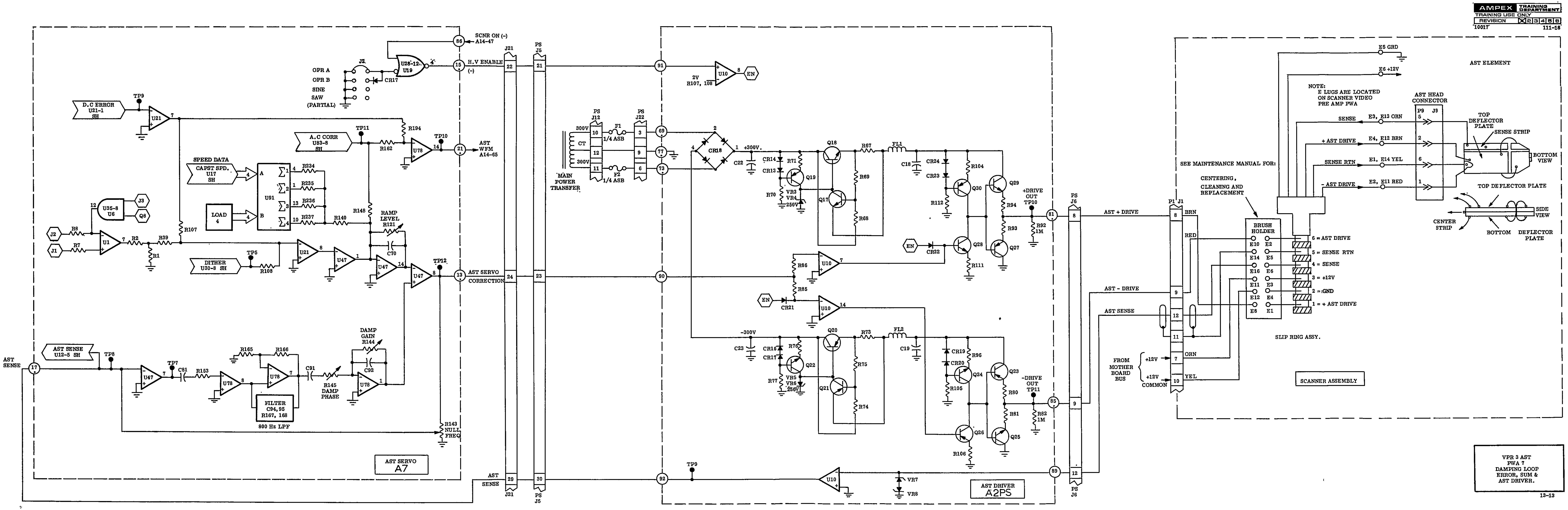


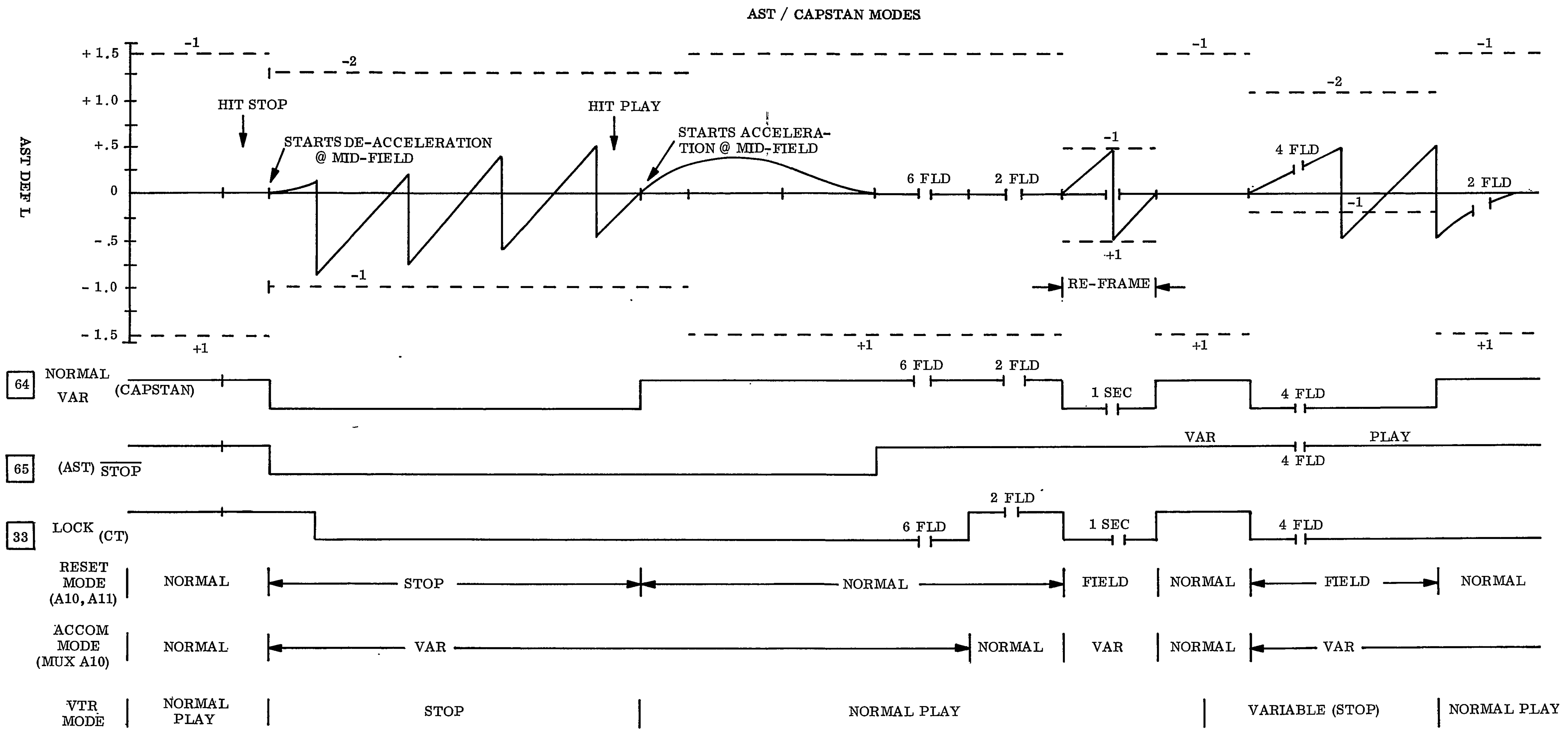
VPR-3 A7-
AST SERVO
CAPSTAN TACH PROCESSING
525/625

13-9/10

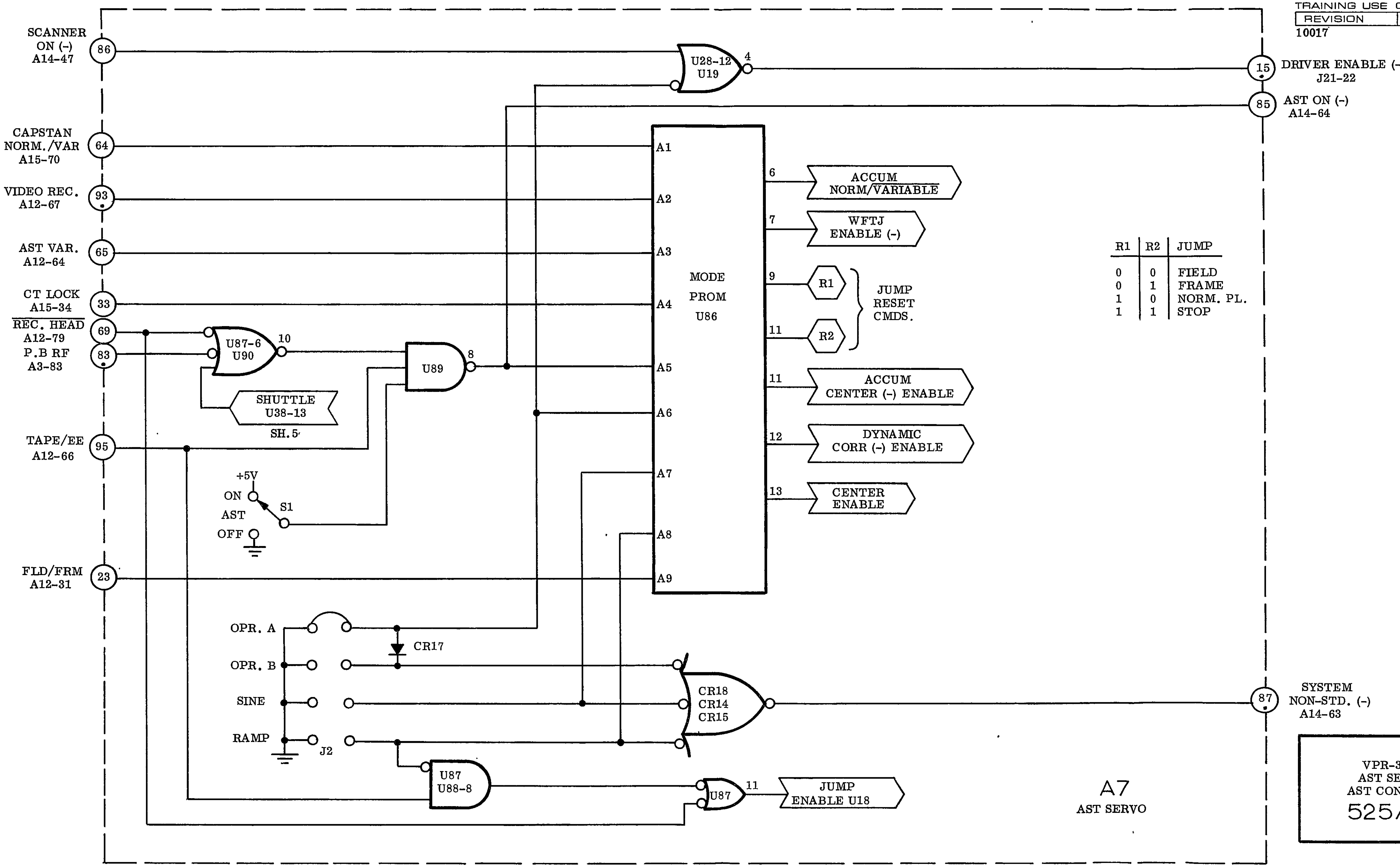


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
108-23
P/B FR. MATCH A6-55
55
U46
4
WFTS ENABLE U87-7 SH
CNTR. EN U86-13 SH
U39-12 U45
6
R140/ C69
D
SCNR FR. U55-5 SH
U46
10
R
4 BIT CNTR. U44
QA
QD
3
6
8
U36
U36
11
D8
ACCUM. OUTPUT SH
U46-1 U28
8
DELAYED RESET U43-5 SH
÷ 2
U29
R
Q
8,12
U36
3
Q3
TIMING SH
U36
13
U36
6
Q4
TIMING
D S Q
U20
R
Q
5
J1
TO MUX. A24-5
6
41
J1
A6-41 A5-41
U6
10
J1'
TO OUTPUT SUM U1-7
D Q
U20
9
J2
TO MUX. A24-6
8
43
J2
A6-43 A5-43
U6
4
J2'
TO OUTPUT SUM U1-7
1
U28-4 U19 U28-2
J3
U28-6 U19
FLD/FRM A12-31
23
U19
13
+5
NORM
J1
STAG
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
9
10
11
14
15
16
17
RAMP DATA U25 SH
5
A1-A5
JUMP PROM U18
SPEED DATA U17 SH
4
A6-A9
RESET
R1
A10
COMMANDS U86
R2
A11
OE
JUMP EN. U87-11
RESET DYN. ERROR U90-1 SH
D S Q
U29
R
Q
5
J3
TO MUX. A24-7
TO OUTPUT SUM U35-8
6
45
J3
A6-45 A5-45
J3 TO AC CORR. U79-9 SH
91
SHUTTLE A12-65
D Q
U37
Q
SCNR.FR. U55-5 SH
U39-8 U38
13
U39
10
25
SHTL TO TBC J36-6
SHUTTLE U90-10
D Q
U37
Q3
R
TIMING SH
6
81
AST DOC A3-85
A7
AST SERVO
VPR-3 A7- AST SERVO JUMP TIMING
525/625
13-11/12

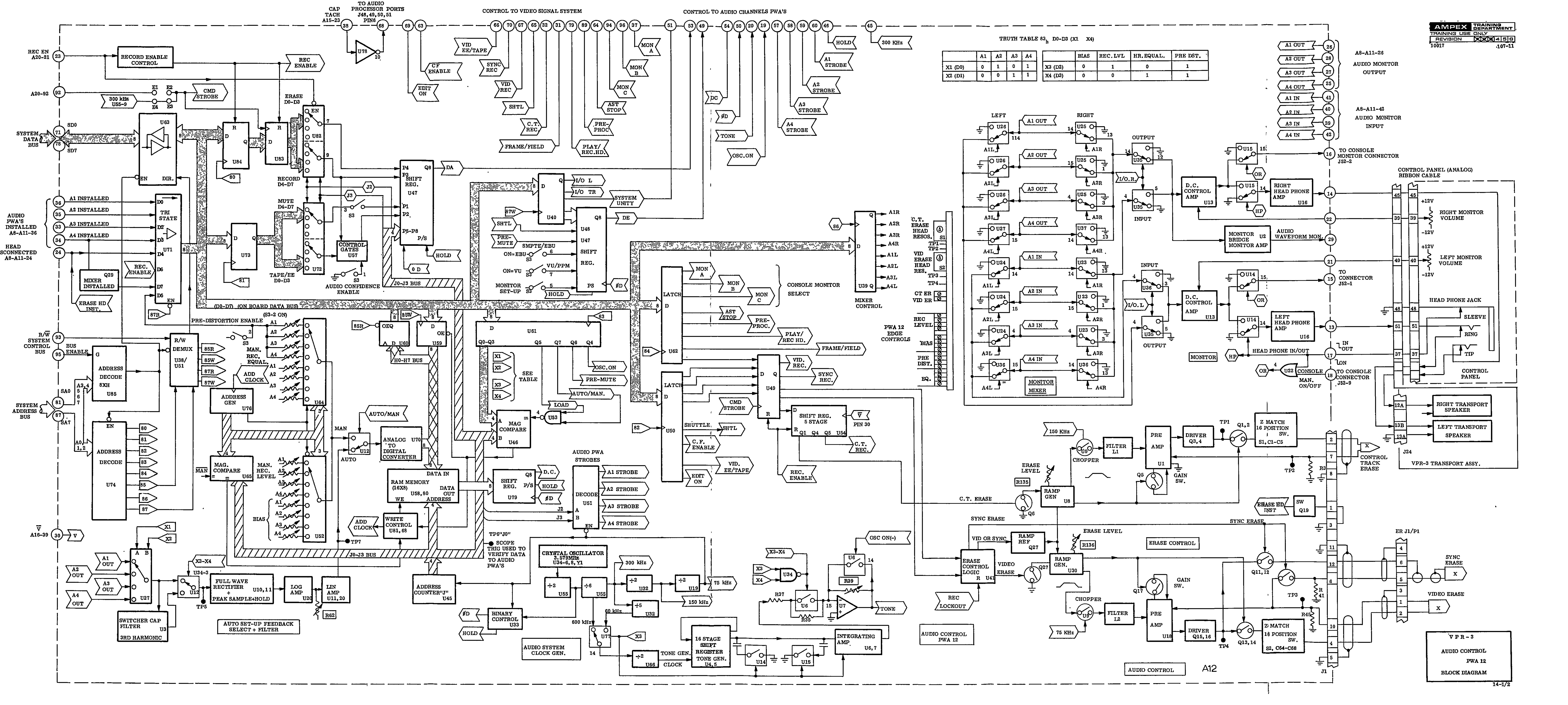

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION
10017
111-18
SCNR ON (-)
A14-47
H.V ENABLE
(-)
OPR A
OPR B
SINE
SAW
(PARTIAL)
J2
U28-12
U19
CR17
D.C ERROR
U21-1
SH
TP9
U21
R194
A.C CORR
U83-8
SH
TP11
R162
U78
TP10
AST
WFM
A14-65
SPEED DATA
CAPST SPD.
U17
SH
U91
R234
R235
R236
R237
R140
R148
RAMP
LEVEL
R121
C70
U35-8
U6
J3
Q8
LOAD
4
R107
R8
R7
J2
J1
U1
R2
R39
R1
DITHER
U30-8 SH
TP5
R108
U47
TP12
AST SERVO
CORRECTION
AST SENSE
U12-5 SH
TP8
TP7
C81
R153
R165
R166
C91
DAMP
GAIN
R144
C92
R145
DAMP
PHASE
FILTER
C94, 95
R167, 168
800 Hz LPF
R143
NULL
FREQ
AST SERVO
A7
AST
SENSE
J21
PS
J5
2V
R107, 108
U10
EN
PS
J12
PS
J22
F1
1/4 ASB
F2
1/4 ASB
300V
CT
MAIN
POWER
TRANSFER
CR18
+300V
C22
CR14
CR13
R71
Q19
VR3
VR4
250V
R70
Q18
Q17
R67
FL1
R69
R68
C18
CR24
CR23
R104
R112
Q30
Q29
R94
R93
R92
1M
+DRIVE
OUT
TP10
Q28
Q27
CR22
R111
R86
R85
CR21
-300V
C23
CR16
CR17
R76
Q22
VR5
VR6
250V
R77
Q20
Q21
R73
FL2
R75
R74
C19
CR19
CR20
R96
R105
Q24
Q23
R80
-DRIVE
OUT
TP11
R81
R82
1M
Q26
Q25
R106
VR7
VR8
AST DRIVER
A2PS
PS
J6
AST + DRIVE
AST - DRIVE
AST SENSE
FROM
MOTHER
BOARD
BUS
+12V
+12V
COMMON
P1
J1
BRN
RED
ORN
YEL
SEE MAINTENANCE MANUAL FOR:
CENTERING,
CLEANING AND
REPLACEMENT
BRUSH
HOLDER
E10
E2
E14
E5
E16
E6
E11
E3
E12
E4
E8
E1
6 = AST DRIVE
5 = SENSE RTN
4 = SENSE
3 = +12V
2 = GND
1 = + AST DRIVE
SLIP RING ASSY.
SCANNER ASSEMBLY
E5 GRD
E6 +12V
AST ELEMENT
NOTE:
E LUGS ARE LOCATED
ON SCANNER VIDEO
PRE AMP PWA
SENSE
E3, E13 ORN
+ AST DRIVE
E4, E12 BRN
SENSE RTN
E1, E14 YEL
- AST DRIVE
E2, E11 RED
AST HEAD
CONNECTOR
P9
J9
TOP
DEFLECTOR
PLATE
SENSE STRIP
BOTTOM
VIEW
TOP DEFLECTOR PLATE
SIDE
VIEW
CENTER
STRIP
BOTTOM
DEFLECTOR
PLATE
VPR 3 AST
PWA 7
DAMPING LOOP
ERROR, SUM &
AST DRIVER.
13-13



VPR-3 A7-
AST SERVO
SERVO MODES



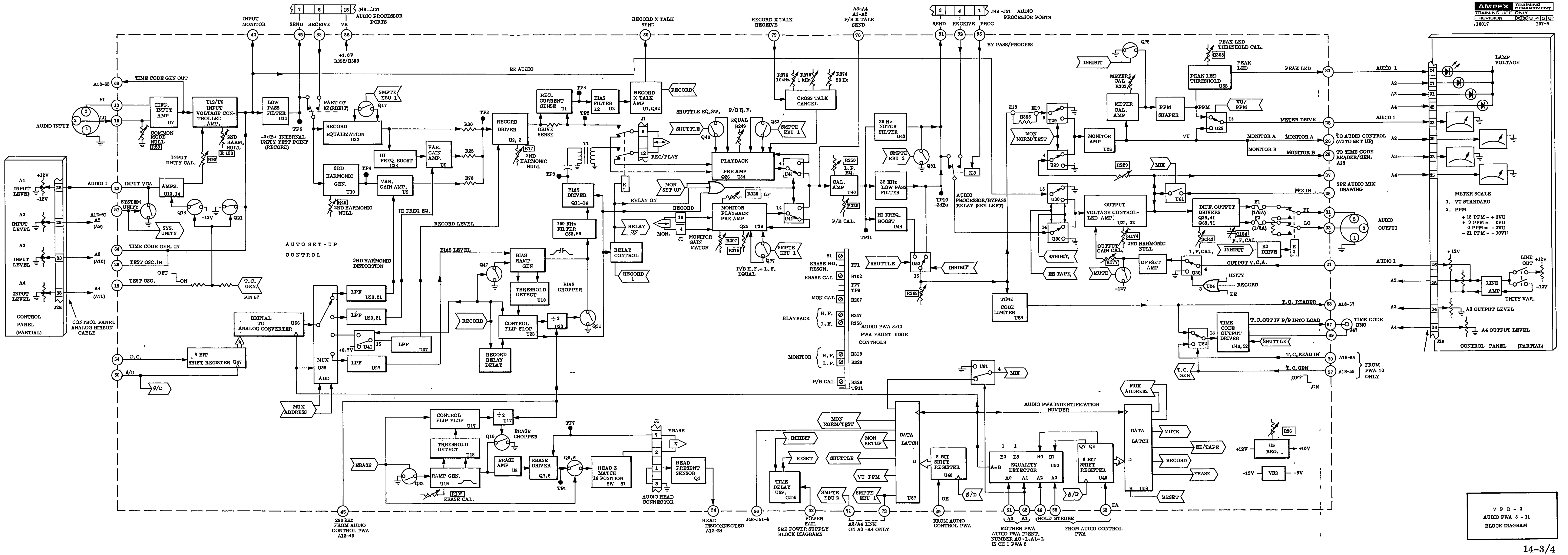
VPR-3 A7- 7/7
AST SERVO
AST CONTROL
525/625

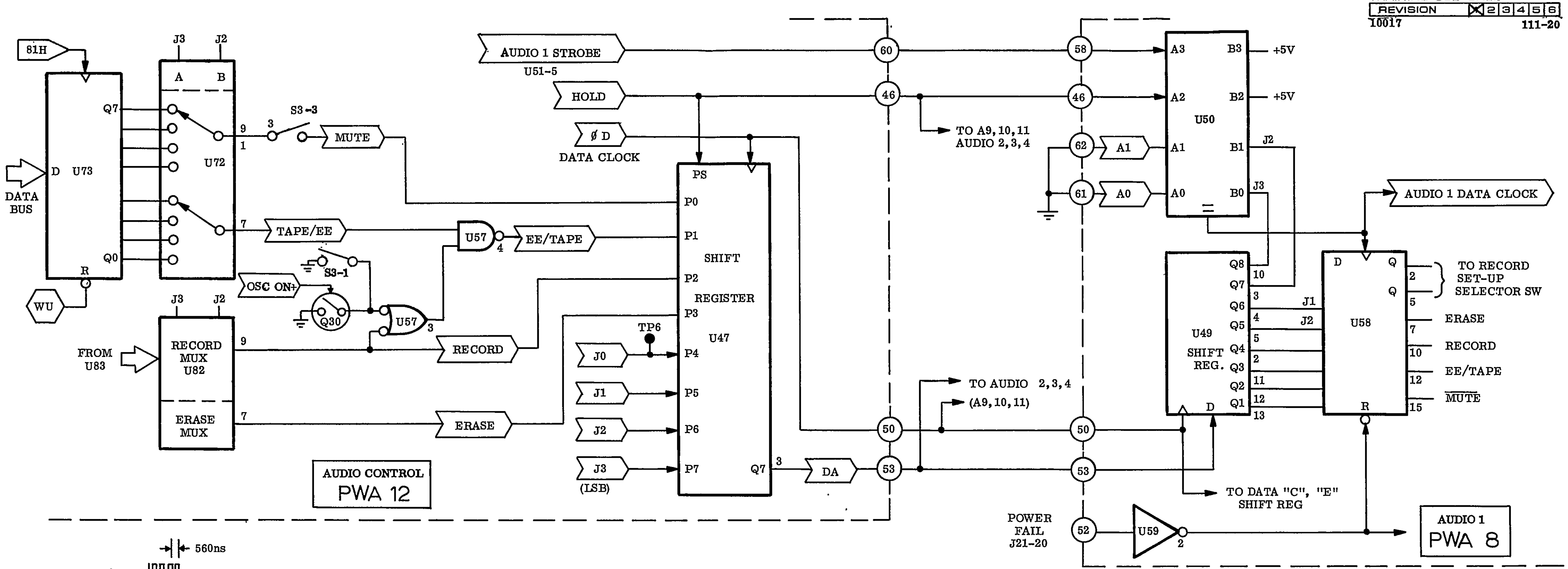


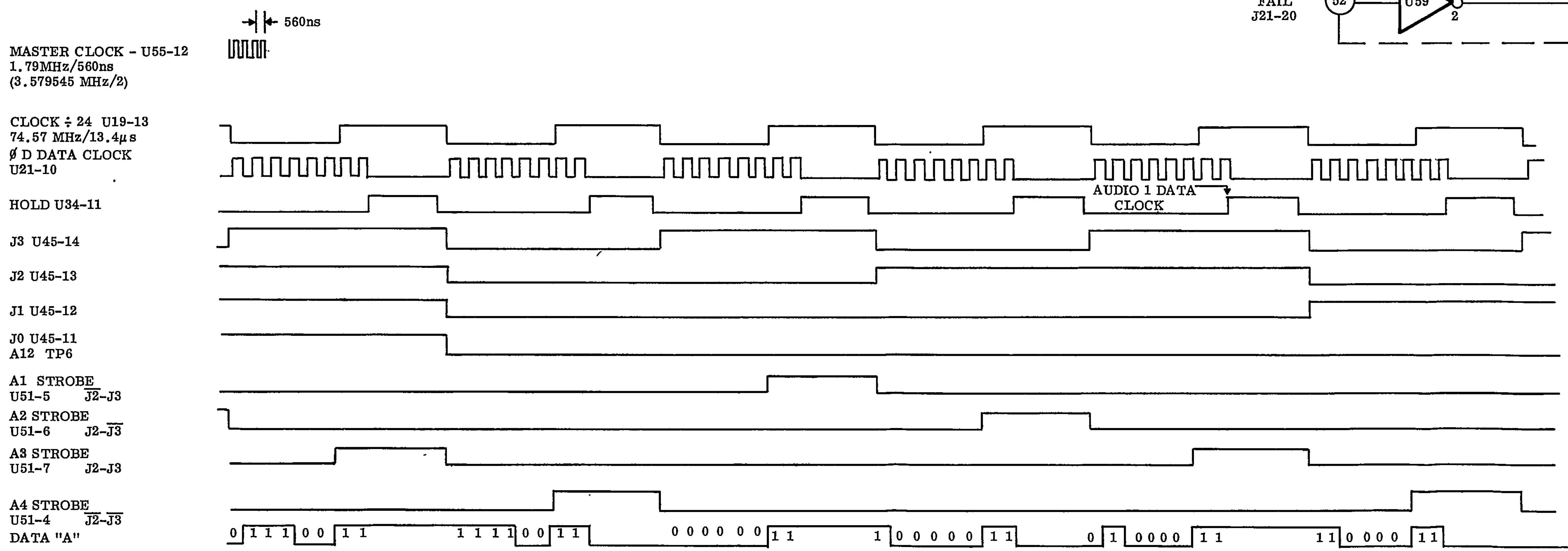
TRUTH TABLE 83_h D0-D3 (X1 X4)

	A1	A2	A3	A4
X1 (D0)	0	1	0	1
X2 (D1)	0	0	1	1

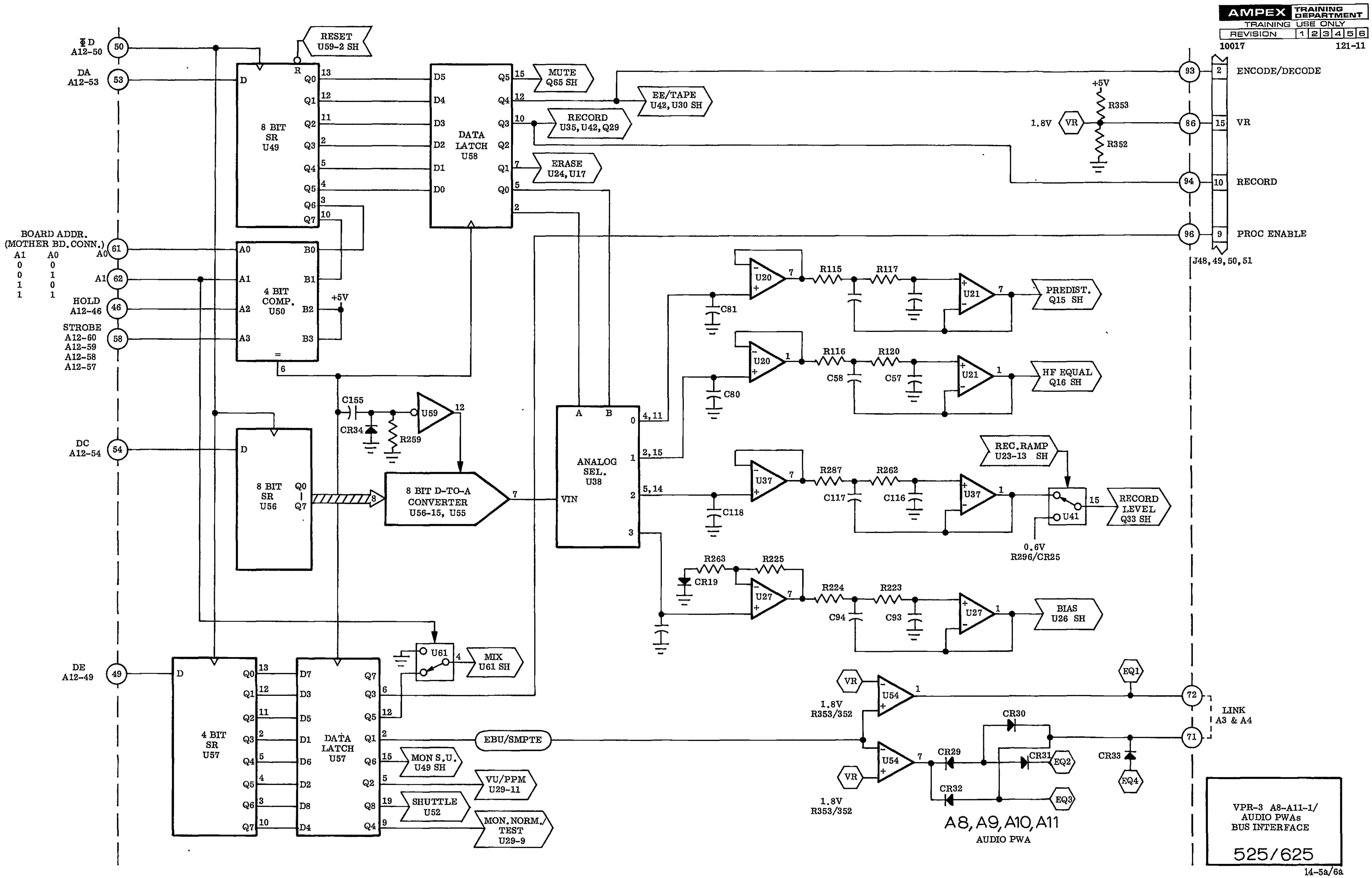
	BIAS	REC. LVL	HR. EQUAL.	PRE DST.
X3 (D2)	0	1	0	1
X4 (D3)	0	0	1	1


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION
1001 7
107-9
VPR-3
AUDIO PWA 8-11
BLOCK DIAGRAM
AUDIO INPUT
HI
LO
DIFF. INPUT AMP U7
U12/U6 INPUT VOLTAGE CONTROLLED AMP.
COMMON MODE NULL R59
INPUT UNITY CAL. R93
2ND HARM. NULL R130
LOW PASS FILTER U11
-3dBu INTERNAL UNITY TEST POINT (RECORD)
INPUT MONITOR
SEND
RECEIVE
VR
+1.8V R352/R353
J48-J51 AUDIO PROCESSOR PORTS
TIME CODE GEN OUT
EE AUDIO
INPUT VCA
AMPS. U13, 14
SYSTEM UNITY
SYS. UNITY
TIME CODE GEN. IN
TEST OSC. IN
TEST OSC.
T.C. GEN. PIN 57
CONTROL PANEL (PARTIAL)
CONTROL PANEL ANALOG RIBBON CABLE
INPUT LEVEL
AUTO SET-UP CONTROL
RECORD EQUALIZATION U22
SMPTE EBU 1
PART OF K3 (RIGHT)
HI FREQ. BOOST C38
VAR. GAIN AMP. U9
3RD HARMONIC GEN. U10
2ND HARMONIC NULL
HI FREQ EQ.
RECORD LEVEL
3RD HARMONIC DISTORTION
BIAS LEVEL
RECORD DRIVER U2, 3
2ND HARMONIC NULL R77
REC. CURRENT SENSE U1
DRIVE SENSE
BIAS FILTER L2 U2
RECORD X TALK AMP U1, Q82
RECORD X TALK SEND
RECORD
BIAS DRIVER Q11-14
150 KHz FILTER C52, 66
BIAS RAMP GEN
THRESHOLD DETECT U18
BIAS CHOPPER
CONTROL FLIP FLOP U23
RECORD RELAY DELAY
DIGITAL TO ANALOG CONVERTER U56
8 BIT SHIFT REGISTER U47
LPF U20, 21
LPF U37
LPF U27
MUX U38
ADD
MUX ADDRESS
REC/PLAY
RELAY ON
RELAY CONTROL
RECORD 1
MON SET UP
MONITOR GAIN MATCH
SHUTTLE EQ. SW.
SHUTTLE
P/B H.F. EQUAL
PLAYBACK PRE AMP Q26 U34
MONITOR PLAYBACK PRE AMP Q25 U39
P/B H.F. + L.F. EQUAL
RECORD X TALK RECEIVE
CROSS TALK CANCEL
A3-A4 A1-A2 P/B X TALK SEND
30 Hz NOTCH FILTER U43
32 KHz LOW PASS FILTER
HI FREQ. BOOST U44
CAL. AMP U40
L.F. EQ.
P/B CAL.
AUDIO PROCESSOR/BYPASS RELAY (SEE LEFT)
BY PASS/PROCESS
INHIBIT
ERASE HD. RESON.
ERASE CAL
MON CAL
PLAYBACK
MONITOR
P/B CAL
AUDIO PWA 8-11 PWA FRONT EDGE CONTROLS
TIME CODE LIMITER U53
MON NORM/TEST
MONITOR AMP U28
METER CAL. AMP
METER CAL R302
PPM SHAPER
PEAK LED THRESHOLD U55
PEAK LED THRESHOLD CAL.
PEAK LED
METER DRIVE
MONITOR A
MONITOR B
TO AUDIO CONTROL (AUTO SET UP)
TO TIME CODE READER/GEN. A18
SEE AUDIO MIX DRAWING
MIX IN
MIX
OUTPUT VOLTAGE CONTROLLED AMP. U31, 32
OUTPUT GAIN CAL.
2ND HARMONIC NULL
DIFF. OUTPUT DRIVERS Q38, 41 Q69, 71
H.F. CAL.
L.F. CAL.
K2 DRIVE
AUDIO OUTPUT
OFFSET AMP
OUTPUT V.C.A.
UNITY
EE
EE TAPE
MUTE
T.C. READER
TIME CODE OUTPUT DRIVER U46, 52
T.C. OUT IV P/P INTO LOAD
TIME CODE BNC
T.C. READ IN
T.C. GEN
FROM PWA 10 ONLY
LAMP VOLTAGE
METER SCALE
1. VU STANDARD
2. PPM
+18 PPM = +3VU
+9 PPM = 0VU
0 PPM = -3VU
-21 PPM = -10VU
LINE OUT
LINE AMP
UNITY VAR.
A3 OUTPUT LEVEL
A4 OUTPUT LEVEL
CONTROL PANEL (PARTIAL)
CONTROL FLIP FLOP U17
THRESHOLD DETECT U18
RAMP GEN. U19
ERASE CAL. R102
ERASE AMP U8
ERASE CHOPPER
ERASE DRIVER Q7, 8
HEAD Z MATCH 16 POSITION SW S1
HEAD PRESENT SENSOR Q1
AUDIO HEAD CONNECTOR
ERASE
298 kHz FROM AUDIO CONTROL PWA A12-45
HEAD DISCONNECTED A12-24
TIME DELAY U59 C156
POWER FAIL SEE POWER SUPPLY BLOCK DIAGRAMS
A3/A4 LINK ON A3+A4 ONLY
RESET
VU PPM
DATA LATCH U57
8 BIT SHIFT REGISTER U48
FROM AUDIO CONTROL PWA
AUDIO PWA INDENTIFICATION NUMBER
EQUALITY DETECTOR U50
8 BIT SHIFT REGISTER U49
HOLD STROBE
MOTHER PWA AUDIO PWA IDENT. NUMBER A0=L, A1=L IS CH 1 PWA 8
DATA LATCH U58
EE/TAPE
U5 REG.
+12V
+10V
-12V
-5V
VR2

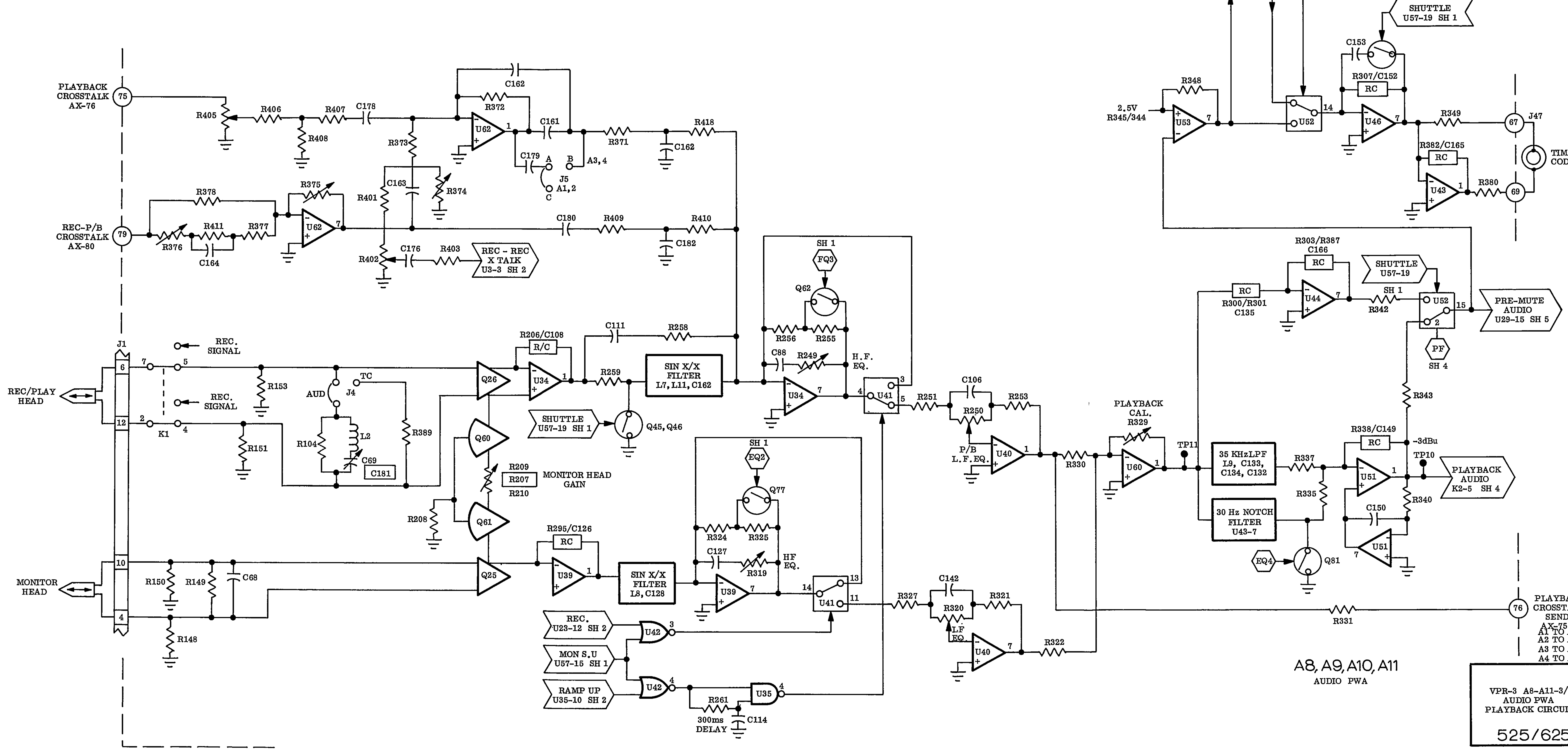




VPR-3
AUDIO
SERIAL DATA
TIMING
(IDEALIZED)
"DA" BUS


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
121-11
Φ D A12-50
DA A12-53
BOARD ADDR. (MOTHER BD. CONN.)
A1 A0
0 0
0 1
1 0
1 1
HOLD A12-46
STROBE A12-60 A12-59 A12-58 A12-57
DC A12-54
DE A12-49
8 BIT SR U49
DATA LATCH U58
4 BIT COMP. U50
8 BIT SR U56
8 BIT D-TO-A CONVERTER U56-15, U55
ANALOG SEL. U38
4 BIT SR U57
DATA LATCH U57
RESET U59-2 SH
MUTE Q65 SH
EE/TAPE U42, U30 SH
RECORD U35, U42, Q29
ERASE U24, U17
C155
CR34
R259
U59
U61
MIX U61 SH
EBU/SMPTE
MON S.U. U49 SH
VU/PPM U29-11
SHUTTLE U52
MON. NORM./TEST U29-9
ENCODE/DECODE
VR
RECORD
PROC ENABLE
J48, 49, 50, 51
+5V
R353
R352
1.8V
U20
U21
R115
R117
C81
PREDIST. Q15 SH
R116
R120
C58
C57
C80
HF EQUAL Q16 SH
U37
R287
R262
C117
C116
C118
REC. RAMP U23-13 SH
U41
RECORD LEVEL Q33 SH
0.6V R296/CR25
R263
R225
CR19
U27
R224
R223
C94
C93
BIAS U26 SH
EQ1
U54
1.8V R353/352
CR30
CR29
CR31
EQ2
CR32
EQ3
CR33
EQ4
LINK A3 & A4
A8, A9, A10, A11
AUDIO PWA
VPR-3 A8-A11-1/ AUDIO PWAs BUS INTERFACE
525/625
14-5a/6a

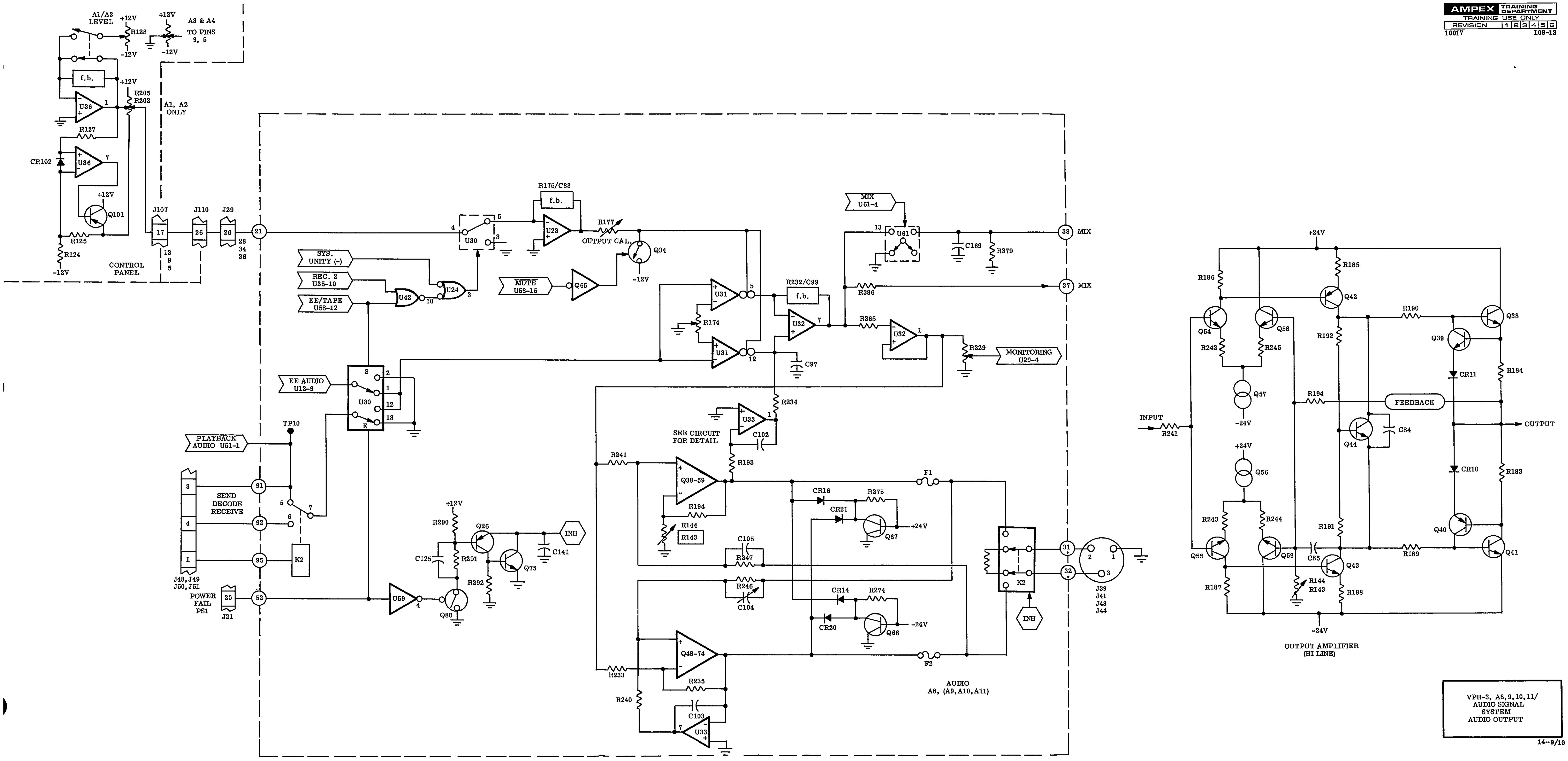
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 121-9



VPR-3 A8-A11-3/4
AUDIO PWA
PLAYBACK CIRCUITS

525/625

14-7/8



VPR-3, A8,9,10,11/ AUDIO SIGNAL SYSTEM AUDIO OUTPUT

AUDIO PREDISTORTION

Stan Busby

The basic concept of pre-distortion has been around for a long time. It was known to have been applied to a Scully audio tape recorder about 20 years ago.

The idea is: if you know that in passing something through some process, the something is going to get bent to the left, then you bend it to the right first, so when it leaves the system it will have been straightened.

A perfectly tweaked audio recorder, or the audio part of a video recorder should produce only odd-order harmonic distortion, mostly the third. The phase of the distortion is such as to correspond to compression of both negative and positive peaks (equally).

Typical distortions are 0.8% at normal operating level, and 3% at 8db above that. Program peaks frequently reach this level. The absolute amplitude of the distortion is very closely proportional to the cube of the recorded signal. Predistortion generates and injects into the record path a cubic distortion of opposite phase to that which the recording process will generate later, causing cancellation of distortion. It is not perfect, but will typically reduce distortion at 8db above normal record level to 1/5 to 1/6 of what it would otherwise be.

The presence of predistortion does not mean that the dynamic range offered by the tape has been increased. The ceiling of tape saturation is still there, unmodified, but as the record level rises to that ceiling, it sees an improved linearity. This feature makes predistortion unpopular in some quarters, especially the golden ear types. With predistortion, overload is more abrupt, and is said by some to be inferior to the "softer" overload characteristics of unmodified recording.

When wide record gaps are used on the thick coatings of audio tape, it is possible to minimize distortion by careful adjustment of bias current. This feature is not available on video recorders because the tape is thin, and, for lip sync, the same gap must be used for record and playback. Having an improved linearity allows more audio generations of dubbing to be done before the distortion accumulates to disasterous levels.

First-order intermodulation distortion is reduced by predistortion to the same extent as is harmonic distortion. Second-order effects are unaffected, and higher order effects gets worse, but are usually down in the noise.

I know of three ways to generate the cubic record distortion:

1. Back-to-back diodes shunting the feedback path of an amplifier, thereby stretching peaks. This method was used in AVR-1, ACR-25, VPR-2, VPR-6.

2. A number of biased-off dual matched transistors are sequentially turned on as the signal amplitude rises, increasing the gain on peaks. This was used on the AVR-3.

3. Two four-quadrant multipliers can be connected to generate the cube of the input to them, in this case record audio. This was used in an accessory for the AVR-2, and in the VPR-3.

During playback, there is a group delay distortion effect which is entirely a time distortion, not proportional to amplitude. In audio systems, this is minimized by making each alternate copy while moving the tape in reverse, tending to cancel the time distortion each pair of generations. This method is not available on video machines, so in many cases they have an all-pass second-order network to time-distort the signal before recording.

The AVR-1 and AVR-3 used separate circuits to do delay predistortion. The ATR-100, ATR-124, VPR-3, VPR-6, VPR-2 use a patented record equalizer which performs delay predistortion while adjusting record frequency response equalization.

AUDIO PWAs; REFERENCE LEVELS:

All levels in the Audio system are referenced in dBu. dBu is a voltage relative reference level and is defined as;

$$0dBu = 0dBm$$

Since 0dBm is defined as the power level of 1mW in 600 then 0dBu is calculated as the voltage that will produce 1mW in 600 .

$$P = \frac{V^2}{R}$$

$$1mW = \frac{V^2}{600}$$

$$V^2 = (1 \times 10^{-3}) \times 600$$

$$V = 774mV$$

The other major references used in the VPR3 are -3dBu and -8dBu.

These can be calculated from;

$$dB = 20 \log \frac{Vo}{Vi}$$

Therefore:-

$$-3dBu = 20 \log \frac{Vo}{774} mV$$

$$\text{antilog} \frac{-3}{20} = \frac{Vo}{774} mV$$

$$0.708 = \frac{Vo}{774} mV$$

$$Vo = 548mV$$

Hence;

$$-3dBu = 548mV \text{ RMS}$$

$$-8dBu = 308mV \text{ RMS}$$

VPR-3 AUDIO CONTROL

1. The functions of the Audio Control Board, PWA 12, are:
   - Decode system data bus information for the signal system, AST, and color framer.
   - Convert audio record and erase commands on the system data bus and the audio control **J** bus into a recirculating string of 16 serial words sent to the four audio boards.
   - Convert the audio set-up information stored in memory and put on the system data bus in AUDIO SET-UP mode on the system data bus into a recirculating string of 16 serial words which are sent to the four audio boards.
     1. Convert audio board's analog response to audio set-up information into an eight bit word that is written to the system data bus.
   - Convert miscellaneous audio control information into a recirculating serial data word which is sent to the four audio boards.
   - Send audio status information back on the system data bus to system control.
   - Decode audio monitor switching information from the system data bus.
   - Audio functions:
     1. Reference audio frequency generator.
     2. Sine wave synthesizer (1 and 10kHz) for audio set-up.
     3. Signal processing circuitry for audio set-up.
     4. Drive circuits for control track, video, and sync erase heads.

2. System control communicates with Audio Control by placing a hexadecimal address between **80** and **87** on the system address bus. U85 (sh 3-G8) decodes the **8** to enable the bus communication circuits.

U 74 decodes the individual addresses for the board. U74-15 (Y0) corresponds to address 80 Hex; U74-15 (Y1) to 81, etc.

U63 and U51 (sh 3-D,E-7/8) buffer and control the direction of data to and from the system data bus. There are several latches dedicated to latching in data from the bus at specific addresses.

3. Since system control Data and Address bus end at AUDIO CONTROL PWA 12, an important function of the board is to decode commands for the video signal system. Address **82H** (video bus) latches information into U50. Record and erase commands are not updated until the audio board receives a command strobe from System Control. U 49 is the buffer latch. The Data bit and corresponding pin on U50 are:

DATA BIT/U50	COMMAND NAME
0/2	COLOR FRAME ENABLE (+)
1/5	VIDEO ERASE (+), buffered by U49.
2/6	SHUTTLE (+). This signal is modified on AST PWA 7, and goes to Signal System and the Time Base Corrector as AST RANGE.
3/9	VIDEO TAPE (+)/EE (-). This is modified on Equalizer PWA 3 by a switch before going to the Mod/Demod PWA's.
4/12	VIDEO RECORD (+) is buffered by U49.
5/15	CONTROL TRACK (CT) RECORD (+) is buffered by U49.
6/16	EDITOR ON (+).
7/19	SYNC HEAD RECORD (+) is buffered by U49.

The data latch for monitor/control address **84H** is U62. The output pins on U62 correspond to the following commands:

DATA BIT/PIN	COMMAND NAME
0/2	SYNC ERASE (+), buffered and latched into U49.
1/5	FIELD(+)/FRAME(-), to AST Servo.
2/6	PLAY HEAD(+)/RECORD HEAD(-). Record head playback is automatically selected in EDIT PREVIEW mode. It may be selected on the VIDEO SET-UP menu for interchange adjustments.
3/9	VIDEO TAPE(+)/EE(-). This command is routed through the switch on RF EQUALIZER PWA 3 to the MODULATOR and DEMODULATOR PWA's.
4/12	STOP.
5/15	VIDEO MONITOR SWITCHING A
6/16	VIDEO MONITOR SWITCHING B
7/19	VIDEO MONITOR SWITCHING C. This three bit code A, B & C is generated by the control panel monitor select buttons, and is decoded on PWA 1 and PWA 3 to select the displays on the Waveform and Picture monitors.

4. Address **80H** latches audio record and erase commands into U84. A command strobe from the control board latches these commands into U83. The output pins on U84 correspond to the following commands:

DATA BIT/U84 PIN	COMMAND NAME
0/2	AUDIO 1 ERASE (+)
1/5	AUDIO 2 ERASE (+)
2/6	AUDIO 3 ERASE (+)
3/9	AUDIO 4 ERASE (+)
4/12	AUDIO 1 RECORD (+)
5/15	AUDIO 2 RECORD (+)
6/16	AUDIO 3 RECORD (+)
7/19	AUDIO 4 RECORD (+)

The data latch for address **81H** is U73.

DATA BIT/U73 PIN	COMMAND NAME
0/2	AUDIO 1 TAPE (+)/EE (-)
1/5	AUDIO 2 TAPE (+)/EE (-)
2/6	AUDIO 3 TAPE (+)/EE (-)
3/9	AUDIO 4 TAPE (+)/EE (-)
4/12	AUDIO 1 MUTE (-)
5/15	AUDIO 2 MUTE (-)
6/16	AUDIO 3 MUTE (-)
7/19	AUDIO 4 MUTE (-)

The RECORD and ERASE commands from buffer latch U83 go to dual 4 x 1 line selector U82. The TAPE/EE and MUTE commands go to dual 4 x 1 line selector U72. The four outputs of the two line selectors are the parallel input to shift register U47, whose serial output is designated **DA.** The two bit address to the line selectors are the two most significant bits of the **J** bus, **J0** and **J1.**

The **J** Bus is an internal four line address bus. **J0** is the most significant bit, **J3** the LSB. They are the other four parallel inputs to eight bit shift register U47.

J0 and J1 are used to address one of the four audio boards. J2 and J3 are used during set-up mode to designate the set-up function being performed, or the digital data being sent to the audio boards to establish the record parameters - record level, bias, equalization, and pre-distortion.

The audio board connectors are hard wired to determine the address (board number), so that individual audio boards decode only the commands and data applicable to their address.

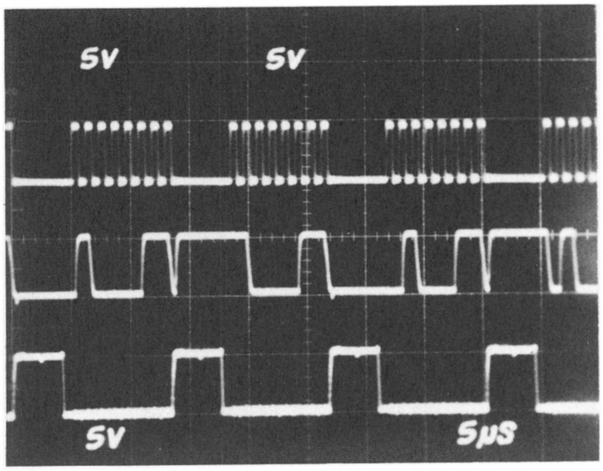
The serial bus designated **DA** is continuously circulating sixteen eight bit words (16 bytes) in the following format:

- D8 - Audio board address MSB
- D7 - Audio board address LSB
- D6 - Set-up function MSB
- D5 - Set-up function LSB

00	Bias
01	Record Level
10	Equalization
11	Pre-distortion

- D4 - Erase
- D3 - Record
- D2 - Tape/EE
- D1 - Mute

VPR-3 AUDIO CONTROL PWA 12
"DA" SERIAL BUS

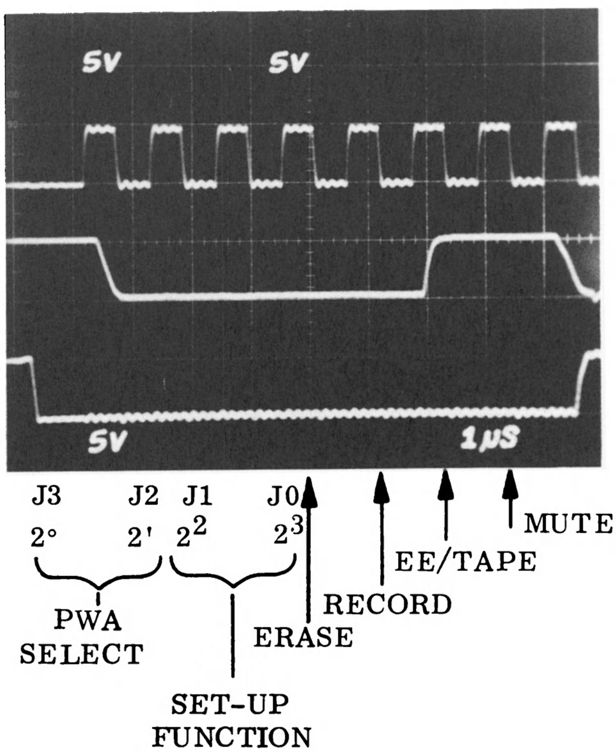


SCOPE TRIGGER: 12T6 "J0"

WF1 Pin 50 Φ D Serial Clock

WF3 Pin 53 "DA" Serial Data

WF2 Pin 46 "HOLD"



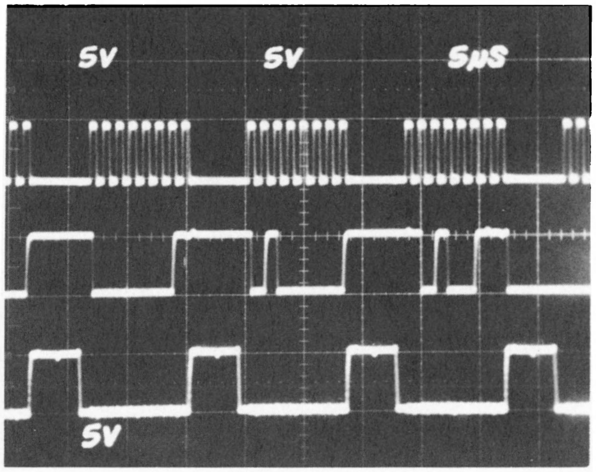
WF1 Pin 50: Φ D Clock

WF3 Pin 53: "DA" Serial Data

WF2 Pin 46: "HOLD"

A2 Data
ERASE: Low, OFF
RECORD: LOW, OFF
EE/TAPE: High, EE
MUTE: High, no Mute
Bias is Set-up function

VPR-3 AUDIO CONTROL PWA 12
"DC" SERIAL BUS
A-POT SET-UP MODE

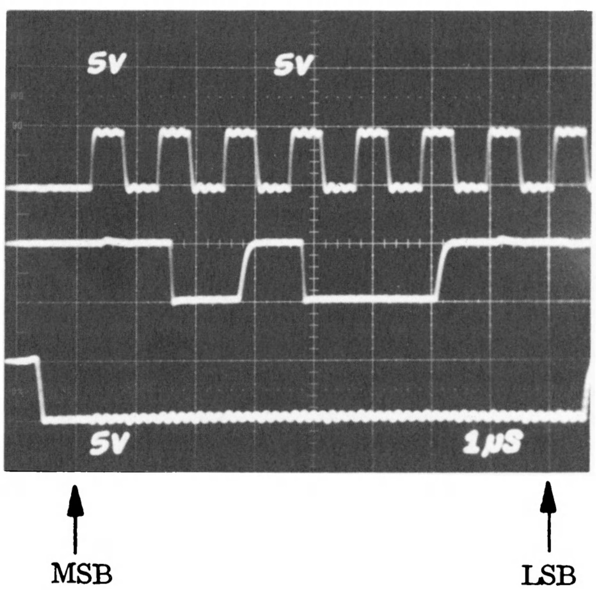


SCOPE TRIGGER 12 TP6 "J0"

WF1 Pin 50: Φ D Serial Clock

WF5 Pin 54: "DC" Serial Data

WF2 Pin 46: "HOLD"

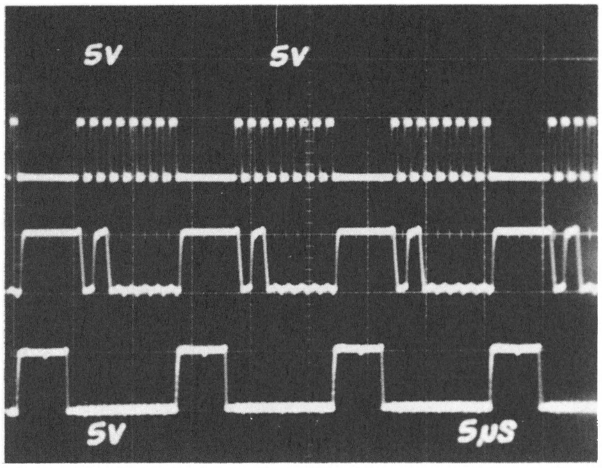


WF1 Pin 50: Φ D Serial Clock

WF5 Pin 54: "DC" Serial Data

WF2 Pin 46: "HOLD"

VPR-3 AUDIO CONTROL PWA 12
"DE" SERIAL BUS

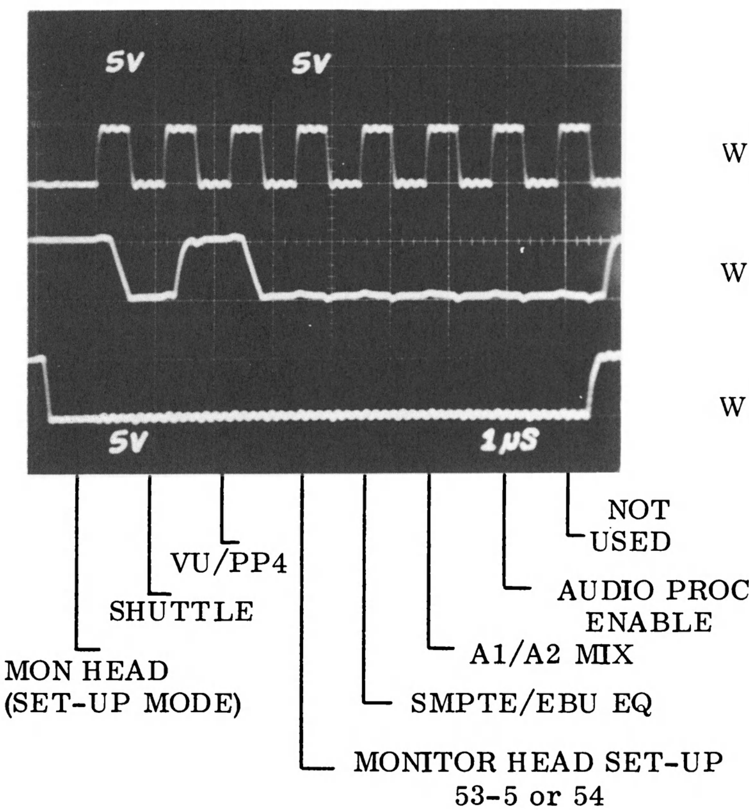


SCOPE TRIGGER: 12 TP6: "J0"

WF1 Pin 50: Φ D Serial Clock

WF4 Pin 49: "DE" Serial Data

WF2 Pin 46: "HOLD"

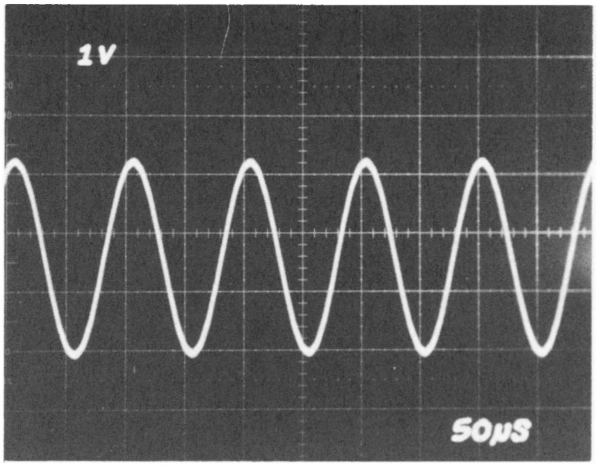


WF1 Pin 50: Φ D Serial Clock

WF4 Pin 49: "DE" Serial Data

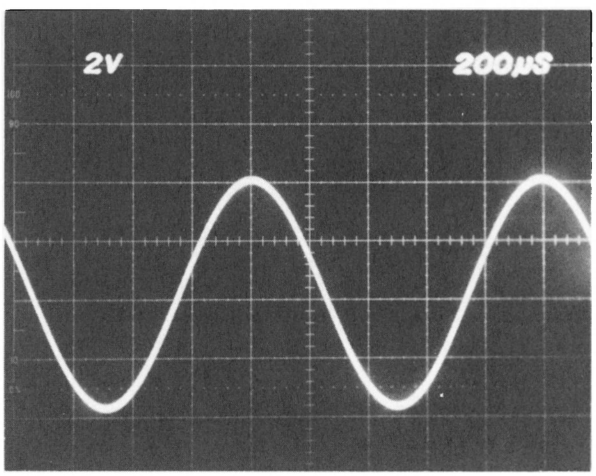
WF2 Pin 46: "HOLD"

VPR-3 AUDIO CONTROL PWA 12



WF9 Pin 20: Oscillator Out

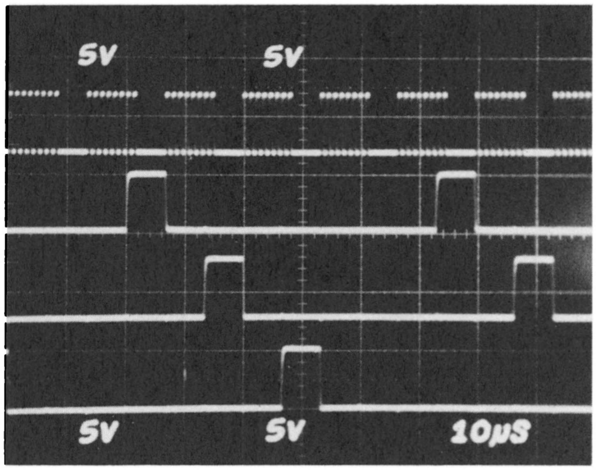
VPR-3 in TAPE 1 Set-Up,
Audio 1, Bias, Knob.



WF9 Pin 20: Test Oscillator Out

VPR-3 in TAPE 1, Set-Up,
Audio 1, Pre-Distort, Knob.

VPR-3 AUDIO CONTROL PWA 12



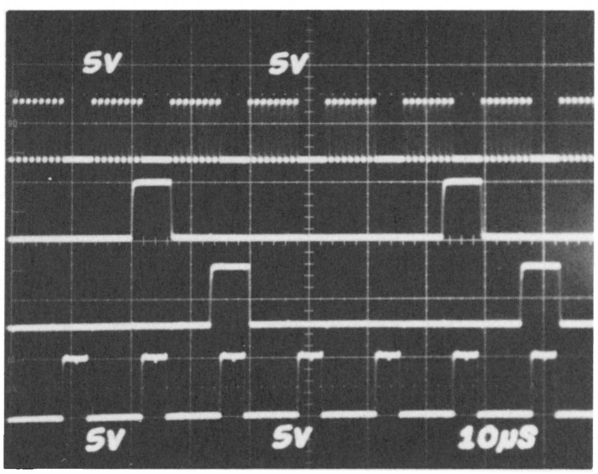
SCOPE TRIGGER J TP6 "J0"

WF1 Pin 50: Φ D Serial Clock

WF6 Pin 60: Audio Strobe 1

WF7 Pin 59: Audio Strobe 2

WF8 Pin 58: Audio Strobe 3



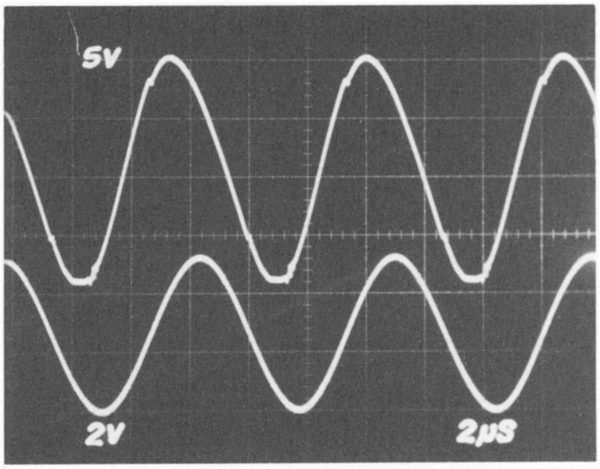
WF1 Pin 50: Φ D Serial Clock

WF6 Pin 60: Audio Strobe 1

WF7 Pin 59: Audio Strobe 2

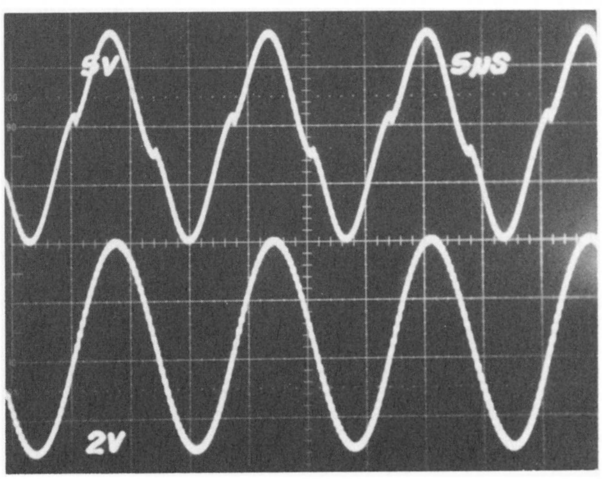
WF2 Pin 46: "HOLD"

VPR-3 AUDIO CONTROL PWA 12



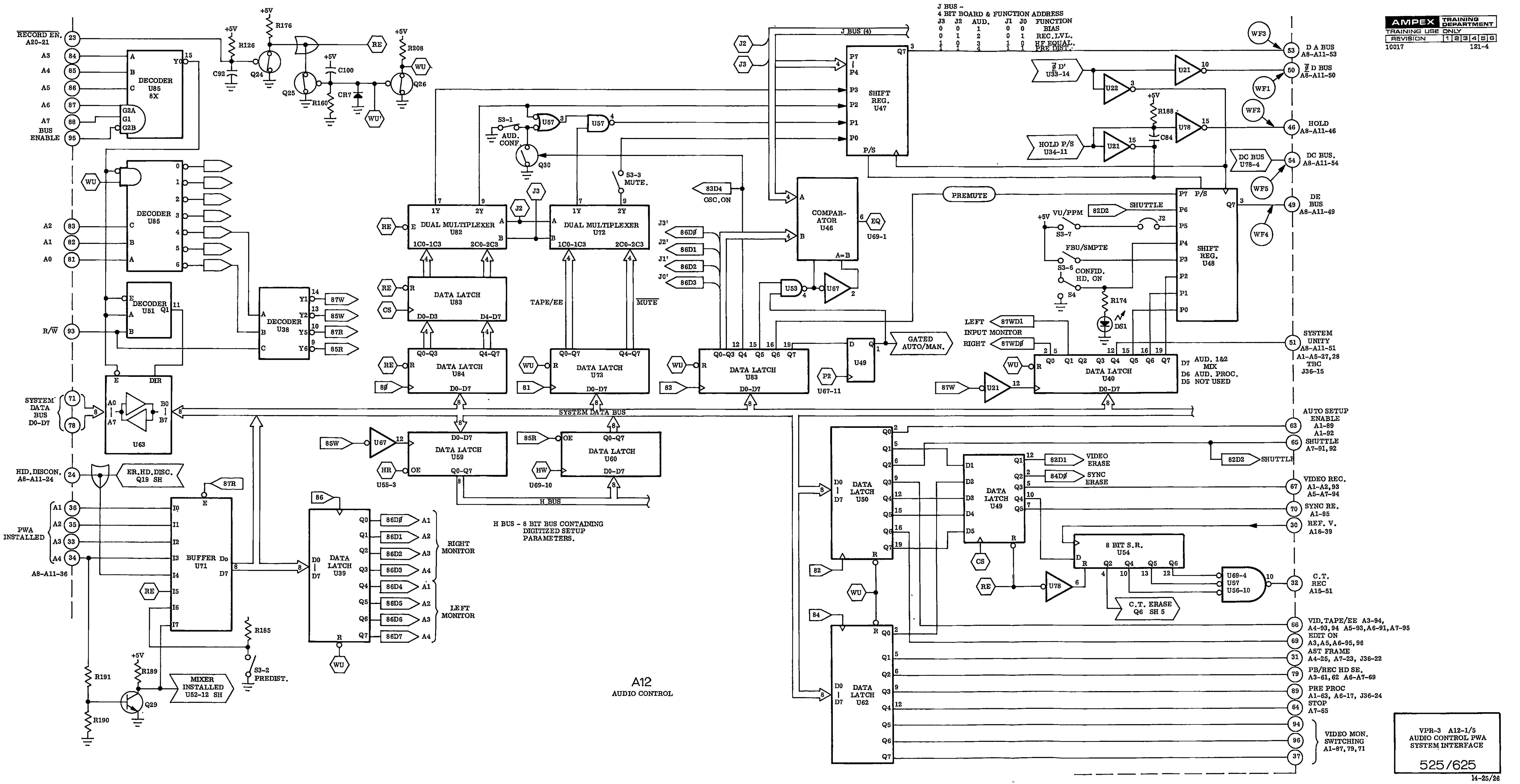
WF10 12TP1: Control Track Erase Drive

WF11 12TP2: Control Track Erase Head Current (VPR-3 in RECORD)

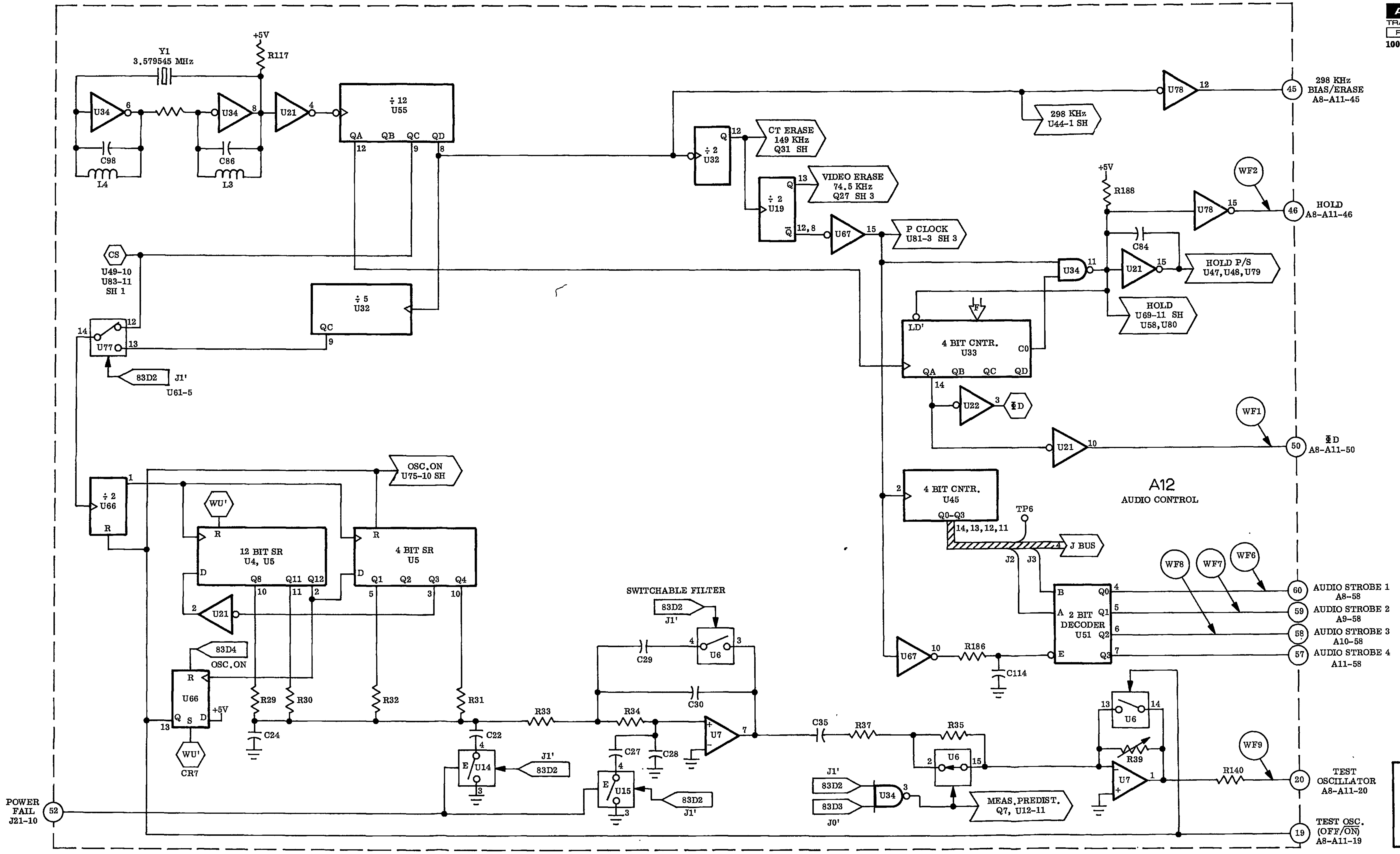


WF12 12TP4: Video Erase Drive

WF13 12TP3: Video Erase Head Current (VPR-3 in RECORD)



AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
121-4
RECORD EN. A20-21
BUS ENABLE
DECODER U85 8X
DECODER U85
DECODER U51
DECODER U38
R/W
SYSTEM DATA BUS D0-D7
U63
HID.DISCON. A8-A11-24
ER.HD.DISC. Q19 SH
PWA INSTALLED
A8-A11-36
BUFFER U71
DATA LATCH U39
RIGHT MONITOR
LEFT MONITOR
S3-2 PREDIST.
MIXER INSTALLED U52-12 SH
DUAL MULTIPLEXER U82
DUAL MULTIPLEXER U72
DATA LATCH U83
DATA LATCH U84
DATA LATCH U73
TAPE/EE
MUTE
S3-1 AUD. CONF.
S3-3 MUTE.
SYSTEM DATA BUS
DATA LATCH U59
DATA LATCH U60
H BUS
H BUS - 8 BIT BUS CONTAINING DIGITIZED SETUP PARAMETERS.
A12
AUDIO CONTROL
J BUS -
4 BIT BOARD & FUNCTION ADDRESS
J3 J2 AUD. J1 J0 FUNCTION
0 0 1 0 0 BIAS
0 1 2 0 1 REC.LVL.
1 0 3 1 0 HF EQUAL.
1 1 4 1 1 PRE DIST.
J BUS (4)
SHIFT REG. U47
COMPARATOR U46
OSC.ON
GATED AUTO/MAN.
DATA LATCH U83
DATA LATCH U40
LEFT INPUT MONITOR RIGHT
AUD. 1&2 MIX
AUD. PROC.
NOT USED
PREMUTE
SHUTTLE
VU/PPM
S3-7
FBU/SMPTE
S3-6 CONFID. HD. ON
SHIFT REG. U48
DS1
D A BUS A8-A11-53
D BUS A8-A11-50
HOLD A8-A11-46
HOLD P/S U34-11
DC BUS U78-4
DC BUS. A8-A11-54
DE BUS A8-A11-49
SYSTEM UNITY A8-A11-51 A1-A5-27,28 TBC J36-15
AUTO SETUP ENABLE A1-89 A1-92
SHUTTLE A7-91,92
DATA LATCH U50
DATA LATCH U49
VIDEO ERASE
SYNC ERASE
VIDEO REC. A1-A2,93 A5-A7-94
SYNC RE. A1-95
REF. V. A16-39
8 BIT S.R. U54
C.T. ERASE Q6 SH 5
C.T. REC A15-51
DATA LATCH U62
VID.TAPE/EE A3-94, A4-93,94 A5-93,A6-91,A7-95
EDIT ON A3,A5,A6-95,96
AST FRAME A4-25, A7-23, J36-22
PB/REC HD SE. A3-61,62 A6-A7-69
PRE PROC A1-63, A6-17, J36-24
STOP A7-65
VIDEO MON. SWITCHING A1-87,79,71
VPR-3 A12-1/5
AUDIO CONTROL PWA
SYSTEM INTERFACE
525/625
14-25/26



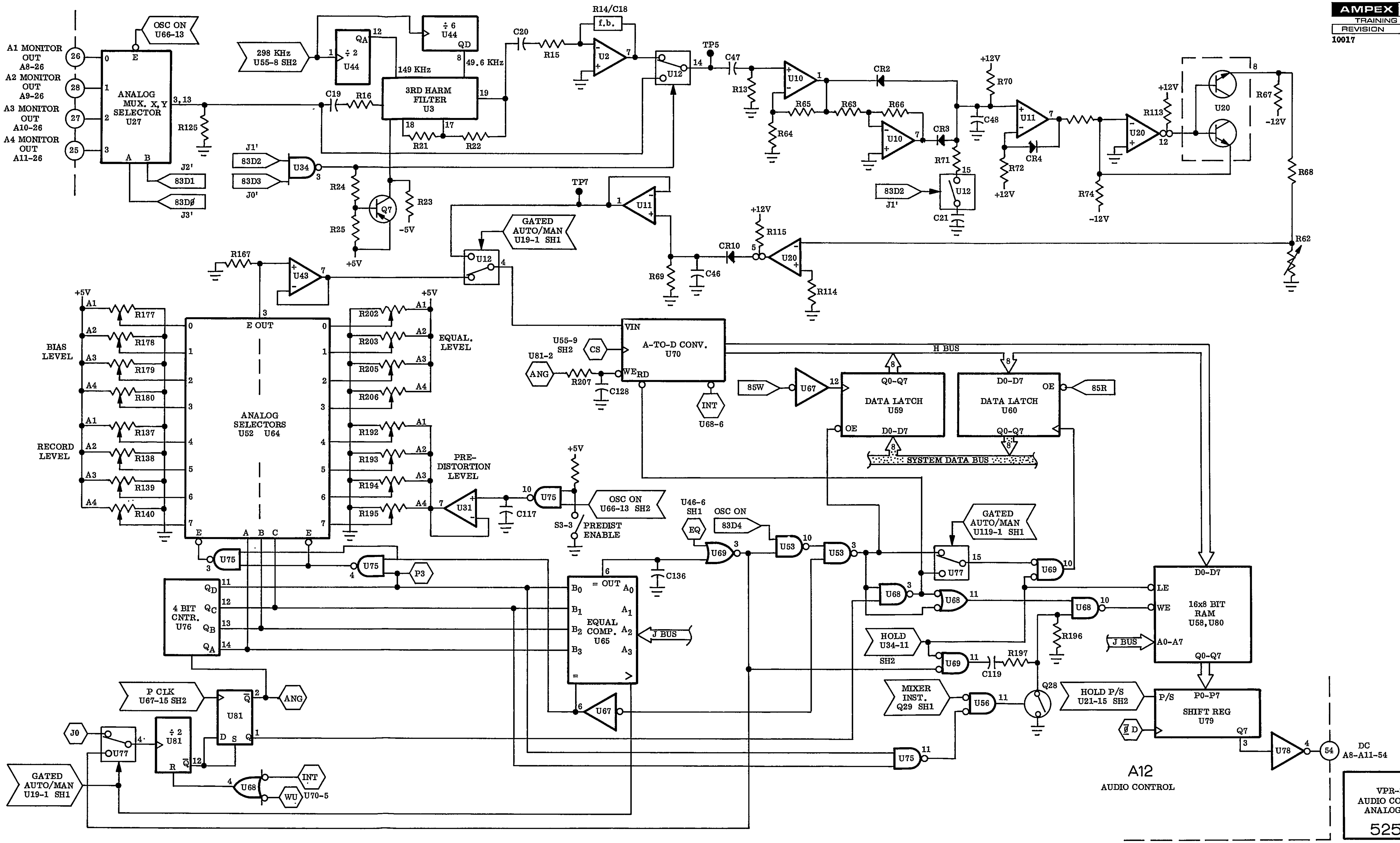
VPR-3 - A12-2/5
AUDIO CONTROL PWA
MASTER OSC, CLOCK &
TEST OSCILLATOR

525/625

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY

REVISION	1	2	3	4	5	6

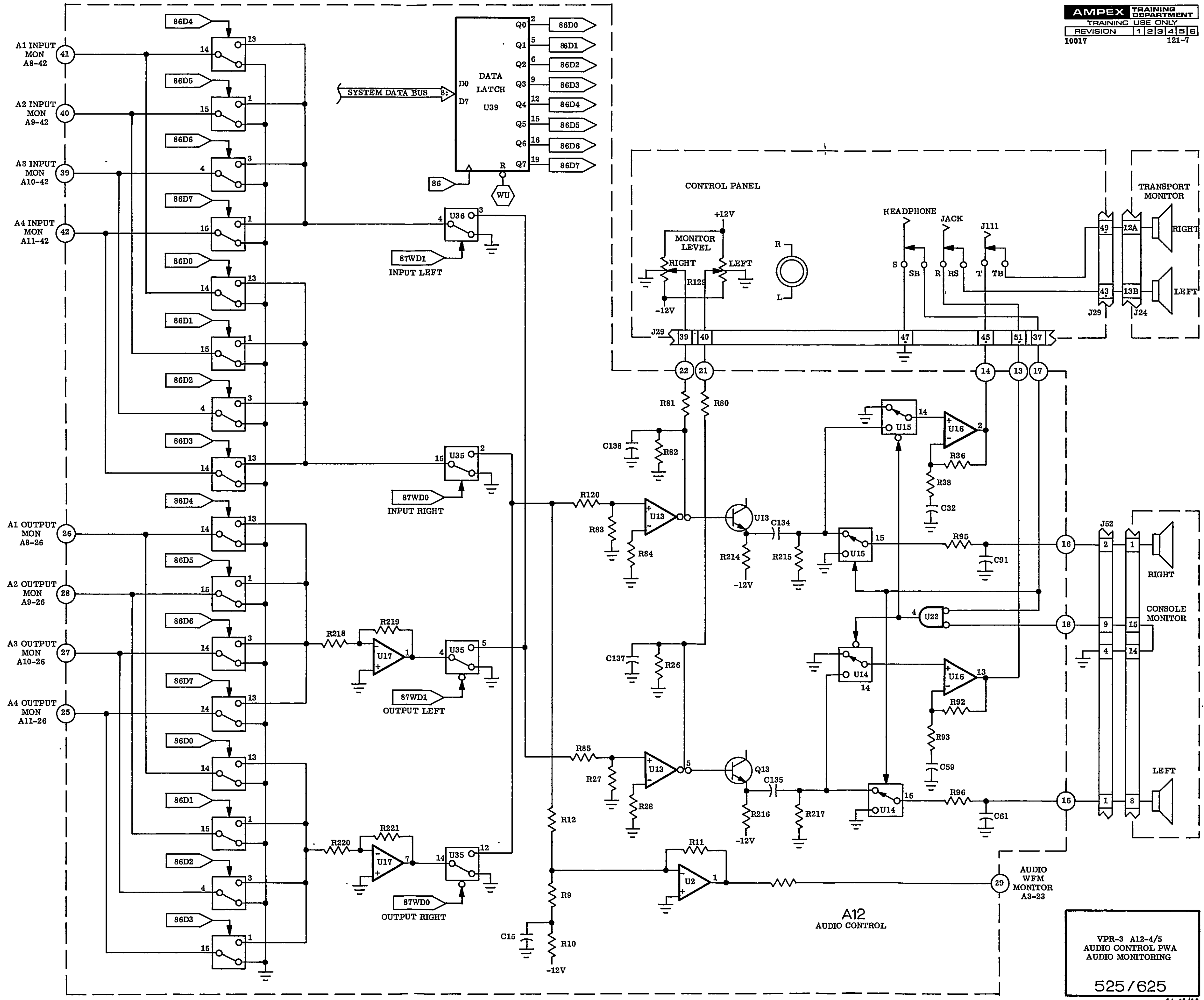
10017 121-6

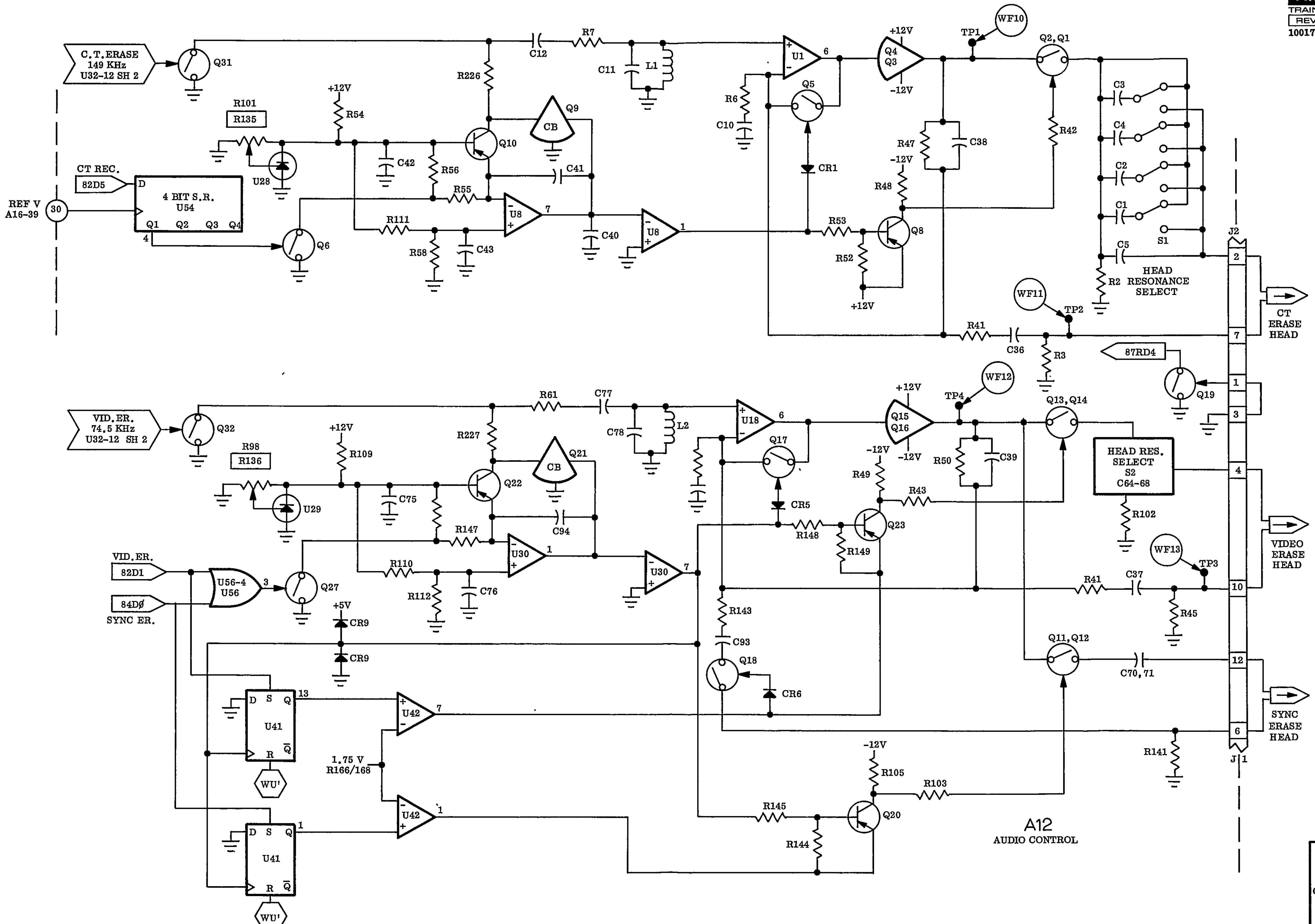


A12
AUDIO CONTROL

VPR-3 A12-3/
AUDIO CONTROL PWA
ANALOG CONTROL
525/625

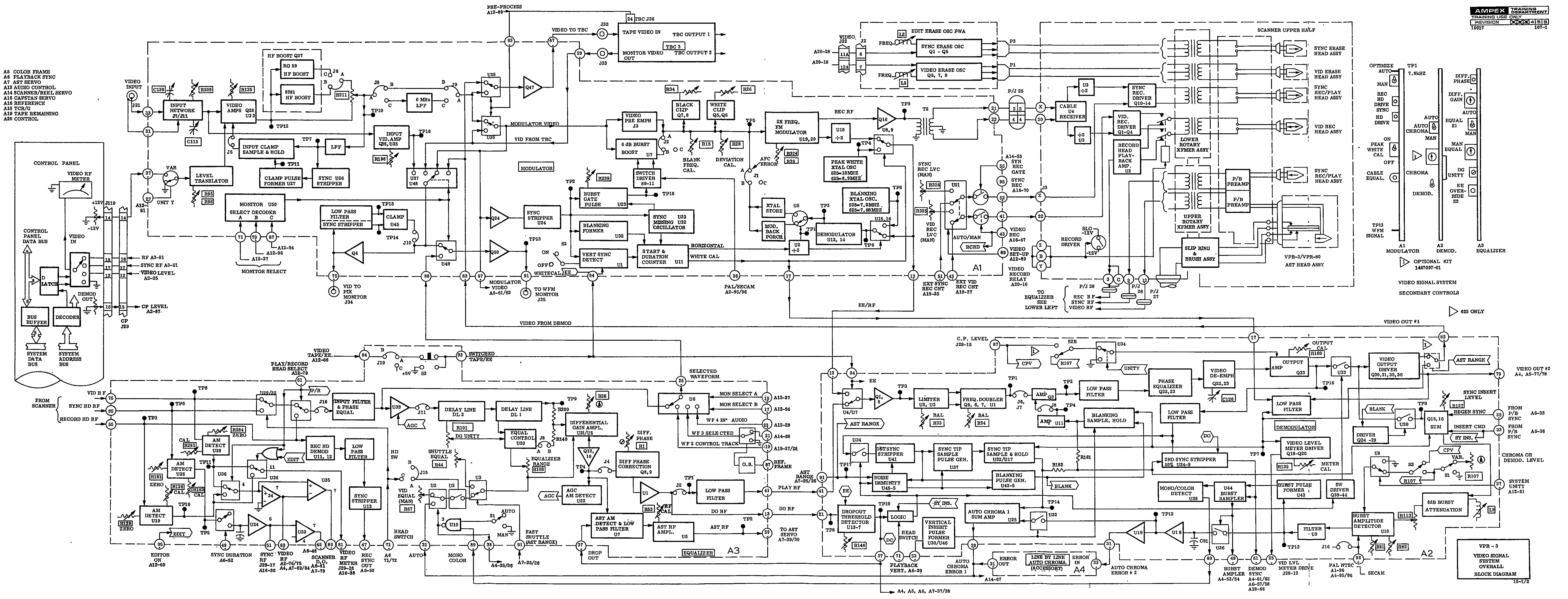
14-29/30

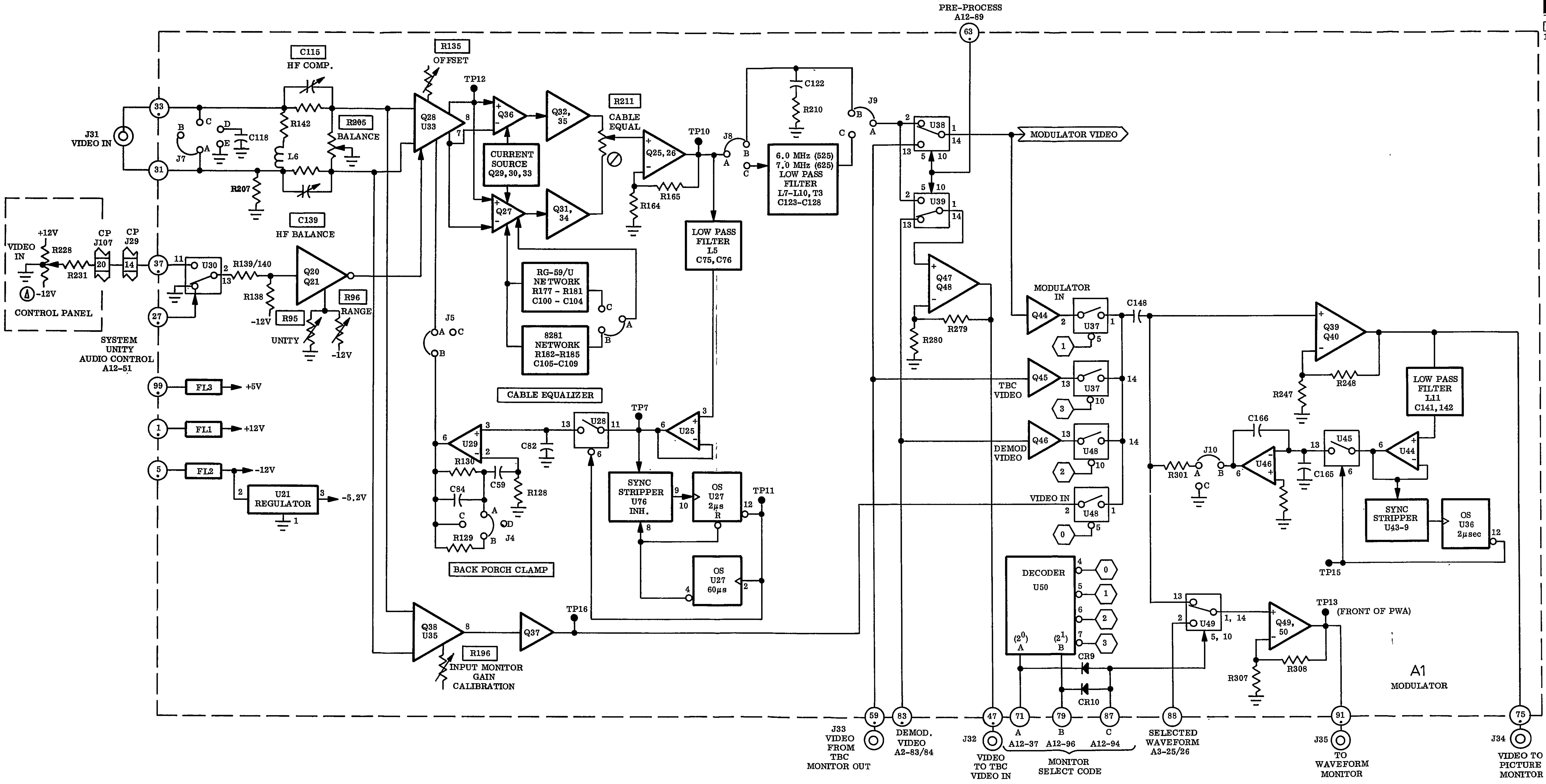

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
121-7
A1 INPUT MON A8-42
A2 INPUT MON A9-42
A3 INPUT MON A10-42
A4 INPUT MON A11-42
A1 OUTPUT MON A8-26
A2 OUTPUT MON A9-26
A3 OUTPUT MON A10-26
A4 OUTPUT MON A11-26
SYSTEM DATA BUS
DATA LATCH U39
INPUT LEFT
INPUT RIGHT
OUTPUT LEFT
OUTPUT RIGHT
CONTROL PANEL
MONITOR LEVEL
HEADPHONE JACK
J111
TRANSPORT MONITOR
RIGHT
LEFT
CONSOLE MONITOR
AUDIO WFM MONITOR A3-23
A12
AUDIO CONTROL
VPR-3 A12-4/5
AUDIO CONTROL PWA
AUDIO MONITORING
525/625
14-31/32



VPR-3 A12-5/5
AUIDO CONTROL PWA
C.T., VIDEO, SYNC ERASE

525/625

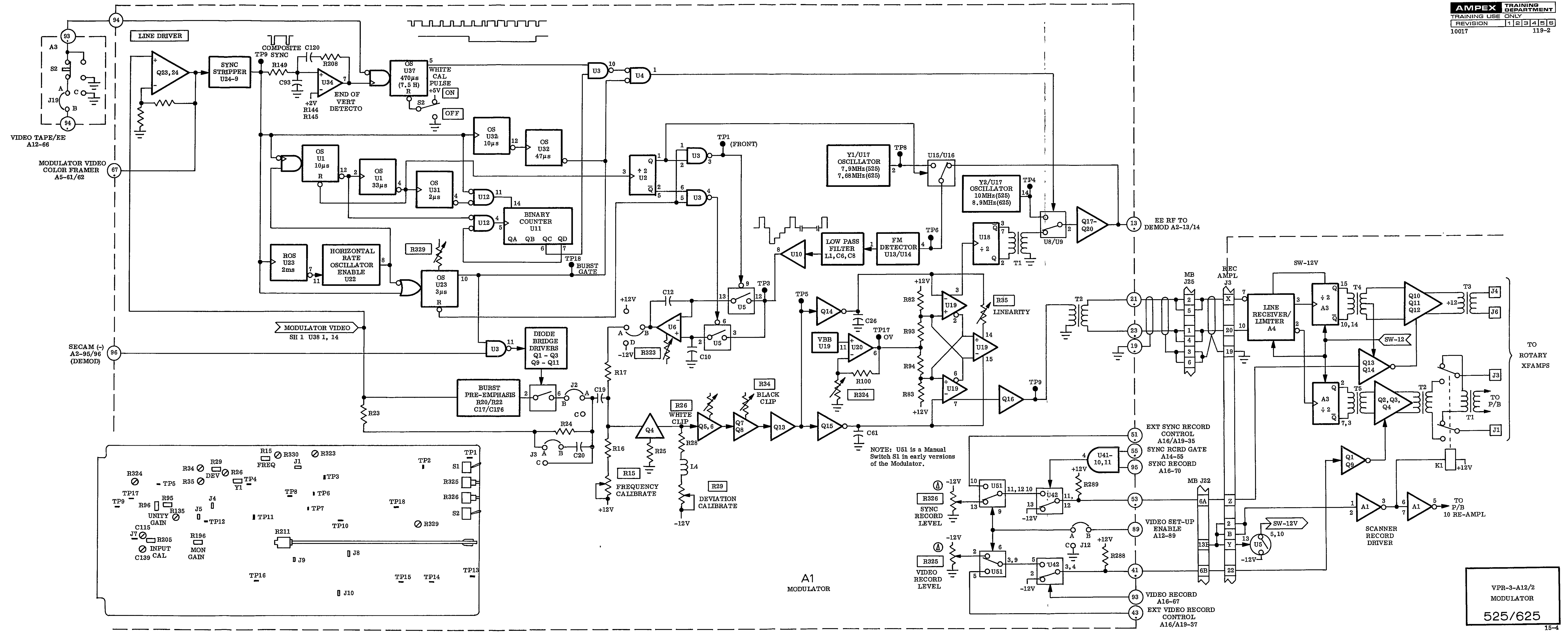

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION
10017
107-1
A5 COLOR FRAME
A6 PLAYBACK SYNC
A7 AST SERVO
A13 AUDIO CONTROL
A14 SCANNER/REEL SERVO
A15 CAPSTAN SERVO
A16 REFERENCE
A18 TCR/G
A19 TAPE REMAINING
A20 CONTROL
CONTROL PANEL
VIDEO RF METER
CONTROL PANEL DATA BUS
VIDEO IN
LATCH
BUS BUFFER
DECODER
SYSTEM DATA BUS
SYSTEM ADDRESS BUS
DEMOD OUT
CP LEVEL A2-87
CP J29
RF A3-81
SYNC RF A3-51
VIDEO LEVEL A2-25
VIDEO INPUT
INPUT NETWORK J7/J11
VIDEO AMPS Q28 U33
HF BOOST Q27
RG 59 HF BOOST
8281 HF BOOST
6 MHz LPF
INPUT CLAMP SAMPLE & HOLD
LPF
INPUT VID. AMP Q38, U35
CLAMP PULSE FORMER U27
SYNC U26 STRIPPER
LEVEL TRANSLATOR
MONITOR U50 SELECT DECODER
MONITOR SELECT
LOW PASS FILTER SYNC STRIPPER
CLAMP U45
PRE-PROCESS A12-89
VIDEO TO TBC
TAPE VIDEO IN
MONITOR VIDEO OUT
TBC 3
TBC OUTPUT 1
TBC OUTPUT 2
TBC J36
MODULATOR VIDEO
VID FROM TBC
MODULATOR
VIDEO PRE EMPH J3
6 dB BURST BOOST U7
BLACK CLIP Q7, 8
WHITE CLIP Q5, Q6
BLANK FREQ. CAL.
DEVIATION CAL.
2X FREQ. FM MODULATOR U19, 20
REC RF
AFC ERROR
PEAK WHITE XTAL OSC. 625=10MHZ 625=8.9MHZ
XTAL STORE
MOD. BACK PORCH
DEMODULATOR U13, 14
BLANKING XTAL OSC.
SWITCH DRIVER
BURST GATE PULSE U23
SYNC STRIPPER U24
SYNC MISSING OSCILLATOR U23 U32
BLANKING FORMER U32
VERT SYNC DETECT U1
START & DURATION COUNTER U11
HORIZONTAL
WHITE CAL
WHITECAL EE
VID TO PIX MONITOR J34
MODULATOR VIDEO A5-61/62
TO WFM MONITOR J35
PAL/SECAM A2-95/96
EXT SYNC REC CNT A19-35
EXT VID REC CNT A19-27
VIDEO FROM DEMOD
EE/RF
A1
EDIT ERASE OSC PWA
SYNC ERASE OSC Q1 - Q5
VIDEO ERASE OSC Q6, 7, 8
SCANNER UPPER HALF
SYNC ERASE HEAD ASSY
VID ERASE HEAD ASSY
SYNC REC/PLAY HEAD ASSY
VID REC HEAD ASSY
CABLE U4 RECEIVER
SYNC REC. DRIVER Q10-14
VID. REC. DRIVER Q1-Q4
RECORD HEAD PLAY-BACK AMP. U2
LOWER ROTARY XFMER ASSY
UPPER ROTARY XFMER ASSY
P/B PREAMP
SLIP RING & BRUSH ASSY
VPR-3/VPR-80 AST HEAD ASSY
SYNC REC LVC (MAN)
VID REC LVC (MAN)
AUTO/MAN
RCRD
SYN REC GATE
SYNC REC A16-70
VIDEO REC A16-67
VIDEO SET-UP A12-89
VIDEO RECORD RELAY A20-16
RECORD DRIVER
TO EQUALIZER SEE LOWER LEFT
REC RF
SYNC RF
VIDEO RF
OPTIMIZE
AUTO
MAN
REC HD DRIVE SYNC
HD DRIVE
PEAK WHITE CAL
CABLE EQUAL.
CHROMA
DEMOD.
TP13 WFM SIGNAL
A1 MODULATOR
A2 DEMOD.
A3 EQUALIZER
DIFF. PHASE
DIFF. GAIN
EQUAL S1
MAN EQUAL
DG UNITY
EE OVER-RIDE S2
OPTIONAL KIT 1467097-01
VIDEO SIGNAL SYSTEM SECONDARY CONTROLS
625 ONLY
VIDEO OUT #1
VIDEO TAPE/EE A12-66
SWITCHED TAPE/EE
PLAY/RECORD HEAD SELECT A12-79
SELECTED WAVEFORM
MON SELECT A
MON SELECT B
WF 4 IN AUDIO
WF 3 SELECTED
WF 2 CONTROL TRACK
FROM SCANNER
VID R F
SYNC HD RF
RECORD HD RF
INPUT FILTER & PHASE EQUAL
DELAY LINE DL 2
DELAY LINE DL 1
DG UNITY
SHUTTLE EQUAL
EQUAL CONTROL U20
EQUALIZER RANGE
DIFFERENTIAL GAIN AMPL. U21/U5
DIFF. PHASE
DIFF PHASE CORRECTION Q8, 9
AM DETECT U38
AM DETECT U28
AM DETECT U19
REC HD DEMOD U11, 12
LOW PASS FILTER
SYNC STRIPPER U13
HD SW
VID EQUAL (MAN)
AGC AM DETECT U22
AST AM DETECT & LOW PASS FILTER U7
AST RF AMPL. U5
LOW PASS FILTER
O.S.
REF. FRAME
PLAY RF
DO RF
AST RF
TO AST SERVO A7-29/30
EQUALIZER
A3
EDITOR ON A12-69
SYNC DURATION A6-52
SYNC RF J29-17 A16-36
VIDEO RF A2-76/75 A4, A7-83/84
SCANNER D.O. A6-51 A7-79
VIDEO RF METER J29-16 A16-38
REC SYNC OUT A6-50
HEAD SWITCH
MONO COLOR
FAST SHUTTLE (AST RANGE)
DROP OUT
C.P. LEVEL J29-15
CPV
UNITY
PHASE EQUALIZER Q22, 23
VIDEO DE-EMPH Q22, 23
OUTPUT AMP Q33
OUTPUT CAL
VIDEO OUTPUT DRIVER Q30, 31, 35, 36
AST RANGE
VIDEO OUT #2 A4, A5-77/78
LIMITER U2, U3
FREQ. DOUBLER Q5, 6, 7, U1
BAL
AMP U11
LOW PASS FILTER
BLANKING SAMPLE, HOLD
LOW PASS FILTER
DEMODULATOR
BLANK
DRIVER Q24 -29
SUM
SYNC INSERT LEVEL
REGEN SYNC
INSERT CMD
SY INS.
FROM P/B SYNC A6-35
FROM P/B SYNC A6-36
1ST SYNC STRIPPER U41
SYNC TIP SAMPLE PULSE GEN. U37
SYNC TIP SAMPLE & HOLD U22/U17
NOISE IMMUNITY U45-5
BLANKING PULSE GEN. U43-5
2ND SYNC STRIPPER 50% U24-9
VIDEO LEVEL METER DRIVER Q18-Q20
METER CAL
CHROMA OR DEMOD. LEVEL
SYSTEM UNITY A12-51
DROPOUT THRESHOLD DETECTOR U13-7
LOGIC
VERTICAL INHIBIT PULSE FORMER U30/U46
AUTO CHROMA 1 SUM AMP U25
MONO/COLOR DETECT U38
U44 BURST SAMPLER
BURST PULSE FORMER U43
SW DRIVER Q39-44
6dB BURST ATTENUATION
BURST AMPLITUDE DETECTOR U10
FILTER U9
AST RANGE A7-25/26
PLAYBACK VERT. A6-39
AUTO CHROMA ERROR 1
ERROR OUT
LINE BY LINE AUTO CHROMA (ACCESSORY)
ERROR IN
A4
AUTO CHROMA ERROR ÷ 2
A14-67
BURST AMPLER A4-53/54
DEMOD SYNC A4-61/62 A6-57/58 A18-66
VID LVL METER DRIVE J29-12
PAL NTSC A1-96 A4-95/96
SECAM
A2
A4, A5, A6, A7-37/38
VPR - 3 VIDEO SIGNAL SYSTEM OVERALL BLOCK DIAGRAM
15-1/2

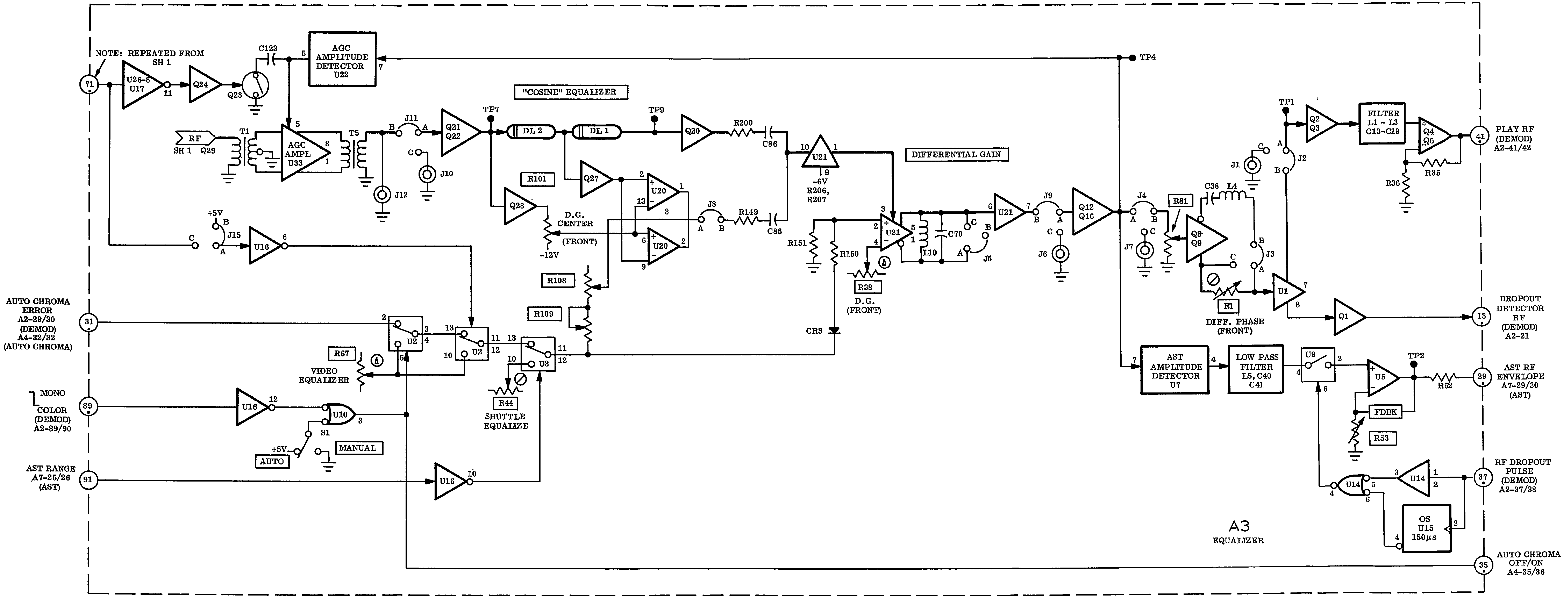


VPR-3-A1-1/2
MODULATOR
INPUT PROCESSOR

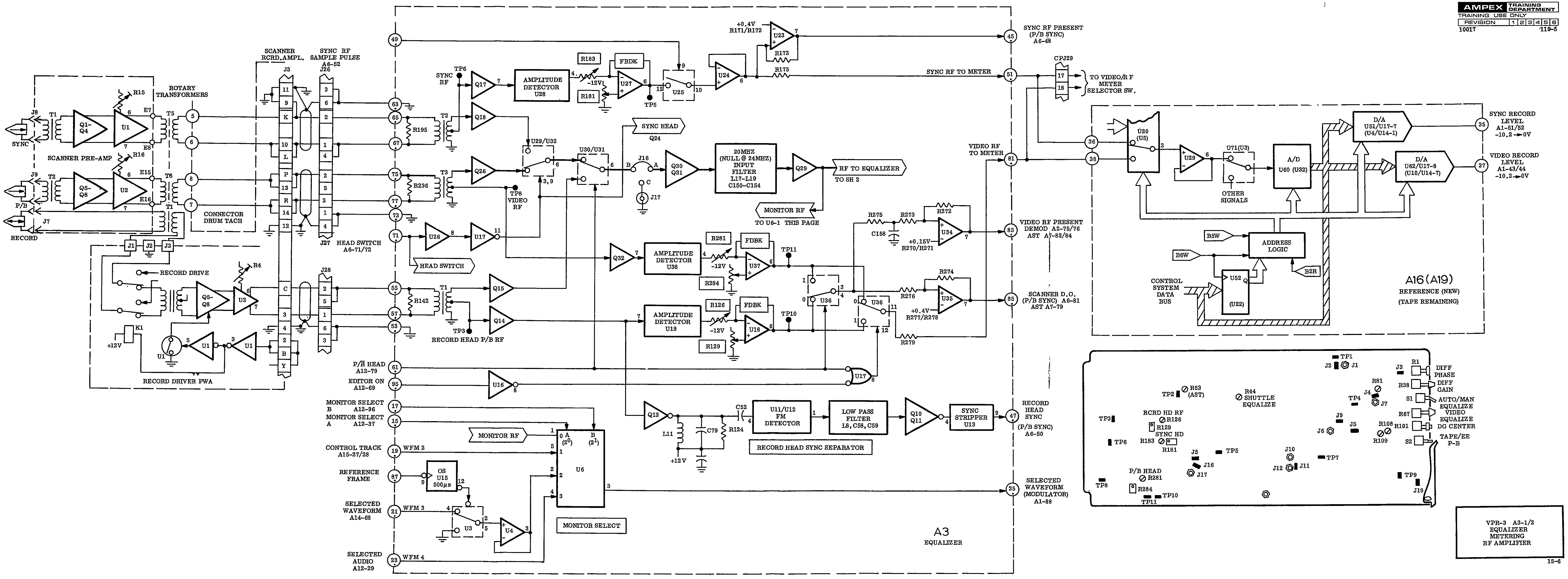
525/625

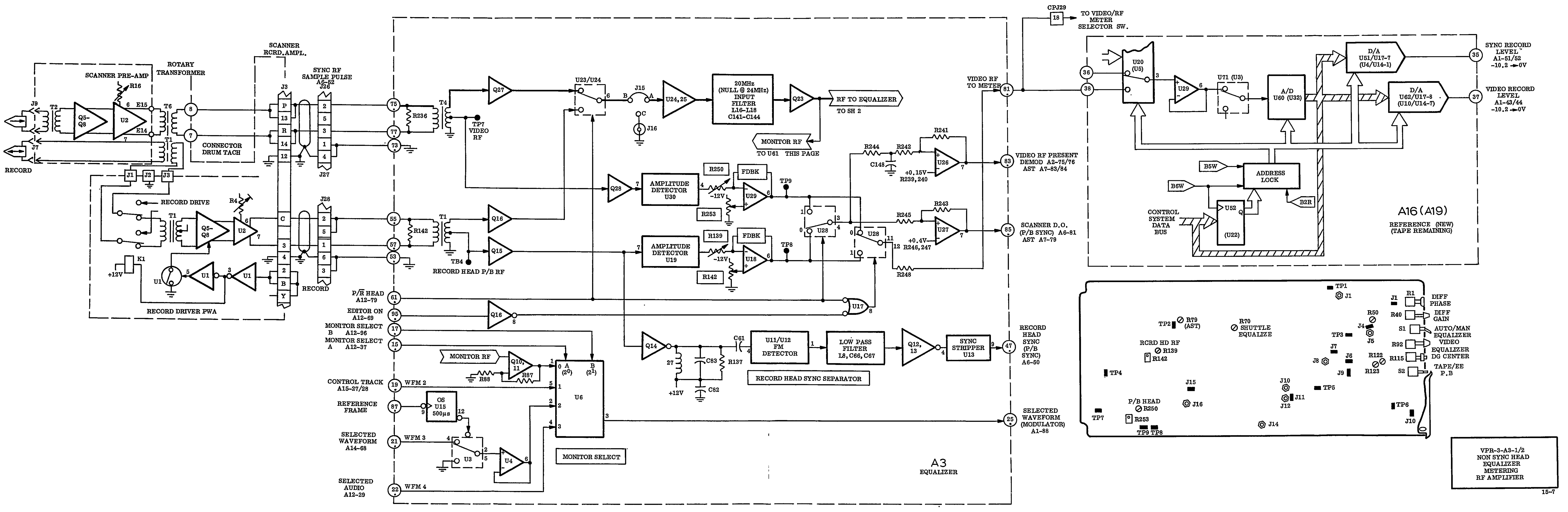
AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 119-2





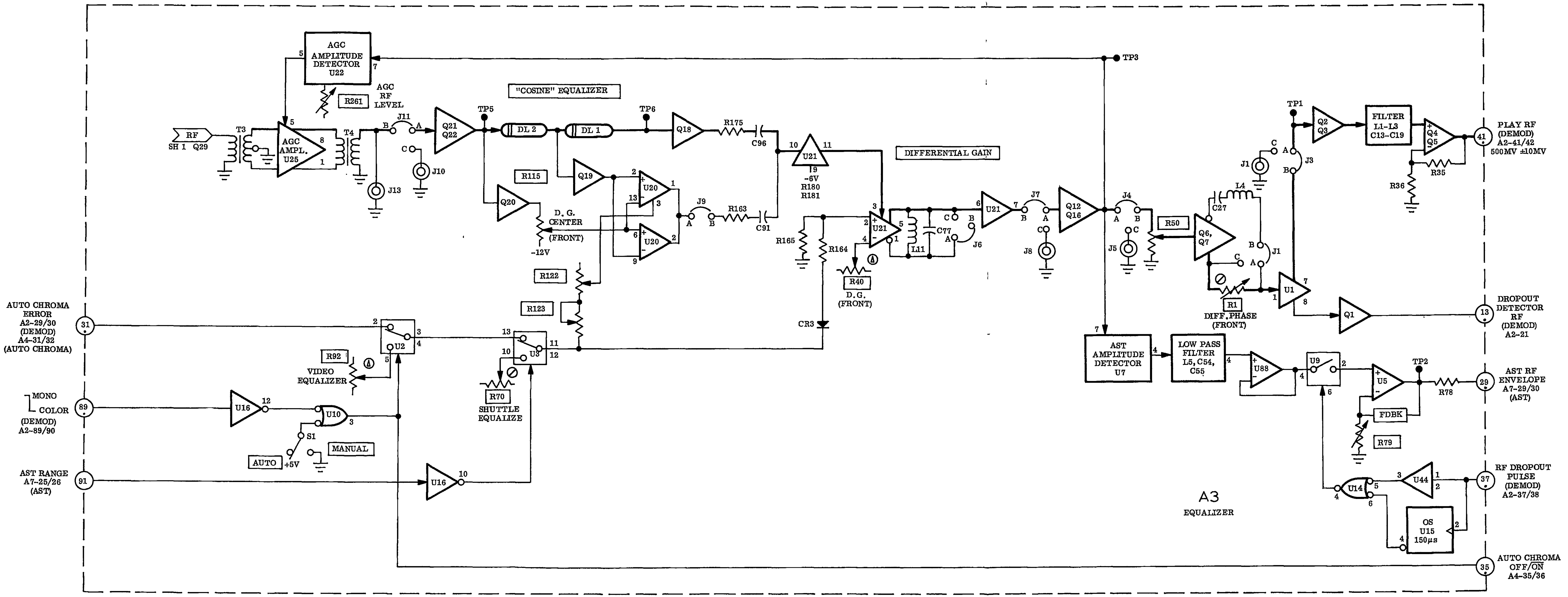
VPR-3 A3-2/2
RF EQUALIZER
525/625


AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
119-5
SYNC
P/B
RECORD
SCANNER PRE-AMP
ROTARY TRANSFORMERS
SCANNER RCRD. AMPL.
SYNC RF SAMPLE PULSE A6-52
CONNECTOR DRUM TACH
RECORD DRIVE
RECORD DRIVER PWA
HEAD SWITCH A6-71/72
HEAD SWITCH
SYNC RF
AMPLITUDE DETECTOR U28
FBDK
SYNC HEAD Q24
20MHZ (NULL @ 24MHZ) INPUT FILTER L17-L19 C150-C154
RF TO EQUALIZER
TO SH 2
MONITOR RF
TO U6-1 THIS PAGE
TP8 VIDEO RF
AMPLITUDE DETECTOR U38
AMPLITUDE DETECTOR U19
RECORD HEAD P/B RF
P/R HEAD A12-79
EDITOR ON A12-69
MONITOR SELECT B A12-96
MONITOR SELECT A A12-37
CONTROL TRACK A15-27/28
REFERENCE FRAME
SELECTED WAVEFORM A14-68
SELECTED AUDIO A12-29
OS U15 500μs
MONITOR SELECT
U11/U12 FM DETECTOR
LOW PASS FILTER L8, C58, C59
SYNC STRIPPER U13
RECORD HEAD SYNC SEPARATOR
A3 EQUALIZER
SYNC RF PRESENT (P/B SYNC) A6-48
SYNC RF TO METER
TO VIDEO/R F METER SELECTOR SW.
VIDEO RF TO METER
VIDEO RF PRESENT DEMOD A2-75/76 AST A7-83/84
SCANNER D.O. (P/B SYNC) A6-81 AST A7-79
RECORD HEAD SYNC (P/B SYNC) A6-50
SELECTED WAVEFORM (MODULATOR) A1-88
SYNC RECORD LEVEL A1-51/52 -10.2→0V
VIDEO RECORD LEVEL A1-43/44 -10.2→0V
D/A U51/U17-7 (U4/U14-1)
D/A U62/U17-8 (U10/U14-7)
A/D U60 (U32)
OTHER SIGNALS
ADDRESS LOGIC
CONTROL SYSTEM DATA BUS
A16 (A19) REFERENCE (NEW) (TAPE REMAINING)
DIFF PHASE
DIFF GAIN
AUTO/MAN EQUALIZE
VIDEO EQUALIZE
DG CENTER
TAPE/EE P-B
SHUTTLE EQUALIZE
RCRD HD RF
SYNC HD
P/B HEAD
VPR-3 A3-1/2 EQUALIZER METERING RF AMPLIFIER
15-6



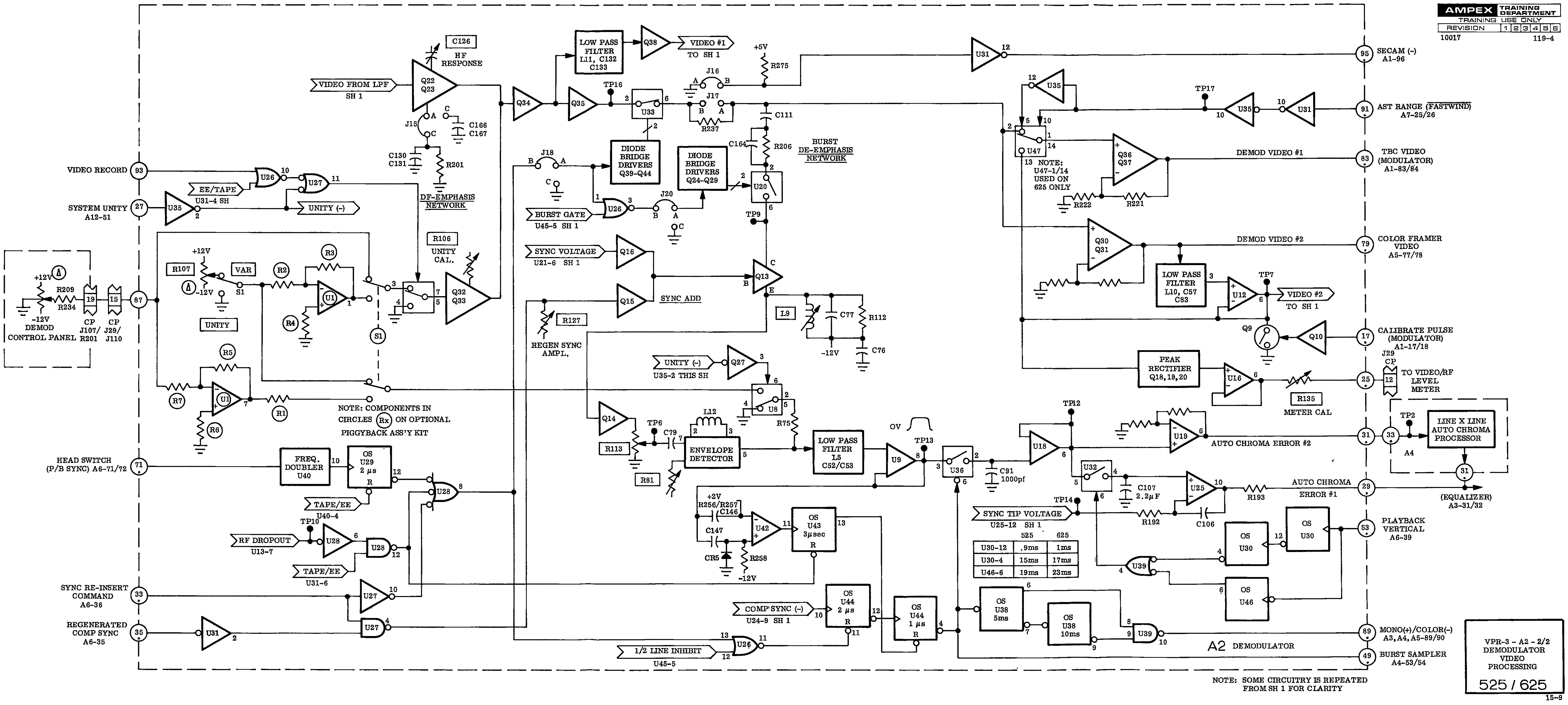
VPR-3-A3-1/2
NON SYNC HEAD
EQUALIZER
METERING
RF AMPLIFIER

15-7

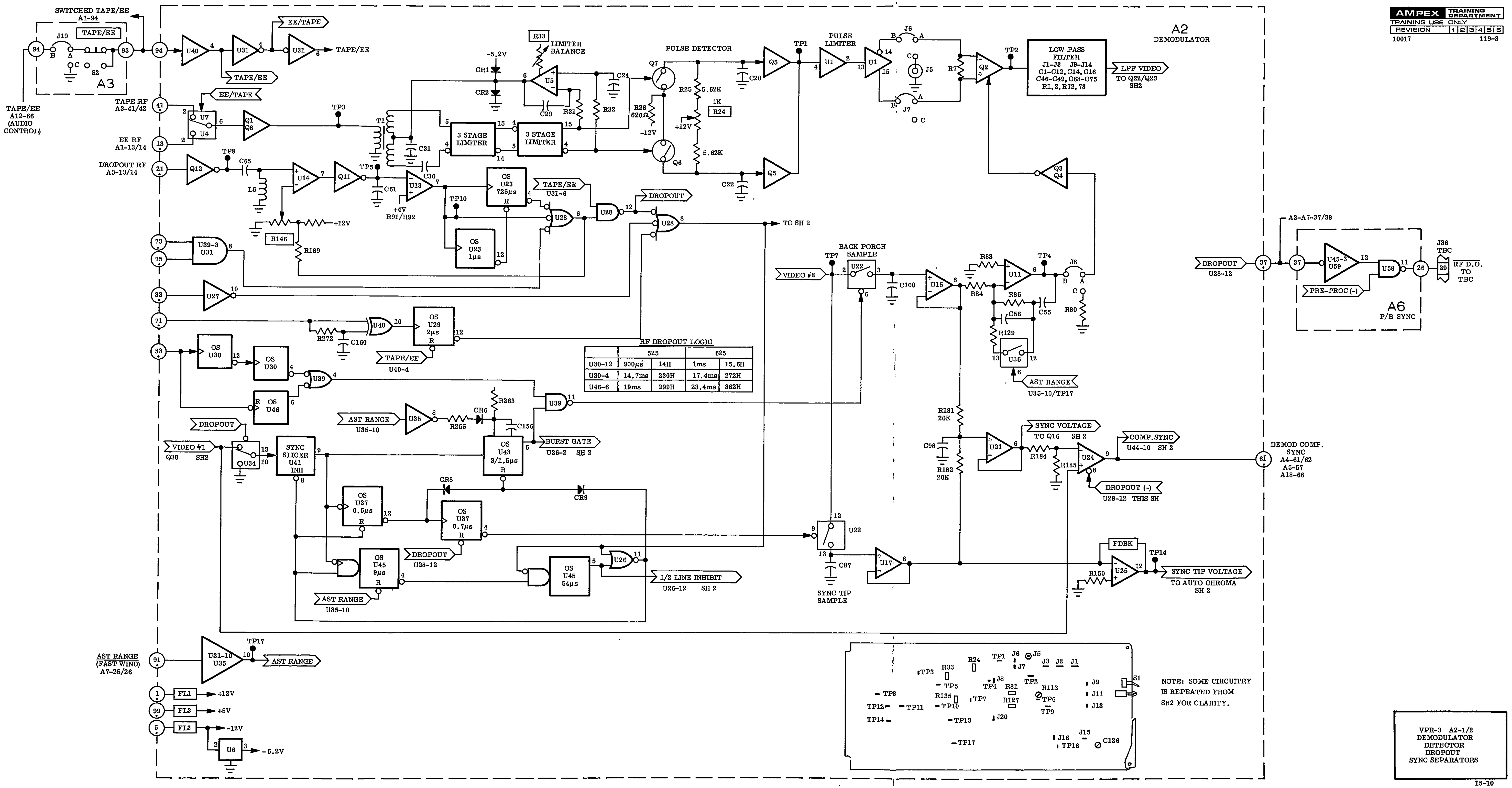


VPR-3-A3-2/2
NON SYNC HEAD
RF EQUALIZER

525/625



	525	625
U30-12	.9ms	1ms
U30-4	15ms	17ms
U46-6	19ms	23ms

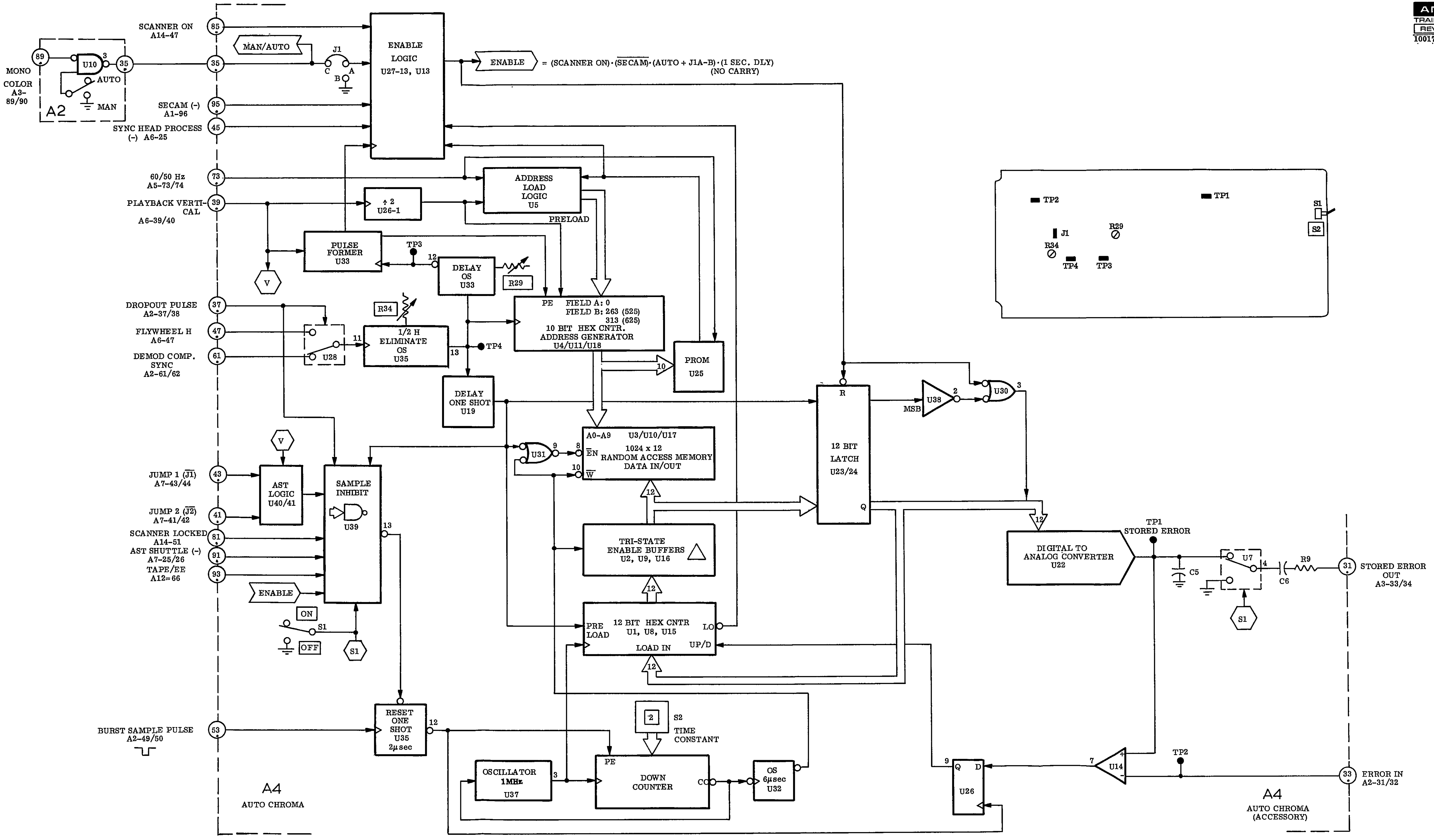


RF DROPOUT LOGIC

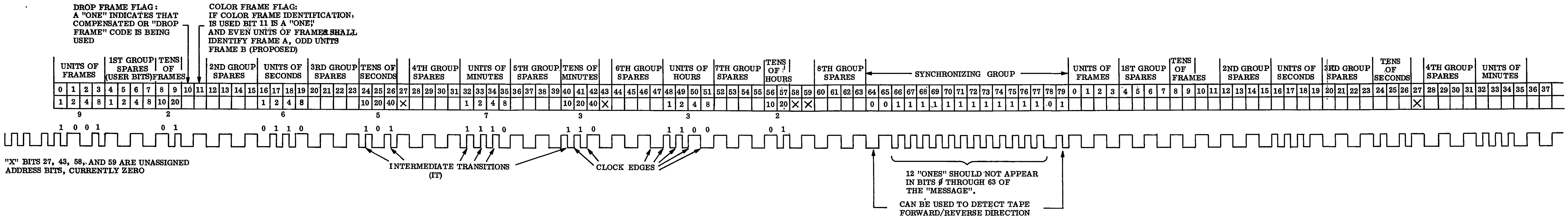
	525		625	
U30-12	900µs	14H	1ms	15.6H
U30-4	14.7ms	230H	17.4ms	272H
U46-6	19ms	299H	23.4ms	362H

VPR-3 A2-1/2
DEMODULATOR
DETECTOR
DROPOUT
SYNC SEPARATORS

AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017 111-19



VPR-3
LINE BY LINE
AUTO CHROMA
525/625
15-11/12



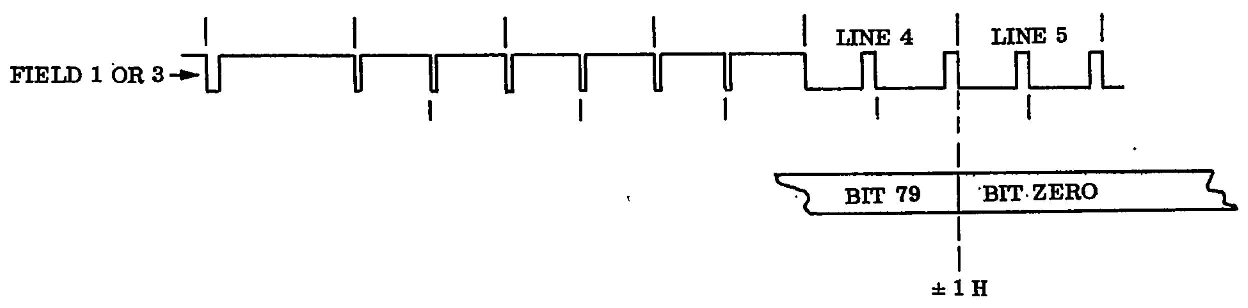
1. THE SMPTE PROPOSED 80 BIT TIME CODE FOR VIDEO TAPE RECORDERS IS RECORDED ON AUDIO TRACK 2 (CUE) ON QUADRAPLEX RECORDERS, AND ON AUDIO 3 ON C FORMAT RECORDERS
2. EIGHTY (80) BINARY BITS - "ONE" OR " ZERO" ARE RECORDED FOR EACH FRAME OF THE TELEVISION SIGNAL. WITH A TAPE SPEED OF 15 ips. THIS REPRESENTS 1/2 INCH (1.27 cm) OF TAPE. AT 9.606 ips (244mm/s) (525 C FORMAT) 0.321" (8.14MM) WILL BE REQUIRED. IN TERMS OF TIME, IT IS 33.4ms ON A 525 STANDARD. EACH "BIT" REPRESENTING A "1" OR A "0" WILL REQUIRE 33.4MS/80 OR 417 µsec ON 525.
   -WHEN THE CODE IS PLAYED BACK IN FAST FORWARD OR REWIND THE PERIOD OF A "BIT" DEPENDS ON TAPE SPEED.
   -ONLY 26 SLOTS ARE REQUIRED FOR THE TIME, WHICH IS RECORDED AS A "1-2-4-8". BINARY CODED DECIMAL ("NATURAL" BCD)
   -EIGHT FOUR BIT GROUPS ARE DESIGNATED "USER BITS." IF NOT USED, ZEROS ARE INSERTED.

3. THE MANCHESTER BI-PHASE MARK ENCODING SYSTEM INCLUDES TWO BASIC ELEMENTS:
   -CLOCK: PERMITS THE DECODER TO BE SYNCHRONIZED TO THE OFF TAPE SIGNAL. IT IS CARRIED BY TRANSITIONS, EITHER POSITIVE OR NEGATIVE GOING, OCCURING EVERY 417 µsec (525) OR 500 µsec (625) WHEN RECORDED.
   -DATA: "ONE" OR "ZERO". A "ONE" IN THE SERIAL STREAM OF INFORMATION IS INDICATED BY A POSITIVE OR NEGATIVE SIGNAL TRANSITION HALFWAY BETWEEN CLOCK TRANSITIONS. IT IS SOMETIMES CALLED AN INTERMEDIATE TRANSITION (IT)

4. THE VERTICAL RATE IN THE 525 COLOR TELEVISION SYSTEM (NTSC OR PAL-M) IS NOT 60Hz (TO WHICH ELECTRIC CLOCKS ARE SYNCHRONIZED), BUT 59.94 Hz. THIS RESULTS IN AN ERROR, OVER A ONE HOUR PERIOD, OF 3.6 SECONDS OR 108 FRAMES.
   —IF THIS TIME DIFERENCE IS IGNORED, THE TIME CODE IS CALLED UNCOMPENSATED AND BIT 10 OF THE CODE IS ALWAYS A ZERO.
   —IN THE COMPENSATED OR DROP FRAME MODE, BIT 10 IS ALWAYS A ONE (BIT 10 IS SOMETIMES CALLED THE "SKIP" BIT). CERTAIN FRAME NUMBERS ARE DELETED, TO ESTABLISH COINCIDENCE BETWEEN TIME CODE AND CLOCK TIME.
   —TWO FRAME NUMBERS -00 AND 01 ARE OMITTED AT THE START OF EACH MINUTE, EXCEPT MINUTES 0, 10, 20, 30, 40, AND 50.

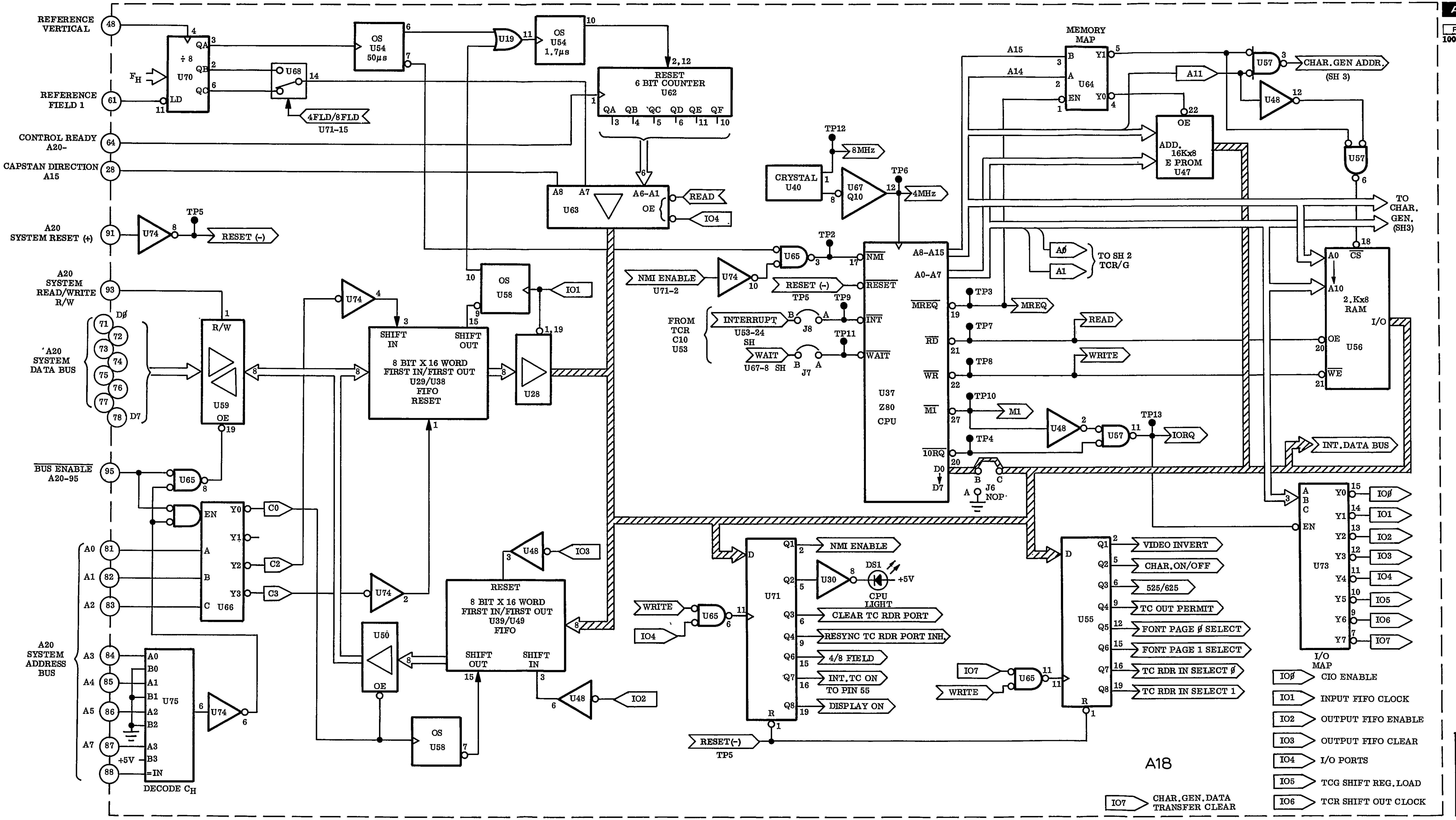
8 MIN	59 SEC	29 FR
9 MIN	00SEC	02 FR
9	00	03FR
9	59	29
10	00	00
10	00	01
10	00	02
10	59	29
11	00	02
11	00	03

5. TIME WITH RESPECT TO THE VIDEO SIGNAL:

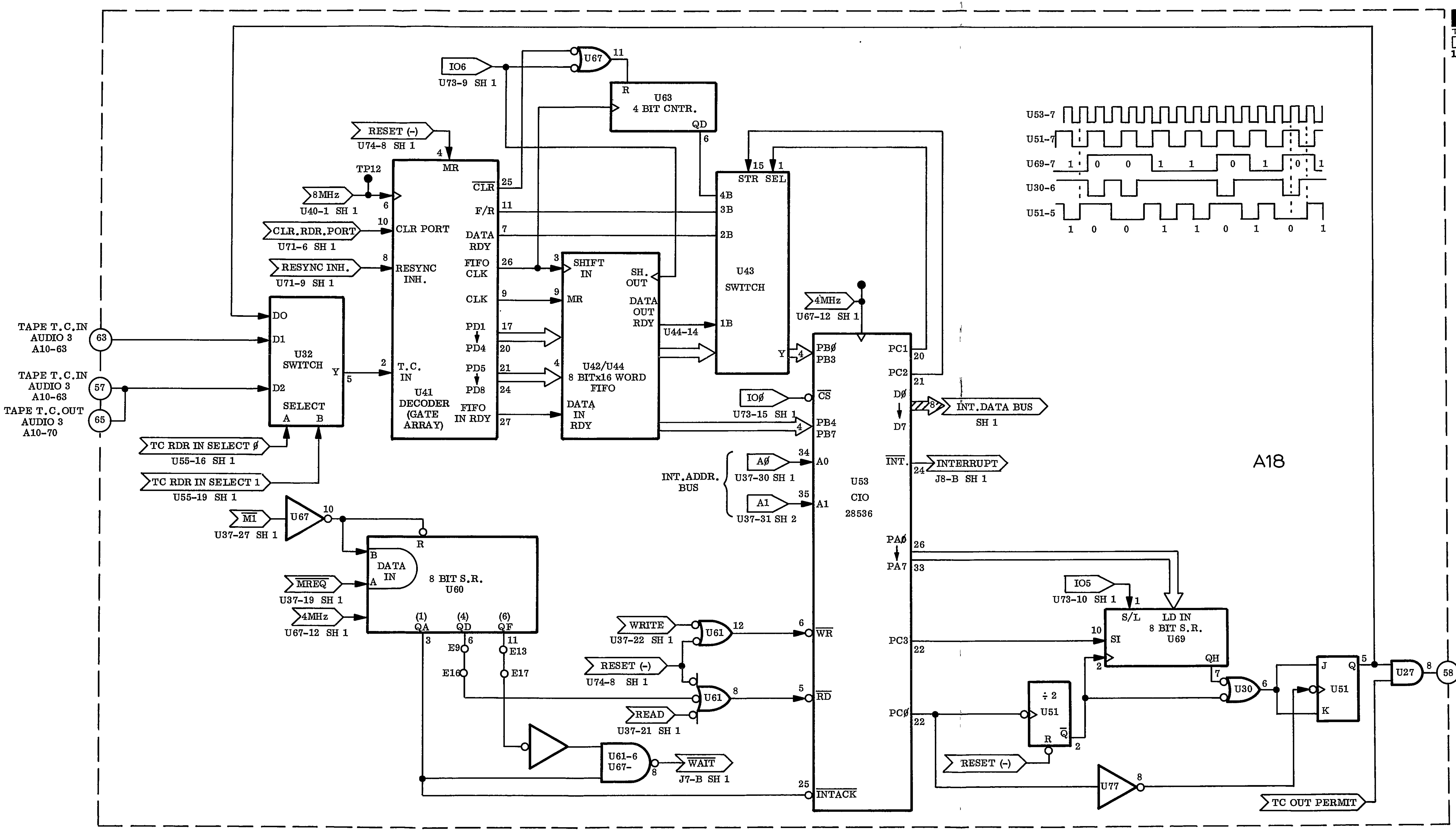


6. a. RISE TIME: 25 ± 5 usec MEASURED BETWEEN 10% AND 90% POINTS.
   b. AMPLITUDE DISTORTION 2 % OF THE PEAK TO PEAK AMPLITUDE.
   c. TIME OF TRANSITIONS ARE MEASURED AT THE HALF AMPLITUDE POINTS. TIME BETWEEN CLOCK TRANSITIONS SHOULD NOT VARY MORE THAN 1% OF THE AVERAGE CLOCK PERIOD OVER ONE FRAME. "ONE" TRANSITIONS SHALL OCCUR HALFWAY BETWEEN TWO CLOCK TRANSITIONS WITHIN 0.5% OF ONE CLOCK PERIOD.

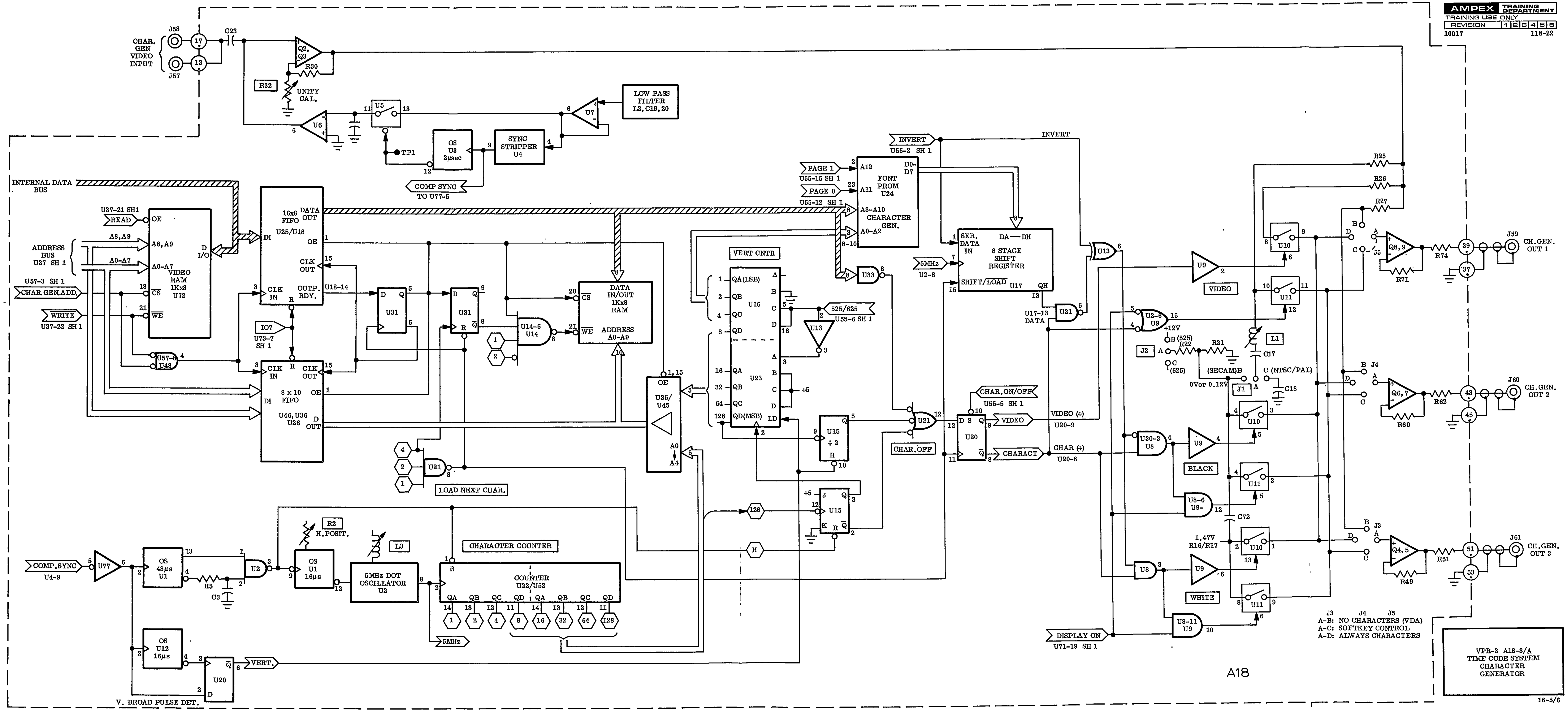
SMPTE TIME CODE
ASA C98.12
525



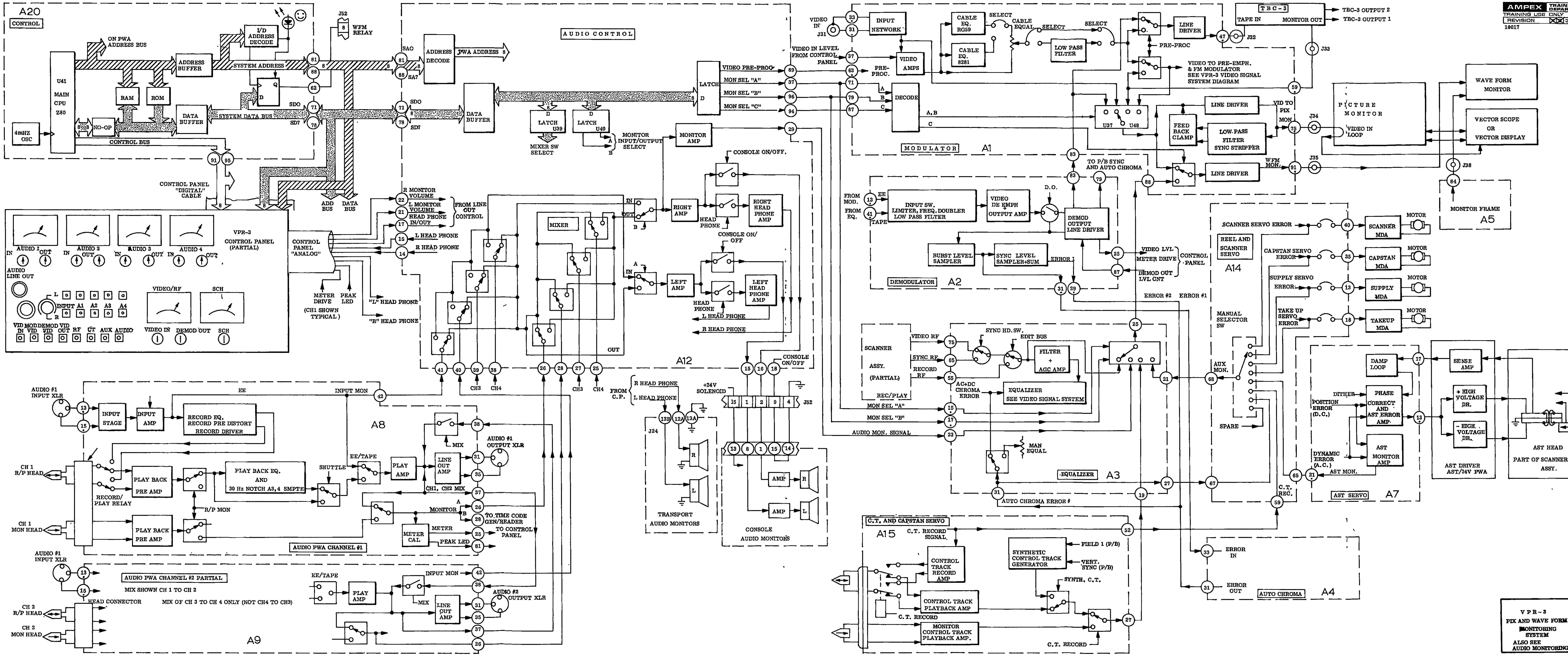
VPR-3 A18-1/
TIME CODE SYSTEM
CONTROL KERNEL
DATA TRANSFER



VPR-3 A18-2/
LONGITUDINAL
TIME CODE READER
GENERATOR



AMPEX TRAINING DEPARTMENT
TRAINING USE ONLY
REVISION 1 2 3 4 5 6
10017
118-22
CHAR. GEN VIDEO INPUT
J58
J57
C23
Q2, Q3
R30
R32
UNITY CAL.
U6
U5
U7
LOW PASS FILTER L2, C19, 20
TP1
OS U3 2μsec
SYNC STRIPPER U4
COMP SYNC TO U77-5
INTERNAL DATA BUS
U37-21 SH1
READ
ADDRESS BUS U37 SH 1
A8, A9
A0-A7
VIDEO RAM 1Kx8 U72
U57-3 SH 1
CHAR.GEN.ADD.
WRITE
U37-22 SH 1
16x8 FIFO U25/U18
DATA OUT
CLK OUT
OUTP. RDY.
CLK IN
U18-14
U31
IO7
U73-7 SH 1
U57-8 U48
8 x 10 FIFO U46, U36 U26
U14-6 U14
DATA IN/OUT 1Kx8 RAM
ADDRESS A0-A9
U35/U45
U21
LOAD NEXT CHAR.
PAGE 1
U55-15 SH 1
PAGE 0
U55-12 SH 1
FONT PROM U24
A3-A10 CHARACTER GEN.
INVERT
U55-2 SH 1
U33
VERT CNTR
QA(LSB)
QD(MSB)
U16
U23
525/625
U55-6 SH 1
U13
U15 ÷ 2
U15
5MHz
U2-8
8 STAGE SHIFT REGISTER U17
SER. DATA IN
SHIFT/LOAD
U17-13 DATA
U21
CHAR.OFF
CHAR.ON/OFF
U55-5 SH 1
U20
VIDEO
CHARACT
VIDEO (+)
U20-9
CHAR (+)
U20-8
U9
U2-6 U9
U30-3 U8
BLACK
U8-6 U9-
U8
WHITE
U8-11 U9
DISPLAY ON
U71-19 SH 1
R25
R26
R27
U10
U11
J5
Q8, 9
R74
R71
J59
CH.GEN. OUT 1
+12V
B (525)
R22
R21
C (625)
(SECAM) B
0V or 0.12V
(NTSC/PAL)
C17
C18
L1
J1
J2
J4
Q6, 7
R62
R60
J60
CH.GEN. OUT 2
C72
1.47V R16/R17
J3
Q4, 5
R51
R49
J61
CH.GEN. OUT 3
J3 J4 J5
A-B: NO CHARACTERS (VDA)
A-C: SOFTKEY CONTROL
A-D: ALWAYS CHARACTERS
COMP.SYNC
U4-9
U77
OS 48μs U1
R5
C3
U2
R2
H. POSIT.
OS U1 16μs
L3
5MHz DOT OSCILLATOR U2
CHARACTER COUNTER
COUNTER U22/U52
5MHz
OS U12 16μs
U20
VERT.
V. BROAD PULSE DET.
A18
VPR-3 A18-3/A TIME CODE SYSTEM CHARACTER GENERATOR
16-5/6

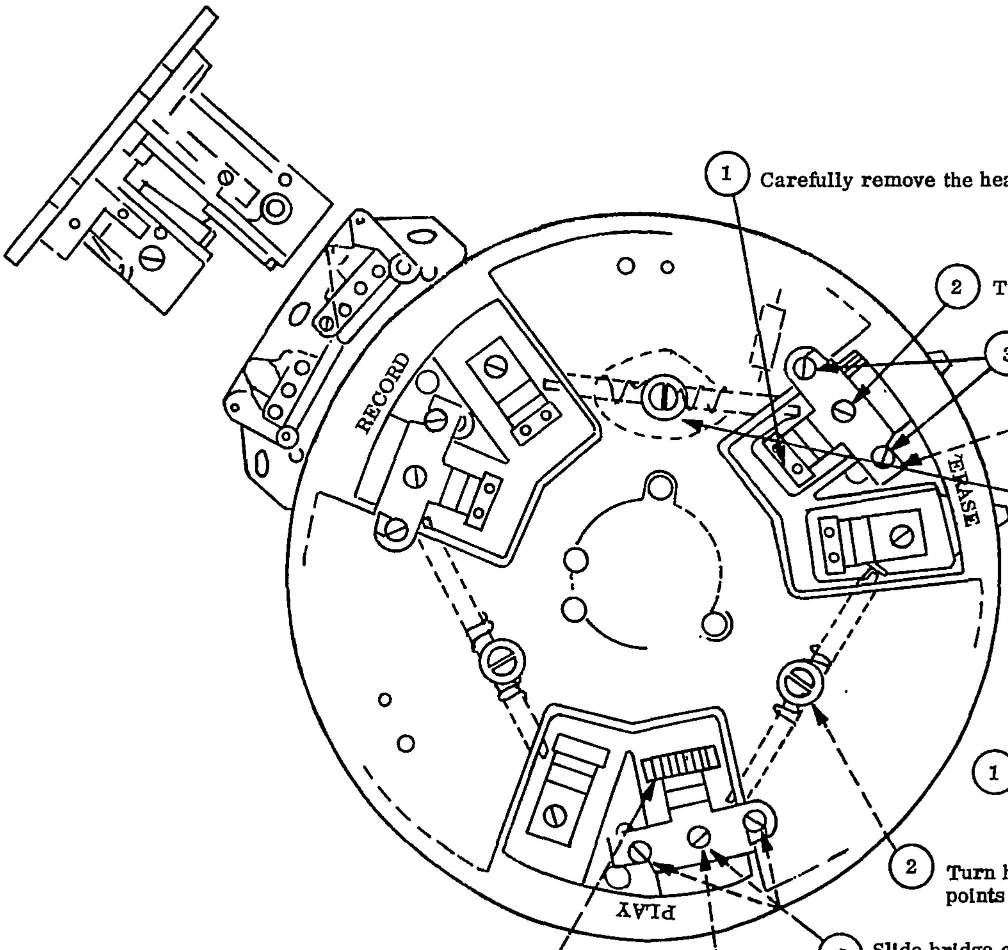


SH 1/2

VPR-3
PIX AND WAVE FORM MONITORING SYSTEM
ALSO SEE AUDIO MONITORING

INDEX

VIDEO HEAD REPLACEMENT



1. Carefully remove the head connector.
2. Turn to stop.
3. Two turns CCW
4. Remove the bridge clamp.
5. Turn head lock CCW until it stops (about 1/4 turn).
6. Slide head back toward center of scanner and up to remove. Clean head mounting area.

REVERSE THE PROCEDURE TO INSTALL THE NEW HEAD

1. Slide the new head in place, carefully sliding the head all the way forward.
2. Turn head lock CW until slot points to center of scanner.
3. Slide bridge clamp under two securing screws and tighten them.
4. Tighten center slot head screw to lock head in place. (Do not over tighten).
5. Carefully insert head connector and replace scnaner cover.

MODULATOR PWA 1
JUMPERS
(X) SCHEMATIC PAGE

J1(3)	**A-B:** normal. **OPEN:** disconnects automatic frequency control (AFC) to the FM modulator for blanking frequency set-up. **A-C; A-D:** used in factory set-up of black and white clip adjustments.
J2(3)	**B-A:** normal. **A-C (open):** disconnects burst pre-emphasis for test.
J3(3)	**A-B:** normal. **A-C (open):** disconnects normal pre-emphasis from modulator video input for test.
J4(1)	**A-B:** normal. Determines the time constant of the modulator input clamp. **A-C** and **A-D** change the time constant.
J5(1)	**A-B:** normal. **A-C (open):** disconnects modulator input video for test.
J6(1)	**A-B:** provides equalization for 8281 cable. **A-C:** equalization for RG-59/U cable.
J7(1)	**A-B:** normal differential video input. **A-C:** used in set-up to adjust input differential amplifier balance. **A-D:** high frequency bypass. Input is still balanced for low frequencies, such as hum. **A-E:** unbalanced input
J8(1)	**A-B:** normal. **A-C:** inserts 6 MHz (525) or 7 MHz (625) low pass filter in video path to modulator. Used where excessive high frequencies are present on the video signal, such as RF interference or those in some computer graphics. **J9** must match position.
J9(1)	**A-B:** normal. **A-C:** see **J8 A-C.**
J10(2)	**A-B:** normal. **A-C:** removes video feedback clamp for monitor video to picture monitor for test purposes.
J11(1)	**A-B:** normal. **A-C:** used in test and in single ended video input mode. Refer also to **J7.**

TEST POINTS
(*)Front of PWA 1

TP1(3)	7.8 kHz Automatic Frequency Control (AFC) sample control signal.
TP2(2)	Composite sync stripped from modulator video.
TP3(3)	Output of AFC video detector.
TP4(3)	Output of "white calibrate" crystal. 525: 10 MHz; 625: 8.9 MHz.
TP5(3)	Video input to modulator.
TP6(3)	Switch modulator RF/crystal RF to AFC detector.
TP7(1)	Low pass filtered video to input clamp sample gate.
TP8(3)	Output of blanking frequency crystal oscillator. 525: 7.9 MHz; 625: 7.68 MHz.
TP9(3)	Modulator output 2 x F RF to record driver. (approximately 14 to 20 MHz)
TP10(1)	Video output of cable equalizer network.
TP11(1)	Input video back porch clamp sample pulse.
TP12(1)	Video output of input differential amplifier.
TP13(2)*	Selected signal to waveform monitor.
TP14(2)	Low pass filtered video input to picture monitor video clamp.
TP15(2)	Picture monitor video clamp sample pulse.
TP16(1)	Input video input to Waveform monitor selector.
TP17(3)	zero volt reference to modulator (see R324).
TP18(2)	Pre-emphasis burst gate. (3 microseconds with R 329)

SWITCHES

S1(2)*	AUTO/MANUAL Video Head Optimize(VHO) control.
S2(2)*	White Calibrate Pulse ON/OFF.

ADJUSTMENTS

C115(1)	Input differential amplifier high frequency compensation.
C139(1)	Input differential amplifier high frequency compensation.
R15(3)	Modulator blanking level frequency. 525: 7.9 MHz; 625: 7.68 MHz.
R26(3)	Factory adjusted white clip.
R29(3)	Peak white deviation calibrate. 525: 10 MHz; 625: 8.9 MHz.
R34(3)	Facory adjusted black clip.
R35(3)	Modulator linearity.
R95(1)	Input unity video gain calibrate.
R96(1)	Video input level control range (0 to +6 dB).
R135(1)	Input differential amplifier offset.
R196(1)	Input video monitor gain calibrate.
R205(1)	Video input differential amplifier balance.
R211(1)*	Cable equalization control.
R323(3)	Automatic frequency control (AFC) calibrate.
R324(3)	Modulator reference voltage calibrate. (zero volts at TP 7)
R325(2)*	Manual video record current control. (See S1)
R326(2)*	Manual sync head record current. (See S1)
R329(2)	Burst gate pre-emphasis pulse width (3 microseconds at TP 18)
T3(1)	6 MHZ low pass filter adjustment (factory).

DEMODULATOR PWA 2
JUMPERS, TEST POINTS & ADJUSTMENTS
(x) SCHEMATIC PAGE

J1(2)	**A-B:** normal. **OPEN:** used in set-up of demodulator low pass filter.
J2(2)	**A-B:** normal. **OPEN:** see J1.
J3(2)	**A-B:** normal. **OPEN:** see J1.
J4	Not used.
J5(2)	Miniature coaxial connector used with J6 in factory set-up of demodulator low pass filter.
J6(2)	**A-B:** normal. **A-C:** connects coaxial connector J5 to the signal path.
J7(2)	**A-B:** normal. **A-C:** used in test with J5 and J6.
J8(2)	**A-B:** normal. **A-C:** test. Disconnects the demodulator video DC restorer clamp error voltage.
J9(2)	**A-B:** normal. Used in factory set-up of demodulator video LPF.
J10(2)	**OPEN:** normal. Used in factory set-up of demodulator video LPF.
J11(2)	**A-B:** normal. Used in factory set-up of demodulator video LPF.
J12(2)	**OPEN:** normal. Used in factory set-up of demodulator video LPF.
J13(2)	**A-B:** normal. Used in factory set-up of demodulator video LPF.
J14(2)	**OPEN:** normal. Used in factory set-up of demodulator video LPF.
J15(2)	**A-B:** normal. **A-C:** bypasses demodulator video de-emphasis network.
J16(1)	**A-B:** Video system PAL or NTSC. **OPEN:** Video system SECAM bus.
J17(1)	**OPEN:** Used with J16.
J18(2)	**A-B:** normal. **A-C:** disconnects dropout pulse from video out gate and clamp gate.
J19( )	
J20(1)	**A-B:** normal. **A-C:** disconnects pulse from diode bridge gating through burst de-emphasis, sync add, etc. to output video driver.

DEMODULATOR PWA 2
TEST POINTS

TP1(3)	RF output of detector frequency doubler.
TP2(2)	Detector RF input to low pass filter.
TP3(3)	Selected EE/Tape RF input to limiter.
TP4(2)	Demodulator video blanking level to dc restorer.
TP5(3)	RF dropout sampling circuit.
TP6(1)	Video input to burst amplitude detector.
TP7(2)	Low pass filtered demodulator video to sync stripper.
TP8(3)	RF signal to dropout detector.
TP9(1)	Regenerated sync and burst de-emphasis signal.
TP10(3)	Dropout.
TP11(3)	Dropout hysteresis feedback.
TP12(1)	Autochroma error.
TP13(1)	Burst sample for autochroma error.
TP14(2)	Sync level voltage to autochroma.
TP15	Not used.
TP16(1)	Demodulator video to dropout clamp/burst de-emphasis.
TP17(3)	"AST RANGE", equivalent to shuttle mode.

DEMODULATOR PWA 2
ADJUSTMENTS

C126(2)	Demodulator video high frequency response.
L1(2)	Factory low pass filter adjustment.
L2(2)	Same as L1.
L3(2)	Same as L1.
L4(2)	Same as L1
L7(2)	Same as L1
L8(2)	Same as L1
L9(1)	Burst detector input peaking coil(?).
R24(3)	Detector balance. Coarse setting for minimum moire at the video output. Precise adjustment requires a spectrum analyzer.
R33(3)	Limiter balance. Coarse setting for minimum moire at the video output. Precise adjustment requires a spectrum analyzer.
R81(1)	Auto chroma calibrate. -2 volt base line at TP 13.(?)
R107(1)	Card edge "Chroma Gain". Card edge switch S1 must be in the variable position. The control panel UNITY mode must also be off.
R113(1)	
R127(1)	Sets amplitude of regenerated sync.
R146(3)	Dropout sensitivity
R160(1)	Demodulator video unity gain.

SYNC EQUALIZER PWA 3
JUMPERS, TEST POINTS & ADJUSTMENTS
(X) Schematic Page

J1(1)	Coaxial connector to allow insertion of test signal into equalizer output filter,
J2(1)	**A-B:** normal. **A-C:** test. Connects J1 into signal path for test.
J3(1)	**A-B:** normal. **A-C:** test. Bypasses differential phase network.
J4(1)	**A-B:** normal. **A-C:** test. Connects coax connector J7 into signal path.
J5(1)	**A-B:** normal (open). **A-C:** test. Bypasses differential gain network.
J6(1)	Miniature coaxial connector for test signal insertion.
J7(1)	Miniature coaxial connector for test signal insertion
J8(1)	**A-B:** normal. **OPEN:** disconnects cosine equalizer reflected path for test of overall frequency response.
J9(1)	**A-B:** normal. **A-C:** connects coaxial connector J6 to signal path for test.
J10(3)	Miniature coaxial connector for test signal insertion.
J11(3)	**A-B:** normal. **A-C:** connects coaxial connector J10 into signal path.
J12(3)	Miniature coaxial connector for test signal insertion.
J15(2)	**A-B:** normal. **A-C:** disconnects equalization control voltage from cosine equalizer during head switch time.
J16(3)	**A-B:** normal. In **A-C** or **B-C** connects coaxial jack J17 into signal path.
J17(3)	Miniature coaxial jack for test signal insertion. Used with J16.
J18(3)	Miniature coaxial connector for signal insertion.
J19(3)	**A-B:** normal. **A-C:** forces switched Tape/EE bus from S2 on PWA 3 to Tape.

TP1(1)	Playback RF signal in to output filter (playback slope filter).
TP2(1)	RF envelope to AST.
TP3(2)	Record head RF (nominal 200 mV).
TP4(2)	Playback RF to AST and dropout detectors.
TP5(2)	Sync head detected RF to meter.
TP6(2)	Sync head RF input (nominal 200 mV).
TP7(3)	Playback RF input to cosine equalizer.
TP8(2)	Playback head (video) RF input (nominal 200 mv).
TP9(1)	RF out of cosine equalizer delay line.
TP10(2)	Detected record head RF to meter.
TP11(3)	Detected playback head RF to meter.
L1(1)	Factory adjustment of P/B slope filter.
L17(2)	Factory adjustment of input 20 MHz low pass filter.
L19(2)	Factory adjustment of input 20 MHz low pass filter.
R1(1)	Differential phase adjustment.
R28(2)	Playback (AST) head RF meter calibrate.
R38(1)	Differential Gain (front of PWA).
R44(3)	Shuttle equalization.
R53(1)	AST envelope amplitude.
R67(3)	Video equalization adjust with S1(3) in the MANUAL position. (front of PWA).
R81(1)	RF level into dropout detector.
R101(2)	Differential gain centering adjust (front of PWA).
R108(1)	Equalization centering.
R126(2)	Record head RF meter calibration.
R129(2)	Record Head RF meter zero.
R181(2)	Sync head meter zero.
R183(2)	Sync head meter calibration.
R284(2)	Playback head meter zero.

AUTO CHROMA PWA 4
JUMPERS, TEST POINTS, SWITCHES

J1	**A-B:** normal. **A-C:** control follows Auto/Manual Switch on Equalizer PWA 3.
R29	
R34	
TP1	Stored error.
TP2	Error input.
TP3	
TP4	
S1	ON/OFF
S2	

COLOR FRAMER DETECTOR PWA 5 (NTSC)
JUMPERS
(X)Schematic Sheet

J1(2)	**A-B:** normal. **A-C:** inverts phas of tape H locked 2xFsc into comparator for test purposes.
J2(2)	**A-B:** normal. **A-C:** test.
J3(1)	**A-B:** normal. **A-C:** connects reference video to tape video path, with **J4** in the **A-C** position. **B-C:** connects demodulator video to the reference video color frame detector, with **J8** in the **A-C** position.
J4(2)	**A-B:** normal. **A-C:** passes reference video through tape video Sc-H detector, with **J3** in the A-B position.
J5(1)	**A-B:** normal. **A-C:** Reference FIELD 1 IDENT ignored after initial lock-up.
J6(1)	**A-B:** normal. **A-C:** used in adjustment of C163 on Chroma Processor U79.
J7(2)	**A-B:** normal. **A-C:** changes meter to fast time constant for test.
J8(2)	**A-B:** normal. **A-C:** used with **J3** in set-up.

TEST POINTS

TP1(2)	910 x Hoscillator output divided by 2.
TP(2)	Burst sample pulse.
TP3(2)	910 H oscillator divided down to subcarrier frequency.
TP4(2)	Playback color field detector.
TP5(2)	Feedback error to lock 910 H oscillator to demodulator horizontal.
TP6(2)	Demodulator video chroma amplifier output.
TP7(2)	Burst Gate.
TP8(2)	Ramp input to demodulator Sc/H meter error detector.
TP9(2)	Sc/H error to control panel meter.

COLOR FRAMER PWA 5 NTSC
TEST POINTS

TP10(2)	Demodulator video sync sliced at 50% point.
TP11(2)	20ns burst/sync phase sample pulse.
TP12(2)	15 kHz ramp to 910 times H oscillator lock circuit.
TP13(2)	Demodulator video half line eliminate pulse.
TP14(2)	Demodulator video.
TP15(1)	Selected reference video Sc/H phase sample pulse.
TP16(1)	Selected reference video (sliced at 50% point).
TP17(1)	Half line eliminate signal.
TP18(1)	Selected reference video to to 50% sync slicer.
TP19(1)	50% voltage to sync separator.
TP20(2)	Demodulator 50% sync slicer voltage.
TP21(1)	Selected reference video composite sync.
TP22(2)	Demodulator video "crude" sync slicer.
TP23(1)	Reference Sc/H phase error.
TP24(1)	Reference phase shifted subcarrier to Sc/H phase detector.
TP25(1)	Regenerated reference subcarrier.
TP26(1)	Sc/H meter calibrate voltage.

ADJUSTMENTS

C163(1)	Reference video subcarrier regenerated subcarrier calibrate.
L1(2)	910 x H oscillator/2 peaking.
L2(2)	Demodulator video chrominance peaker.
L3(2)	910 times H oscillator adjust.
R119(2)	Calibrate meter phase.
R221( )	Monitor display center.
R222( )	Meter linearity.
R223(2)	U18 offset adjust.
R246(1)	Calibrate reference Sc/H.
R263(2)	Sc/H meter range calibrate.

PLAYBACK SYNC PWA 6
JUMPERS & TEST POINTS
(*) Indicates TP on Board Edge

J1	**A-B:** normal. **A-C:** factory test of field counters.
J2	**A-B:** normal. **A-C:** factory test of field counters.
TP1(*)	P/B vertical.
TP2(*)	Demodulator composite sync input.
TP3(*)	Scanner once-around (vertical rate) tachometer signal.
TP4(*)	Reference Vertical.
TP5	Equalizer gate for regenerated sync.
TP6	Detected demodulator (tape) second vertical equalizer pulse.
TP7	Flywheel Tape 2xH (from color framer PWA 5).
TP8	Flywheel Tape H (from color framer PWA 5).
TP9	P/B Frame
TP10	Regenerated tape composite sync.
TP11	Vertical serrations for regenerated composite sync.
TP12	Head Switch (Sync head switching signal to equalizer, autochroma, and time base corrector.

AST SERVO PWA 7
JUMPERS, TEST POINTS & ADJUSTMENTS
(x) Schematic sheet

J1(2)	**NORMAL** OR **FRAME STAGGER** mode. Control of field/frame mode of operation determined in SERVO SET-UP menu
J2(3)	Test set up jumper, to select **OPR A, OPR B, SINE,** or **RAMP.**
J3(3)	**CENT-ENABLE:** normal. **CENT-DISAB:** ?
TP1(3)	Scanner Tach (widened to about 1 ms)
TP2(3)	Detected error (from RF envelope).
TP3(3)	Detected reference dither.
TP4(3)	Detected RF envelope.
TP5(3)	Tone (450 Hz dither signal to AST driver or 750 Hz test tone when J2 in SINE).
TP6(2)	Capstan Tach (2X)
TP7(1*)	Null (used in set-up).
TP8(1*)	Sense strip input.
TP9(2*)	Ramp (DC or tracking error).
TP10(1*)	WF (output to waveform monitor)
TP11(1)	AC correction.
TP12(1)	AST servo correction to driver.
TP13(3)	Signal controlling dither level.
R121(1)	Ramp level
R122(2)	Correction gain.
R143(1)	Null frequency.
R144(1)	Damp gain.
R145(1)	Damp phase.
R187(2)	Reset timing.

(*)Test point on the front of PWA.

SCANNER/REEL SERVO PWA 14 (NTSC/PAL-M)
JUMPERS, TEST POINTS & ADJUSTMENTS
(X) Schematic Sheet)

J1(2)	**B-C:** normal. **B-A:** connects ground to scanner Voltage Controlled Oscillator (VCO) for test.
J2(1)	**OPEN:** disconnects Take-up reel Motor Drive Amplifier (MDA) drive for test.
J3(1)	**OPEN:** disconnects Supply reel MDA drive for test.
J4(1)	**OPEN:** disconnects Capstan MDA drive for test.
J5(2)	**OPEN:** Disconnects Scanner MDA drive for test.
TP1(2)	Scanner position loop error to VCO.
TP2(2)	Scanner position loop vertical ramp.
TP3(2)	Scanner Digital to Analog (D/A) converter reference voltage (+ 5.00 V dc with R95).
TP4(1)	Capstan thermal time constant feedback signal.
TP5(1)	Reel tension/capstan coupling servo error.
TP6(1)	Output of supply tension arm Stop threshold detector.
TP7(1)	Output of take-up tension arm Stop threshold detector.
R6(2)	Scanner position loop centering.
R14(2)	VCO centering.
R46(1)	Capstan error offset.
R95(2)	D/A reference voltage adjust (+ 5 volts at TP3).
R142(1)	Reel/Capstan coupling servo offset.

CAPSTAN SERVO PWA 15 (NTSC/PAL-M)
JUMPERS, TEST POINTS & ADJUSTMENTS
(X) Schematic Sheet

J1(2)	Control Track head connector.
J2	None
J3(3)	**B-A:** normal. **A-C:** test. grounds error input into Voltage Controlled Oscillator (VCO).
TP1(2)	Threshold voltage for control track slicers (tape speed related). Used in adjustment of R108.
TP2(3)	Clock to generate "PLAY 2" command at correct color frame.
TP3(2)	Control Track monitor playback head (confidence head) output. Set to one volt with R92,
TP4(2)	Threshold voltage for control track slicer (tape speed related). Used in adjustment of R107.
TP5(2)	Record/Playback control track head output. (set to 1 volt peak to peak with R91).
TP6(3)	Control track lock window.
TP7(3)	Error voltage to capstan voltage controlled (VCO) oscillator.
TP8(3)	Ramp for Capstan VCO error loop.
TP9(3)	Sample pulse for Capstan VCO error loop.
TP10(2)	Voltage reference for capstan error Digital to Analog converter. Set to 5.00 volts with R30.
R30(2)	A/D converter reference voltage adjust (5 volts at TP10).
R91(2)	Control track playback level (one volt peak to peak at TP3).
R92(2)	Control track monitor head amplitude adjust (one volt peak to peak at TP5).
R107(2)	Playback control track slice point voltage.
R108(2)	Playback control track slice point voltage.
R132(3)	Ramp current source adjust (minimum pulse width at TP 6 in play.
R138(3)	Synthetic control track lock sensor adjustment

REFERENCE GENERATOR PWA 16 (525)
JUMPERS, TEST POINTS & ADJUSTMENTS
(X) Schematic Sheet

J1(3)	**A-B:** enable 2.013886 MHz (128 x H) crystal oscillator to be locked to selected reference sync. **A-C:** enable LC 128 x H oscillator for monochrome (15750) reference, or unstable reference signals.
J2(3)	**A-B:** normal. **OPEN:** disconnects 128 x H oscillator error control voltage.
J3(3)	**A-B:** normal. **OPEN:** disconnects output of 128 x H crystal oscillator.
J4(3)	**A-B:** normal. **OPEN:** disconnects output of 128 x H LC oscillator.
TP1(3)	Error voltage to 128 x H oscillators (- 5 Volts when locked).
C3(3)	Frequency adjustment for 128 times horizontal LC oscillator.
C8(3)	Adjustment for 128 times horizontal crystal oscillator.
L2(3)	Adjustment for 128 times horizontal LC oscillator.

TAPE REMAINING PWA 19
JUMPERS, TEST POINTS & ADJUSTMENTS

J1(2)	Diagnostic probe input
TP1(1)	Selected tape tension error to tape remaining computation logic.
R4(1)	Offset of take up tension error to correct capstan tach counter.
R5(1)	Offset of supply tension error to correct capstan tach counter.

TRANSPORT CONTROL PWA 20
JUMPERS AND TEST POINTS
(X) Schematic Sheet

J1(1)	**A-B:** remote #1 Tx line matching
J2(1)	**A-B:** remote #1 Rx line matching
J3(3)	**A-B:** normal. **OPEN:** opens WAIT line to control CPU U39.
J4(1)	**A-B:** normal. **A-C:** test. Removes V/2 interrogate from serial data address port (S3, S4, S5, & S6).
J5(1)	**A-B:** remote #2 Tx line matching.
J6(1)	**A-B:** remote #2 Rx line matching
J7(1)	**A-B:** normal. **A-C (open):** disconnects INT input to remote CPU U45.
J8(1)	**A-C:** normal. **A-B:** no-op jumper for remote CPU U45.
J9(1)	**B-C:** normal. **A-B:** test. "No-op." connects all serial Tx outputs to all Rx inputs.
J10(3)	**B-C:** normal. **A-B:** no-op jumper for control CPU U39.
J11(3)	**A-B:** normal. **OPEN:** disconnects INT bus from control CPU U39.
TP1(1)	TBC Tx serial data.
TP2(1)	Remote Rx serial data.
TP3(1)	TBC Rx serial data.
TP4(3)	IORQ output of control CPU U39.
TP5(3)	RD (read) output of control CPU U39.
TP6(1)	Remote MREQ, remote CPU U45.
TP7(1)	Remote Tx serial data.
TP8(3)	Microprocessor (CPU) 4 MHz clock.
TP9(1)	V/2
TP10(3)	WAIT to control CPU U39.
TP11(3)	MI output of control CPU U39.
TP12(3)	INT to control CPU U39.
TP13(1)	WAIT test input to serial CPU U45. "Remote WAIT"

TP14(1)	Remote RD from serial data CPU U45.
TP15(3)	RESET to control CPU U39.
TP16(3)	MREQ from control CPU U39. (schematic calls it TP6)
TP17(1)	Remote Clock. 2.4576 clock to U55 DART.
TP18(1)	Remote IORQ. To U45 serial CPU.
TP19(1)	WR (write) from serial (remote) CPU U45.
TP20(3)	WR (write) from control CPU U39.
TP21(3)	Battery voltage.
TP22(3)	NMI to control CPU U39
TP23(1)	Remote MI
TP24(3)	IEO test input to PIO U42.
TP25(1)	IEO test input to PIO U67 (serial machine address)

VPR3JMP.MSS

MODULATOR PWA 1 ADJUSTMENT

1. This procedure covers adjustments on the modulator which do not require special factory test fixtures. These adjustments are not required on a routine maintenance basis, but only if components have been replaced, or there are indications of degraded performance on interchange. Adjustments should not be attempted until the VPR-3 is at a temperature similar to its normal environment.

2. Controls covered in this procedure require the modulator PWA 1 to be on the extender. The front panel controls are covered in the operational procedures for the VPR-3. All jumpers, test points, and adjustments are on MODULATOR PWA 1 unless otherwise noted.

1. With S1 in the LOCAL position, R325 adjusts the video record head current, and R326 the sync record head current. These are normally adjusted for maximum playback RF, as observed on the video confidence playback head.
2. S2 on the front of the PWA turns the WHITE CALIBRATION pulse off, or on.
3. R211 adjusts the cable equalization for optimum video response as observed on the waveform monitor with Modulator video selected on the monitor switcher on the VPR-3 control panel. Jumper J6 on the PWA is used to select RG 59/U or 8281 cable.

CAUTION
TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS
ALWAYS TURN POWER OFF
BEFORE REMOVING OR INSTALLING A PRINTED WIRING ASSEMBLY

3. **Input differential amplifier** noise cancellation and frequency response.

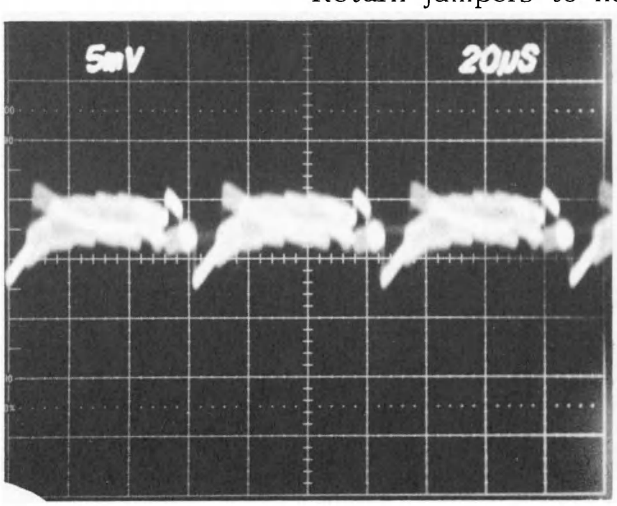
Input signal: 75% color bars.

Test jumpers: **J7 A-C; J11 A-C**

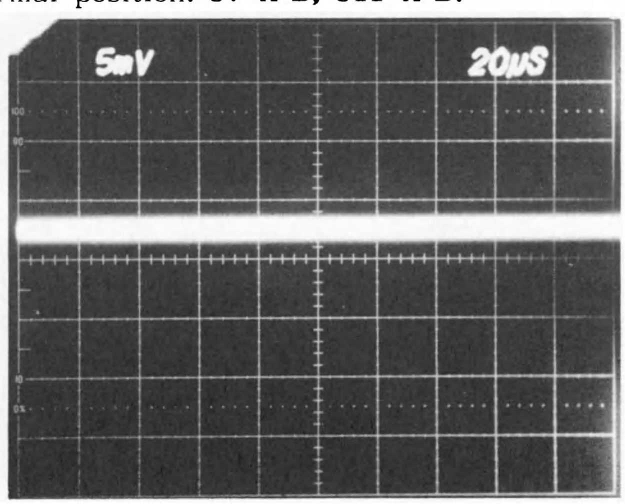
Oscilloscope: External sync: **TP11**; observe **TP 12**

Adjust: **R 205, C139** for minimum signal at **TP 12**

Return jumpers to normal position: **J7 A-B; J11 A-B.**



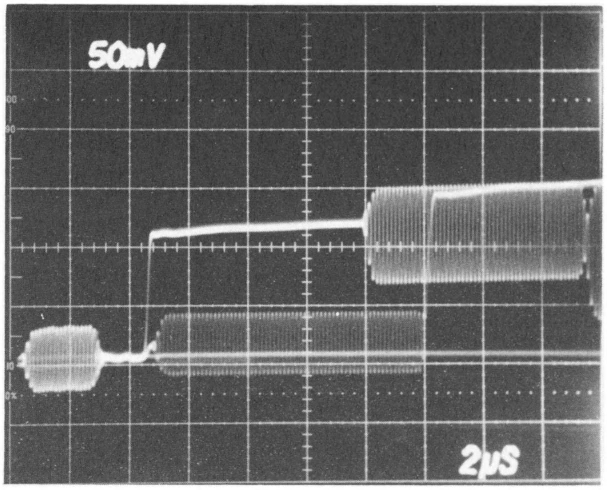
R205/C139 MISADJUSTED



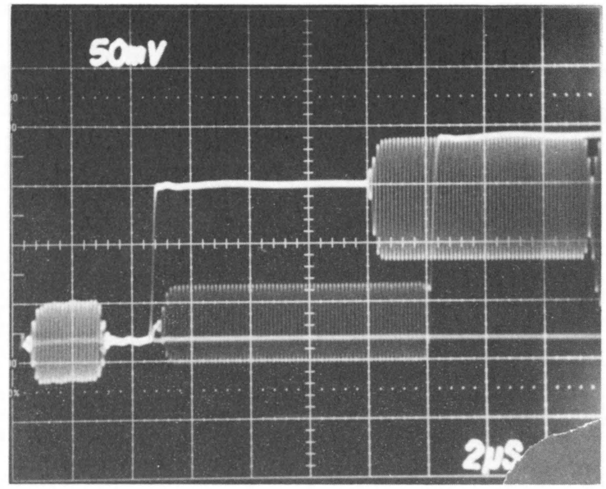
CORRECTLY ADJUSTED

Test signal: Sine squared pulse and bar or split field color bar.

Adjust **C115** for minimum bar tilt at TP 12



C115 MISADJUSTED



CORRECTLY ADJUSTED

4. Variable gain input amplifier dc offset:

   Remove the input video signal.

   Put **J5 A-C**

   Adjust **R135** for zero volts dc.

   Return **J5** to the **A-B** position.

5. Input video monitor gain calibration:

   Check calibration of the waveform monitor.

   Input video signal: One volt (140 IRE) peak to peak signal (luminance value).

   Select VIDEO IN on monitor switcher on the VPR-3 control panel.

   Adjust **R196** for a 1 volt peak to peak (luminance) signal on the VPR-3 waveform monitor.

6. **Modulator linearity** requires a modulated pedestal test signal similar to the TEKTRONIX "Pink Panther" - a 50 % luminance level, and red chroma at three levels of saturation - as video input.

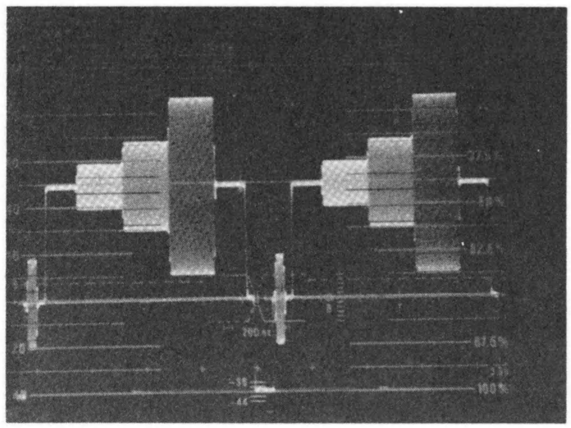
Input signal: modulated pedestal.

Select Demodulator video on the control panel monitor selector, with the scanner off (EE mode).

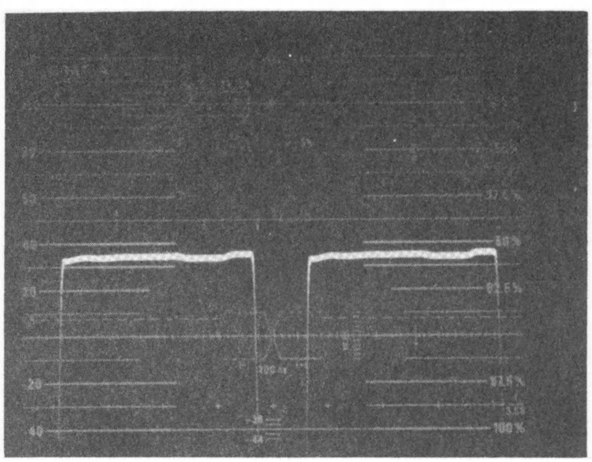
Select the Low Pass (IRE) position on the waveform monitor. Use maximum vertical gain to improve alignment resolution.

Adjust **R35 LINEARITY** for the flattest pedestal.

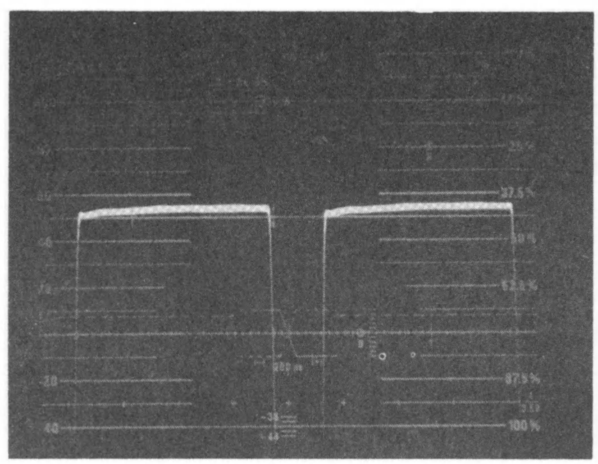
Check modulator frequency and deviation (**R15 and R29**), which interact with **R35**



MODULATED PEDESTAL SIGNAL



R35 MISADJUSTED



CORRECTLY ADJUSTED

7. **Modulator frequency** is checked by comparing the level of blanking on the video input to the modulator with the dc level of the Automatic Frequency Control(AFC) crystal.

Input signal: any test signal which includes a 100 IRE luminance signal (photographs are of split field color bars).

Oscilloscope or digital voltmeter to **TP17**

Adjust **R324** for zero (0) volts dc.

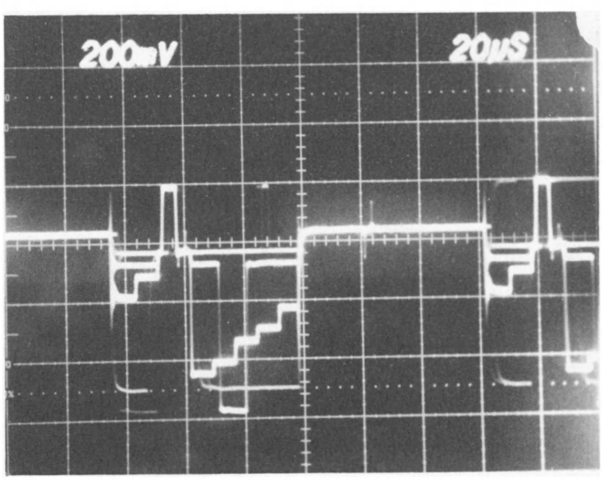
Connect oscilloscope to **TP 3**, triggering from **TP 1** (7.8 kHz).

Test Jumpers: remove **J1**.

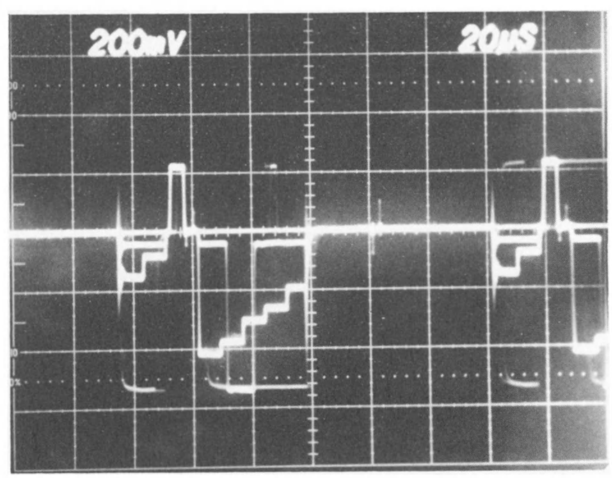
Adjust **R15** so that blanking level on the video signal is the same as the dc level observed on alternate lines which represent the "black" crystal output. (At TP3 the signal alternates at a 7.8 kHz rate between the modulator video signal and the output of the "black" crystal, after FM demodulation.)

Replace **J1** to **A-B** (normal).

If blanking level shifts with respect to level during crystal RF time, adjust **R323** to match the two levels.



R15 MISADJUSTED



CORRECTLY ADJUSTED

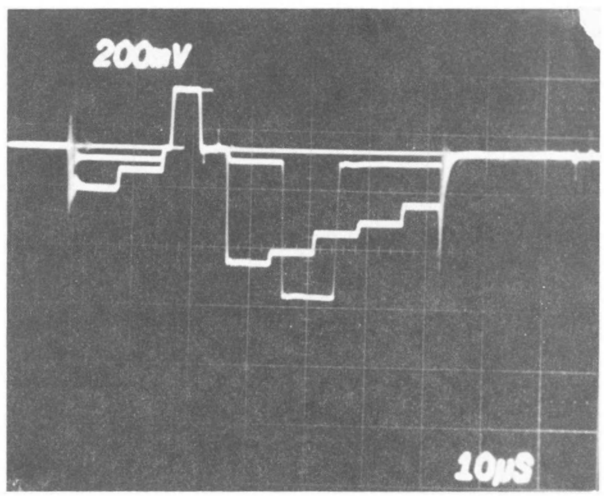
8. Deviation is checked by comparing the output of the level of the "White Cal" pulse (generated by a crystal operating at 10 MHz (525) or 8.9 MHz (625) and the 100 IRE luminance portion of a color bar signal. The white calibrate signal may be observed on the waveform monitor in EE at demodulator output by putting switch S2 on modulator PWA 1 in the ON position (UP). The procedure that follows utilizes test points on Modulator PWA 1.

Video input: any test signal that includes a peak white luminance level component.

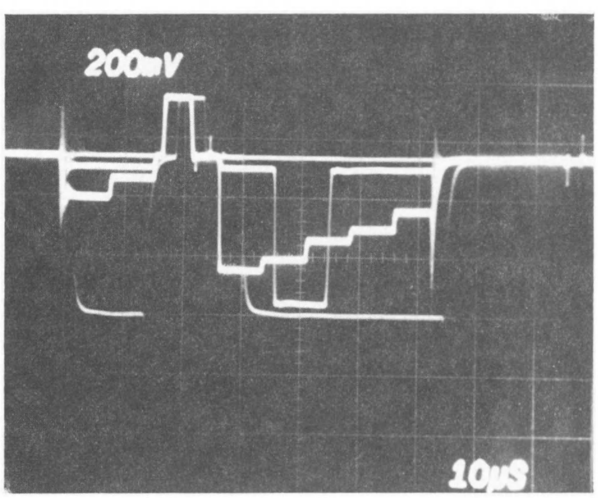
Observe on the oscilloscope **TP 3**, triggering from **TP 1** (7.8 kHz).

With the VPR 3 in EE (STOP, Scanner not READY), turn on the white calibrate pulse (S2 on the MODULATOR PWA 1 UP).

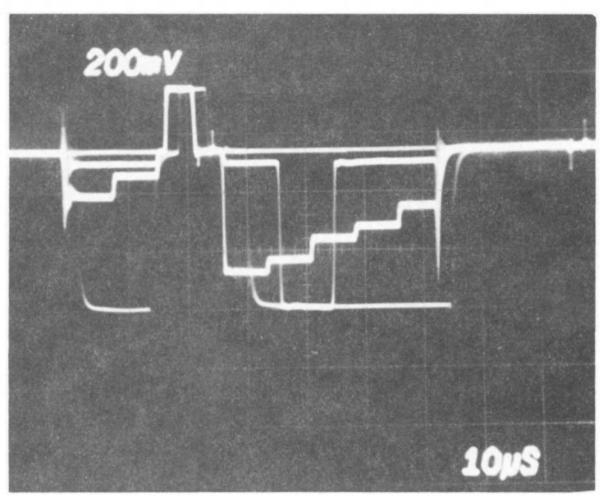
Adjust **R29** for the peak white of the test signal to be equal to the white calibrate pulse.



WHITE CALIBRATE OFF



R29 MISADJUSTED



CORRECTLY ADJUSTED

9. C-Format requires a 6 dB pre-emphasis of burst on NTSC and PAL recordings. **Burst gate** width is adjustable.

Oscilloscope to **TP 18,** triggering on internal.

Adjust **R 329** for a **3 microsecond** pulse width.

10. Peak white clip **R 26** and black clip **R 34** are factory adjusted, (using test jumper **J 1**) to limit modulator deviation.

POWER SUPPLY SYSTEM ALIGNMENT

1. The power supply alignment is not a routine procedure. Power dump and circuit breaker trip adjustment should be done only if there are problems. The low voltage supplies can be checked from the front of the machine and should not be adjusted if within 10 millivolts of the specified voltage.

CAUTION
ALWAYS REMOVE POWER
WHEN REMOVING OR INSTALLING
PRINTED WIRING ASSEMBLIES (PWA)
AND WAIT AT LEAST 30 SECONDS
AFTER TURNING OFF POWER
BEFORE REMOVING A PWA
IN THE POWER CHASSIS ASSEMBLY.

SAFETY GLASSES SHOULD BE WORN
WHEN SERVICING THE POWER CHASSIS ASSEMBLY.

2. **Power dump threshhold detector** adjustment **R16** and **circuit breaker trip threshold detect** adjustment **R22** are located on the Power chassis mother board.

NOTE **There is also a circuit breaker trip command from the control logic which can be disabled by removing J12 on Control PWA 20.**

STEP 1 With power to the VPR-3 OFF, remove the Regulator, 24V Regulator/AST Driver, Reel MDA, and Capstan/Scanner MDA printed wiring assemblies. All test points referenced are on the Power Chassis mother board. Use a digital voltmeter for measurements.

NOTE STEPS 2 through 5 are based on the equation

(TP 4 Volts)/(95) = (TP3 volts)/(R1 Volts).

STEP 2 Measure the + 70 volt supply across **R1**, and note.

STEP 3 Measure the voltage at **TP4** and note.

STEP 4 Multiply the voltage measured across **R1** by the voltage at **TP4**, divide the result by **95** [(R1 x TP4)/95) = TP3], and note.

STEP 5 Measure the voltage at **TP3**. If necessary, adjust **R22** for the voltage calculated in STEP 4.

NOTE The following measurements were made in a typical VPR-3:

R 1: 83.85 V

TP 3: 4.82 V

TP 4: 5.47 V.

CALC: (83.85 x 5.47)/95 = 4.83 (TP 3)

NOTE — STEPS 6 through 8 are based on the equation

(TP 1 volts)/(R1 volts) = (TP 2 volts)/(90).

STEP 6 — Measure the voltage at **TP 2** and note.

STEP 7 — Multiply the voltage measured across **R1** by the voltage at **TP2**, divide the result by **90** [(R1 x TP2)/(90) = TP1], and note.

STEP 8 — Measure the voltage at **TP1.** If necessary, adjust **R16** for the value calculated in STEP 7.

NOTE — Measurements in a typical VPR-3:

R 1: 83.85 V

TP 1: 5.84 V

TP 2: 6.28 V.

CALC: (83.85 x 6.28)/90 = 5.85 (TP 1)

Remove power. Replace the printed wiring assemblies in their proper slots. Restore power to the VPR-3 if no further tests are required.

3. DC to DC converter adjustment **R29.**

With power to the VPR-3 OFF, place the Regulator PWA on an extender.

Voltmeter to pin 19/20. Apply power. If not **6.1 volt ± 50 mV,** adjust **R29.**

4. AST DRIVER/24V PWA reference voltage.

DVM — TP1

ADJUST — **R33** for **+ 5** Volts.

5. Low voltage supplies **(+ 5, ± 12V)** are checked at the front card cage, using the extender.

+ 5 Vdc	Place extender into slot 13 (spare), and connect voltmeter to pin 99/100. Turn on power. Read +5 ± 10 mV.
	If necessary, adjust **R49** on REGULATOR PWA for +5 ± 2 mV.
+ 12 Vdc	Place extender into slot 4 (AUTOCHROMA). Do not install PWA. Connect voltmeter to pin 1/2. Turn on power. Read + 12 ± 10 mV.
	If necessary, adjust **R89** on REGULATOR PWA for +12 ± 2 mV.
- 12 Vdc	Voltmeter to slot 4 pin 5/6. Read - 12 ± 10 mV.
	If necessary, adjust **R111** on REGULATOR PWA for -12 ± 2 mV.
	Plug the extender into slot 14 (REEL & SCANNER SERVO). Do not install PWA. Check following voltages. There are no adjustments.
+ 13 Vdc	Pin 1/2 = + 12.8 to + 15 Vdc.
-13 Vdc	Pin 5/6 = - 12.8 to - 15 Vdc.
SERVO +5	Pin 99/100 = + 5 ± 100 mV.

6. When the TAPE REMAINING PWA 19 Analog to Digital converter is installed, the reference voltage is set by **R95**. Measure the voltage at PWA 19 U 32 pin 12, using a digital voltmeter. It should be **2.45 Volts.** If mis-set, it will cause erroneous fault conditions on the control panel home menu fault display.

7. If no TAPE REMAINING PWA is installed, the A/D reference voltage adjust is on REFERENCE PWA 16. The voltage is set by **R151**. Measure the voltage at PWA 16 U60 pin 12, using a digital voltmeter. It should be **2.45** Volts.

REEL SERVO SYSTEM ADJUSTMENTS

1. With power off, place the SCANNER/REEL SERVO PWA 14 on the extender. Turn VPR-3 power on.

STEP 1 — Connect scope to **PWA 14 Pin 31.** Move **Take-up** tension arm from the left to the right mechanical stops. The voltage should swing from **+ 5 ± .1 V to – 5 ± .1 V.**

STEP 2 — Move the scope to **PWA 14 pin 32,** and move the **Supply** tension arm from one mechanical stop to the other. The voltage swing should be from **+ 5 V ± 0.1 to –5 V ± 0.1.**

- If these parameters are not met, adjustment of mechanical stops or tension arm sensors will be necessary.
- The end stops on both tension arms are eccentric cams which provide a vernier trim to equalize the two voltages.

STEP 3 — If adjustment is required, remove the transport cover trim.

STEP 4 — If any of the above voltages are incorrect, first, loosen the mechanical stop, and try to adjust the eccentric cam to bring the voltage in the correct range.

STEP 5 — If the mechanical stops do not have enough range, place both of them associated with the arm out of adjustment to the mechanical center.

- There are two adjustable resistors, **R1** and **R5,** located on the back of each of the tension arm assemblies.
- Adjust **R5** for a range of ± 5 Volts, and **R1** offset control for the correct voltage at each of the mechanical stops.
- Since the supply arm assembly is located behind the air package, it will be necessary to remove the tension arm assembly, make a trial adjustment, replace it, and verify that the trim was correct.

2. With power off, place the TAPE REMAINING PWA 19 on the extender, and turn VPR 3 power on.

STEP 1 — Move the scope to **PWA 19 pin 28.** Manually turn the capstan counterclockwise and verify that **pin 28** is "low".

STEP 2 — Move scope to **PWA 19 TP1.** Move the **Take up** tension arm from one mechanical stop to the other. If necessary, adjust **PWA 19 R4** to give a **6 volt peak to peak swing.**

STEP 3 — Return the scope to **PWA 19 pin 28** and turn the capstan clockwise, observing that pin 28 voltage is "high".

STEP 4 — With the scope on **PWA 19 TP 1,** swing the **Supply** tension arm from one mechanical stop to the other. If necessary, adjust **R5** for a **6.4 volt peak to peak swing.**

3. On the **REEL MDA, R89 (supply)** and **R10 (take-up)** differential balance adjustments are set using a factory fixture. To adjust the zero balance controls:

CAUTION
ALWAYS REMOVE POWER
WHEN REMOVING OR INSTALLING
PRINTED WIRING ASSEMBLIES (PWA)
AND WAIT AT LEAST 30 SECONDS
AFTER TURNING OFF POWER
BEFORE REMOVING A PWA
IN THE POWER CHASSIS ASSEMBLY.

SAFETY GLASSES SHOULD BE WORN
WHEN SERVICING THE POWER CHASSIS ASSEMBLY.

	Remove tape from the transport. Remove jumpers **J3** and **J2** on Reel and Scanner PWA 14, and return PWA 14 to the card cage.
	Place Reel MDA PWA 3 on the extender.
Scope	Trigger: Reel MDA PWA 3 **pin 59**
	Channel 1: Reel MDA PWA 3 **TP 1**
	Channel 2: Reel MDA PWA 3 **TP 4**
Transport	Place a spacer between the two tension arms and their stops (an IC clip will work). Block the tape in transport sensor mounted on the video erase assembly. Turn on power to the VPR-3 and enter PLAY mode
Adjust	Ground pin **pin 43 or pin 44** of Reel MDA PWA 3 and adjust **R71** until there are no pulses at TP 1 or TP 4.
	Remove the ground from pin 43/44.
Scope	Trigger: Reel MDA PWA 3 **pin 59**
	Channel 1: Reel MDA PWA 3 **TP 9**
	Channel 2: Reel MDA PWA 3 **TP 11**
Adjust	Ground pin **47 or 48** and adjust **R94** until there are no pulses at TP 9 or TP 11.
	Turn off power to the VPR-3. Replace Reel MDA PWA 3 into its slot.
	On Reel and Scanner PWA 14, replace **J2** and **J3**. Remove Tape in Transport sensor block, and the spacers from the tension arms.

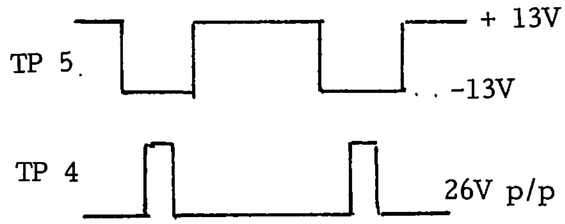
4. Certain faults in the REEL MDA may cause the FET drivers to fail. The following procedure is useful in troubleshooting. It is applicable to all of the MDA's by substituting the correct test points, etc.

STEP 1 Remove the P-channel FET's Q20, Q21, Q49. and Q50.

STEP 2 Install test jumpers **J1** and **J2**.

STEP 3 Connect the oscilloscope to **TP 4** and **TP 5**, triggering from PWA pin 59.

STEP 4 Enable the Reel servos by holding the tension arms in the center of their range. The waveforms should be as shown below. Moving the tension arm should change the width of the pulse at TP 4. The voltage at TP 5 should swing equally positive and negative.



STEP 5 Repeat steps 3 and 4 for the take-up arm, using TP 10 and TP 11.

STEP 6 Remove test jumpers J1 and J2 and replace the P-Channel FET's.

CONTROL TRACK AND CAPSTAN SERVO ALIGNMENT

1. Control track level adjustments. Place Control Track and Capstan servo PWA 15 on the extender. Play a pre-recorded tape for the following adjustments.

- Control Track Monitor Level **R92**

Scope	Trigger **PWA 15 pin 45 (V/2)**
	Channel 1: **TP 3**
Adjust	**R92** for 1 ± 0.1 volt peak to peak

- Control track playback level.

Scope	**TP 5**
Adjust	**R 91** for 1 ± 0.1 volt peak to peak.

- Slice level (525 standards only)

Scope	**15 TP 4**
Adjust	**15R107** for - 0.025 Vdc in STOP/READY OFF mode.
Scope	Move scope to **15 TP 1**
Adjust	**15R108** for + 0.025 Vdc in STOP/READY mode.

- Control track record level (625 standards only)

Scope	**TP3** monitor head ccontrol track
VPR	Record mode.
Adjust	**R 174** for 1 volt peak to peak.

2. VCO adjustment.

Voltmeter	**15 TP10**
Adjust	**15R30** for + 5.0 Vdc.
Jumpers	**15J3 A-C**
Scope	Channel 1 to **15TP 8** (trigger).
	Channel 2 to **15TP 9**
Adjust	In EE mode, **C81** for minimum drift of TP 9 with respect to TP 8.
Jumpers	Return **15J3** to its normal **A-B** position.
Mode	STOP/READY off.
Scope	**15TP 7**
Adjust	C81 for zero volts, ± 0.1 volt.
Scope	Trigger: **15 pin 45**
	Channel 1: **15 TP 6**
Mode	Playback of a pre-recorded tape
Adjust	**15 R132** for minimum pulse width (normally less than 20 microseconds).
Scope	Move channel 2 to **15 TP 7**
Mode	Playback a pre-recorded tape.
Adjust	**15C81** for 0 volts ±0.1 V.

3. Synthetic Control track lock detect.

Scope	Trigger: PWA 15 **pin 39**, Delayed V.
	Channel 1: **U77-3** (TP 9)
	Channel 2: **U77-5**
VPR Mode	Select Synthetic Control Track on Servo SET-UP More menu and play back a pre-recorded tape
Adjust	**15R138** so that the positive pulse at **U77-3** is in the center of the pulse at **U77-5.**
	Remove PWA 15 from the extender and replace the PWA in the card slot.

4. Capstan error offset is on REEL AND SCANNER PWA 14. Place PWA 14 on the extender.

Mode	Stop. not READY.
Capstan stall	Connect **14 Pin 38** to +5 v dc
Scope	**14U48-2**
Adjust	**14 R46** for 0 Vdc.
	Remove jumper to +5 V from 14 Pin 38
Scope	Move scope to **14TP 5**
Mode	Normal PLAY
Adjust	After lock-up, **14R142** for zero volts.

5. Capstan MDA alignment requires that the CAPSTAN/SCANNER MDA be on the Extender. Capstan differential balance **R81** requires a factory fixture to adjust. Zero balance is set as follows:

CAUTION
ALWAYS REMOVE POWER
WHEN REMOVING OR INSTALLING
PRINTED WIRING ASSEMBLIES (PWA) AND
WAIT AT LEAST 30 SECONDS
AFTER TURNING OFF POWER
BEFORE REMOVING OR REPLACING
A PWA IN THE POWER CHASSIS ASSEMBLY.

SAFETY GLASSES SHOULD BE WORN
WHEN SERVICING THE POWER CHASSIS ASSEMBLIES

Scope	Trigger from Sync, **PWA pin 59.**
	Channel 1: **TP 4**
	Channel 2: **TP 1**
Mode	STOP, NOT READY.
Adjust	**R 64** until no pulses are present on either channel.
Note	Check first that pin 43 is at zero volts.
	Turn off power and replace SCANNER/CAPSTAN MDA.

10017 REV 1 V-0286X

SCANNER SERVO ADJUSTMENTS

1. With power removed from the VPR-3, place PWA 14 REEL AND SCANNER SERVO, on the extender.

2. **Digital to analog coverter reference voltage:**

Digital voltmeter	14TP **3**
Adjust	14 **R 95** for **+ 5 volts, ± 10 mV.**

3. The **Voltage controlled oscillator (VCO) adjustment** is necessary only if a component in the area of VCO 14U19 has been replaced, or serious misadjustment has accidentally occurred:

Scope	14**Pin 53** (Scope Trigger): scanner lock reference.
	14**Pin 50,** Scanner vertical tachometer.
Jumper	14J1 **A-B**
VPR MODE	Ready.
Coarse Adjust	14**R14** until **pin 50** is the same frequency as **pin 53.**
Jumper	Restore **J1** to its normal **B-C** position.
Scope	**14 TP 1**
Fine Adjust	**14 R 14** for zero volts.
Adjust	**14 R 6** to put the falling edge of the signal on **pin 50** in the center of the pulse on **pin 53.**

4. To adjust **Scanner MDA Balance,** place the Scanner/Capstan MDA on the extender. Do not adjust differential balance **R115,** which is set using a special factory test fixture.

CAUTION
ALWAYS REMOVE POWER WHEN REMOVING OR INSTALLING PRINTED WIRING ASSEMBLIES (PWA) AND WAIT AT LEAST 30 SECONDS AFTER TURNING OFF POWER BEFORE REMOVING ANY PWA IN THE POWER CHASSIS ASSEMBLY.

SAFETY GLASSES SHOULD BE WORN WHEN SERVICING THE POWER CHASSIS ASSEMBLY

VPR Mode	STOP, NOT READY.
Jumper	Remove 14 **J5** and the Scanner Reel Servo PWA.
Scope	Trigger at SCANNER/MDA PWA **pin 59,** "Sync".
	Scanner MDA **Tp 8**
	Scanner MDA **Tp 9**
Ground	Connect Scanner MDA **Pin 47 or 48** to ground.
Adjust	**R121** Zero balance so that there are no pulses present at either test point.
	Turn off power, replace **14 J5,** and return all boards to the card cages.

VPR-3 REMOTE CONNECTOR PIN ASSIGNMENTS

1. Parallel Remote J54.

PIN	DESCRIPTION and SOURCE/DESTINATION.
1	
2	Record Lamp. A20-23
3	Ready Lamp. A20-25
4	External Command, Video. A20-60
5	Sto Switch. A20-29
6	Remote Analog voltage. A16/A19-31
7	Remote Lamp. A20-34
8	External command, Audio. A20-51
9	Variable Play Switch. A20-54
10	MVC Send. A20-40
11	MVC Receive. A20-45
12	Variable Play Lamp. A20-53
13	Ground.
14	Record Switch. A20-4
15	Ready Switch. A20-26
16	Stop Lamp. A20-27
17	Play Lamp. A20-30
18	Shuttle Lamp. A20-32
19	Play Switch. A20-31
20	Shuttle Switch. A20-33
21	System Fault Lamp. A20-37
22	MVC Cue. A20-39
23	Remote Edit. PWA 20-79
24	Edit Animate Done. PWA 20-80
25	+ 12 Volt Lamp.

2. **Serial 1 Remote, J55.**

PIN	DESCRIPTION and SOURCE/DESTINATION.
1	GROUND
2	Transmit A. A20-49
3	Receive B. A20-47
7	Transmit B. A20-50
8	Receive A. A20-48
9	GROUND.

3. **Serial 2 Remote, J56.**

PIN	DESCRIPTION and SOURCE/DESTINATION
1	GROUND
2	Transmit A. A20-57
3	Receive B. A20-55
7	Transmit B. A20-58
8	Receive A. A20-56
9	GROUND.

INTERCONNECT CABLE

VPR-3 (J36) TBC-3 (J11)

TBC J11	VPR J36	SIGNAL	VPR-3 MODULE	VPR-3 PIN	TBC-3 MODULE	TBC-3 PIN
A	20	Stepback 1	P/B Sync Proc.	XA6-14	Memory Control	XA6-69
C	2	Ground	Mother Board		Mother Board Ground	
B	21	Stepback 2	P/B Sync Proc.	XA6-13	Memory Control	XA6-87
D	3	Ground	Mother Board		Mother Board Bround	
F	23	Sync Retard	P/B Sync	XA6-15	Sync Generator	XA15-63/64
LL	24	Pre-Process	Audio Control	XA12-89		
K	26	Playback Vertical	P/B Sync Proc.	XA6-22	Tape VCO	XA5-33
M	8	Ground	Mother Board		Mother Board Ground	
R	25	Vertical Dropout/	P/B Sync Proc.	XA6-19	Tape VCO	XA5-69/70
		Head Switch			Dropout Comp.	XA7-53/54
					Velocity Comp.	XA13-62
T	7	Ground	Mother Board Ground		Mother Board Ground	
CC	15	Unity	Audio Control	XA12-51	Control Panel	P14-12
V	26	TTL Dropout	P/B Sync	XA6-26	Tape VCO	XA5-76
X	11	Shield Ground	Mother Board Ground		Mother Board Ground	
S	9	Zero Offset		XA6-24	Video Input	XA2-40
					Sync Generator	XA15-28
P	27	Variable	P/B Sync	XA6-21	Tape VCO	XA5-36
		(Slow Motion)			Tape H Comparator	XA4-35
					Memory Control	XA6-39
					Sync Generator	XA15-22
H	14	Ground	Mother Board		Mother Board Ground	
E	32	Step Forward 2	P/B Sync	XA6-30	Memory Control	XA6-81
U	28	2 H Gate	P/B Sync Proc.	XA6-23	Video Input	XA2-87
W	10	Ground	Mother Board		Mother Board Ground	
Y		Reverse/Forward			Tape VCO	XA5-20
		(Down/Up)				
L	6	Fast Shuttle	AST	XA7-25126	Tape VCO	XA5-74
N	5	Video Mute	Control	XA20-22	Video Input	XA2-63
JJ	31	Step Forward 1	P/B Sync Proc.	XA6-27	Memory Control	XA6-88
NN	13	Ground	Mother Board		Mother Board Ground	
EE	30	Sync Head Process	P/B Sync Proc.	XA6-25	Tape VCO	XA5-73
Z	33	Input SC-H	Reference	XA16-62	Tape H Comp.	XA4-34

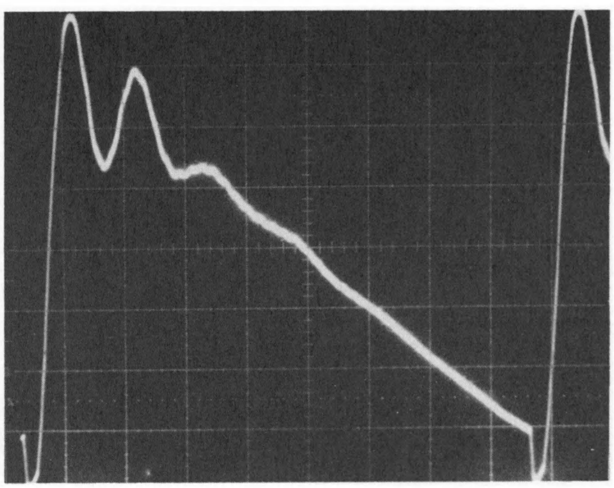
VPR-3 AST HEAD ALIGNMENT

1. This procedure should be performed whenever a new AST head is installed in the scanner.

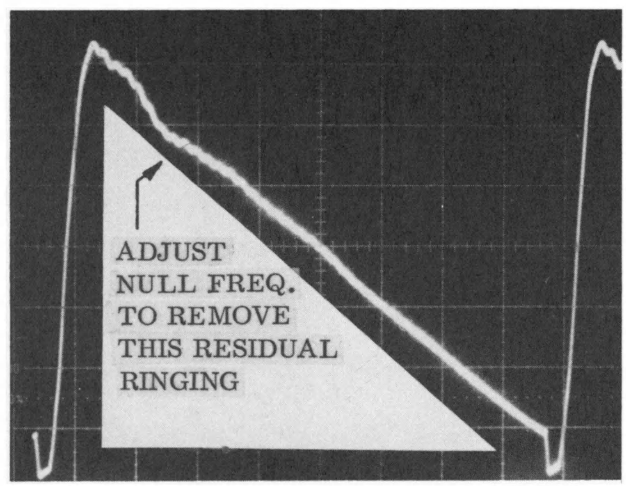
2. Initialize after installation of a new head:
   1. AST PWA 7 on the extender.
   2. Trigger the oscilloscope from PWA **6 TP3**, Scanner Tach.
   3. On AST PWA 7, set RAMP LEVEL **7R121** midrange, and DAMP PHASE **7R145**, DAMP GAIN **7R144** and CORRECTION GAIN **7R122** full counterclockwise.
   4. AST ON (switch on PWA 7), and FIELD mode (SERVO SET-UP MENU).
   5. VPR-3 in READY mode.

3. Place Test Jumper **7J2** in SINE position
   - Scope to **7TP7**, "Null".
   - Adjust **7R143** for a null of the test tone.

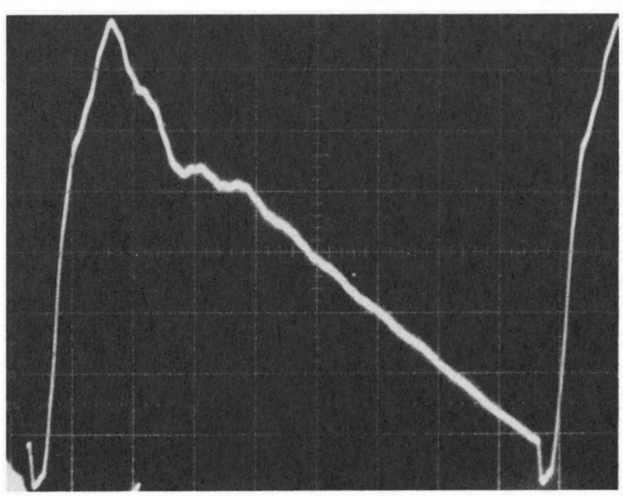
4. Change test Jumper **7J2** to RAMP position.
   - Move the oscilloscope to **7TP8**, "Sense".
   - Adjust **7R144** for the flattest slope on the ramp. See figures 1a, b, and c.



1a. DAMP GAIN TOO LOW

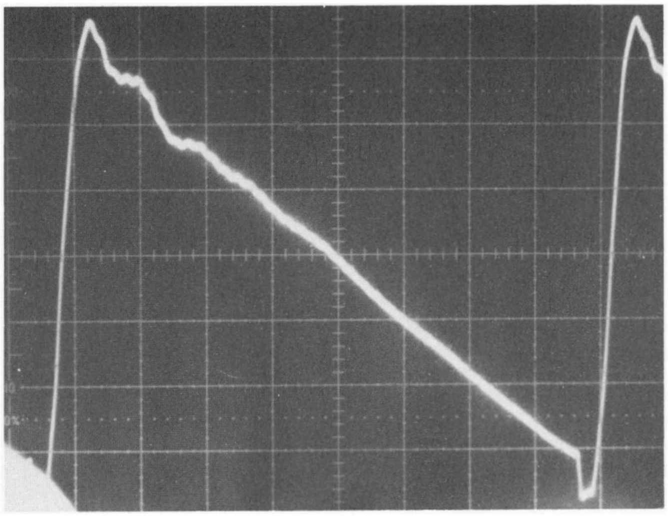


1b. DAMP GAIN CORRECT

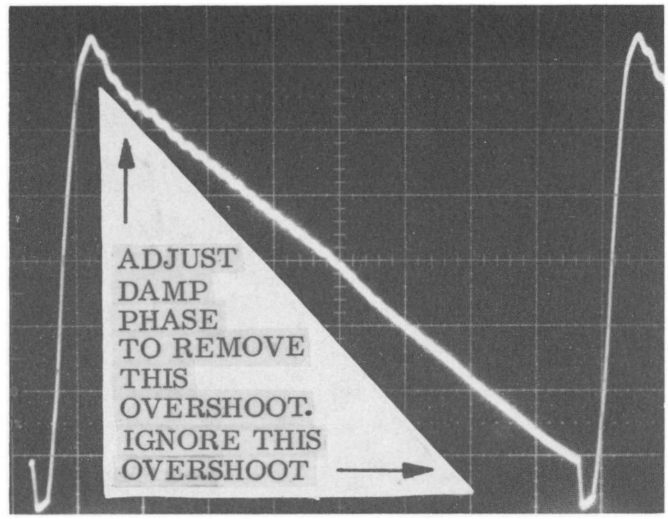


1c. DAMP GAIN TOO HIGH

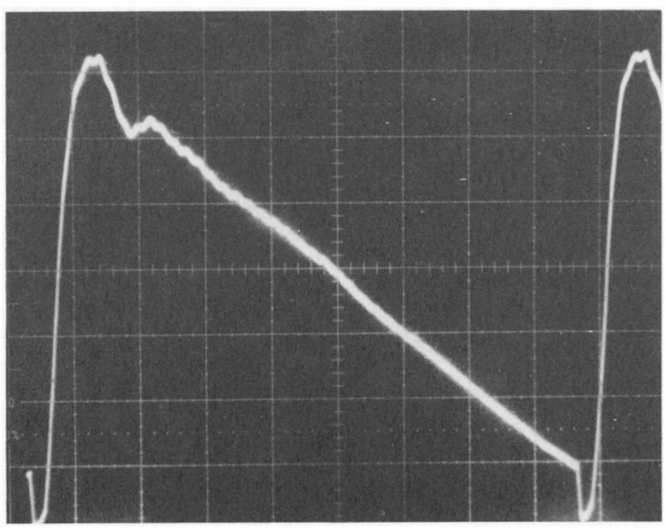
5.Adjust **7R143** NULL FREQUENCY for minimal ringing and overshoot. Refer to Figures 2a. b, and c.



2a. NULL FREQ. TOO LOW



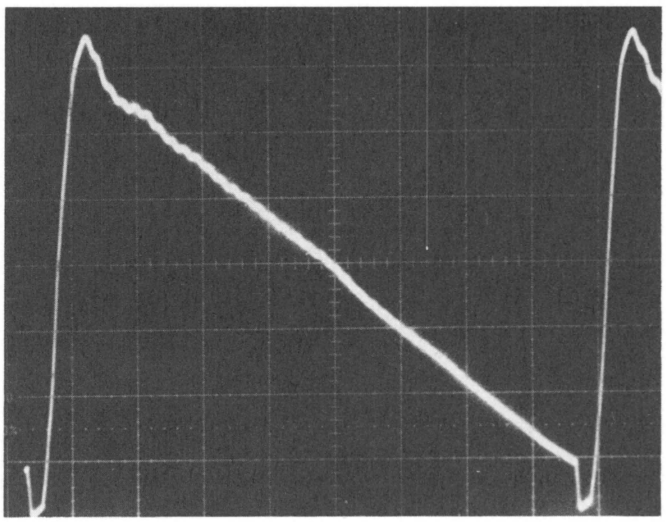
2b. NULL FREQ. CORRECT



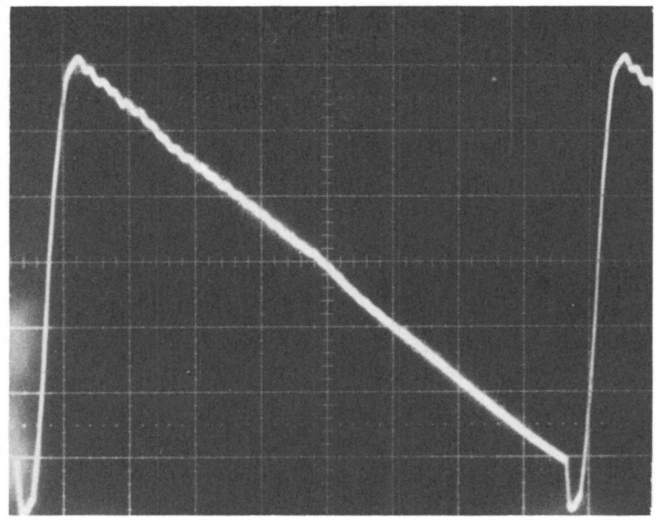
2c. NULL FREQ. TOO HIGH

6. Adjust **7R145** DAMP PHASE for minimal ringing, overshoot, and the flattest slope on the ramp, as in figure 3.

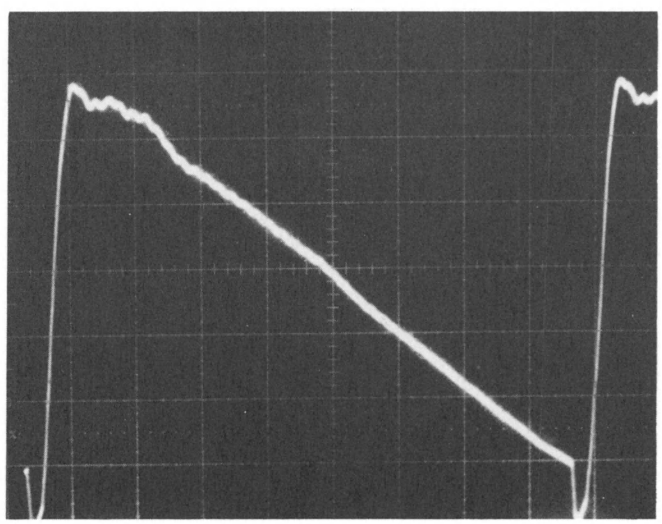
- Try to obtain a waveform resembling Figure 3b as closely as possible.
- All controls are interactive. It typically requires three passes through **7R144, R143,** and **R145** to obtain the desired result.
- Some AST heads will not require any Damp Phase correction, and 7R145 will remain in the full CCW position.



3a. DAMP PHASE TOO LOW



3b. DAMP PHASE CORRECT



3c. DAMP PHASE TOO HIGH

7. Change Test Jumper **7J2** to the **OPR B** position. This inhibits dynamic (AC) correction. Playback a recording made recently on this transport at about ¼ x PLAY speed.

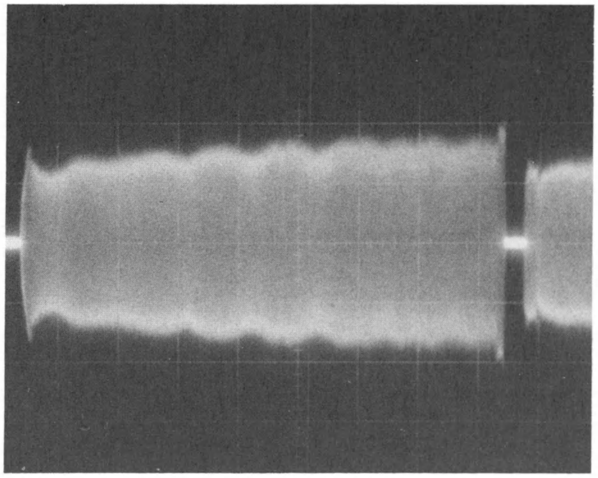
- Look at the RF envelope on the WAVEFORM MONITOR, OR AT PWA 1 MODULATOR **TP13,** with RF selected on the Control Panel. If **1TP13** is used, sync the oscilloscope at PWA **6TP3,** Scanner Tach.
- Adjust **7R121,** Ramp Level, clockwise for minimum flutter on the RF envelope. The optimum point is rather broad - over one turn of **7R121.** Try to adjust it to the high, most clockwise end of the range.
- Refer to Figure **4**.

8. Put the AST Servo in FRAME mode (SERVO SET-UP Menu). Playback at approximately 20% REVERSE SLOW MOTION and adjust CORRECTION GAIN **7R122** for the best RF envelope. The optimum point is broad - several turns. Try to leave it in the center of range.

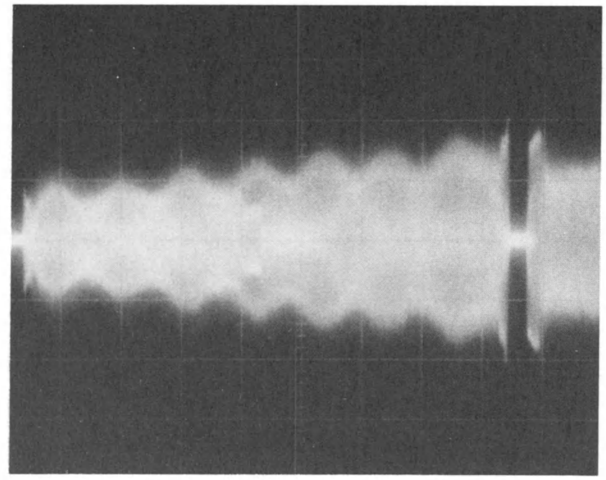
- Re-adjust RAMP LEVEL **7R121** to verify that it is still at the optimum position.

9. Observe DEMOD OUT VIDEO on the WAVEFORM MONITOR, at 2V MAG; or at **1TP13** with DEMOD VIDEO selected on the control panel, using scope delay to observe the vertical interval. If a SYNC HEAD is installed, turn it off with the switch on PWA 6 PLAYBACK SYNC PROC.

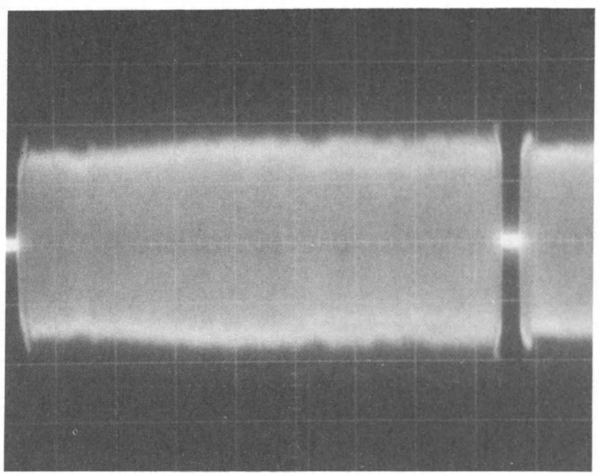
- Play back in full REVERSE SLOW MOTION. Adjust RESET TIMING **7R187** to position the format dropout in the center of the vertical interval.
- Observe TBC VIDEO OUT on the picture monitor. There should be no line tearing before or after vertical blanking.
  * Adjust **7R187** RESET TIMING to eliminate any line tearing.
  * Do not over-adjust - moving the disturbance from before vertical blanking to after vertical blanking.
- Verify operation over the full slow motion range of -1 to +3. Observe the RF ENVELOPE for proper tracking, and the PICTURE MONITOR for any video disturbance before or after verical blanking.
- Return Test Jumper **7J2** to the NORMAL "OPR A" position.
- Operate the VPR-3 over the full slow motion range.



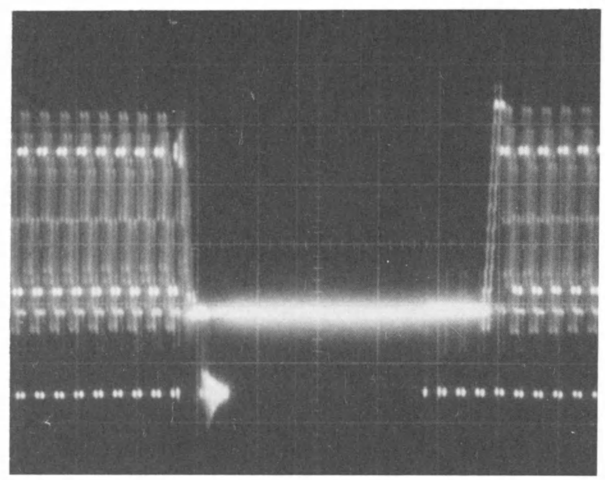
4a. R121 SLIGHTLY MISADJUSTED



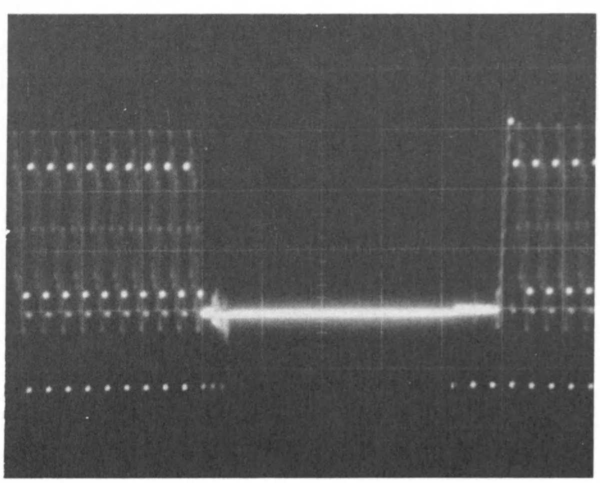
4b. R121 SEVERELY MISADJUSTED



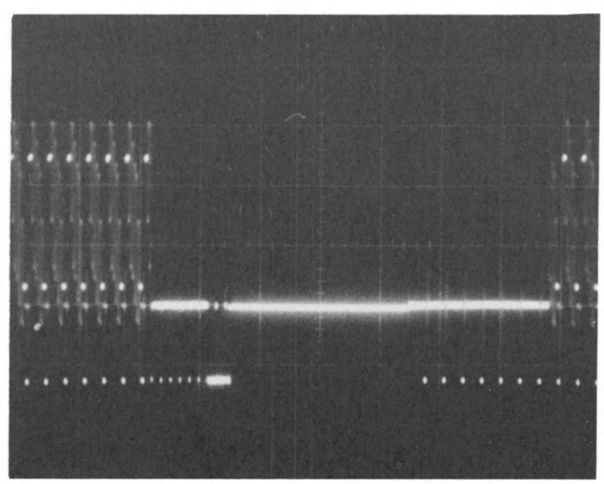
4c. R121 ADJUSTED CORRECTLY



5a. R187 ADJUSTED FOR TEARING AFTER VERT. BLANKING



5b. R187 ADJUSTED FOR LINE TEARING BEFORE VERTICAL BLANKING

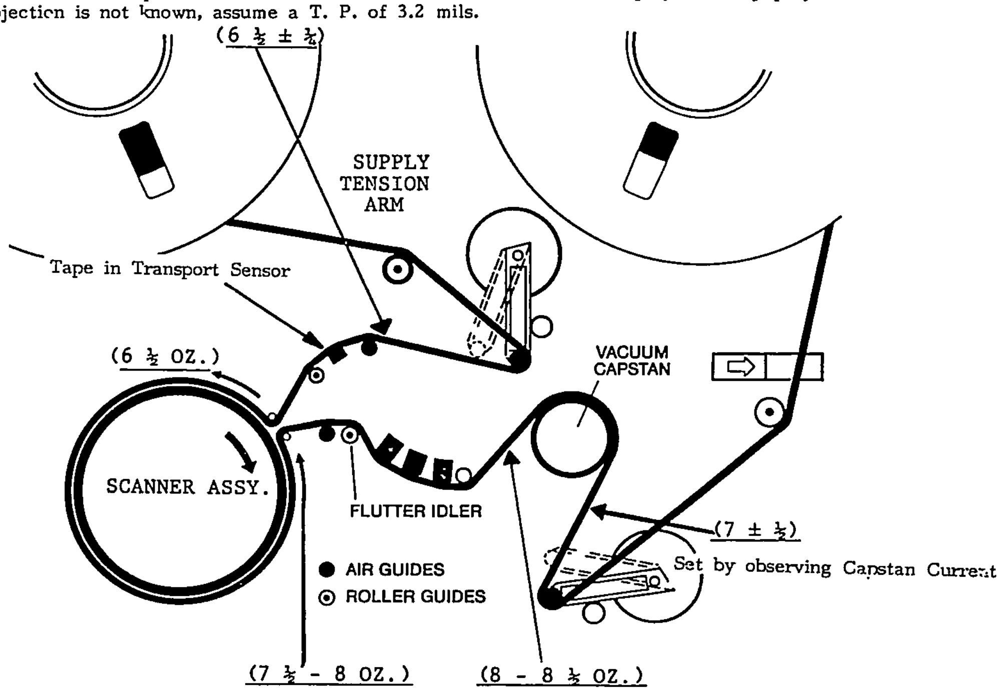


5c. R187 ADJUSTED PROPERLY

VPR 3 HELICAL INTERCHANGE ALIGNMENT

Preliminary checks and adjustments

1. Everything in the tape path should be cleaned thorougly. Xylene or AMPEX head cleaner is recommended for all record/playback and erase heads, metal guides, and the scanner surface.
2. Check the capstan vacuum, scanner and guide air pressure, and adjust if necessary. Check and adjust if necessary tape path tensions.
3. If dropout width and position is to be checked, check the video record/play head tip projection and note. If tip projection is not known, assume a T. P. of 3.2 mils.



Interchange test and adjustment set-up

The VPR-3 should be set-up to simulate record timing for the interchange tests. The following menu selections apply to all of the interchange procedures. Upon the completion of test and/or alignment, they should be returned to their normal position.

1. On the PLAYBACK SYNC PROCESSOR PWA 6 Switch S1 (Composite Sync Insert) and Switch S2 (Sync Head Playback) should be **OFF**
2. VIDEO SET-UP MENU: select RECord head playback.
3. Whenever the guide alignment tape is used, set MASTER RECORD LOCKOUT with the switch on CONTROL PWA 20.
4. **WARNING:** Do not press TACH PHASE mode (SERVO or EDITOR SET-UP Menu) after tape is threaded. If it is inadvertently pressed, the information in memory can be cancelled by lifting the tape off of the tape in transport sensor located on the longitudinal video record head. This will also put tracking back to unity, and set TT 1 and TT 2 to 23:58:00:00.

There is interaction between the various adjustments. It is important that they be checked in the following order:

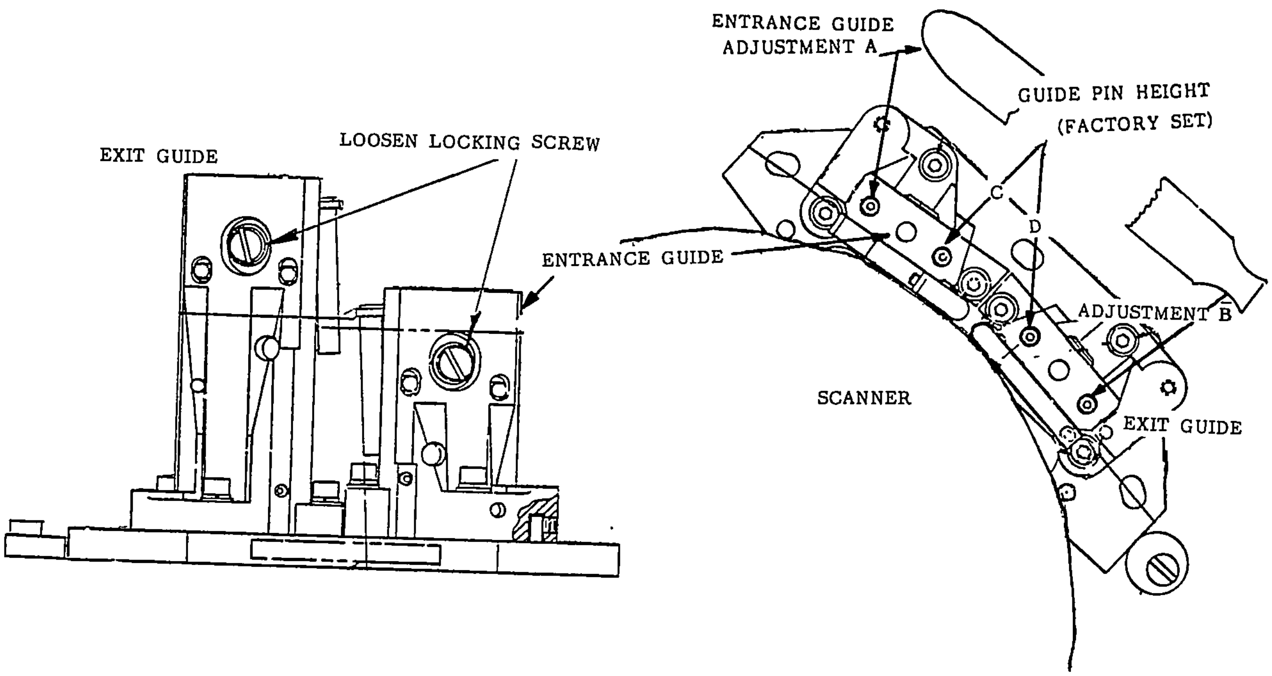
1. Track straightness.
2. Scanner tachometer position.
3. Format dropout position and duration.
4. Control track record/play head position.

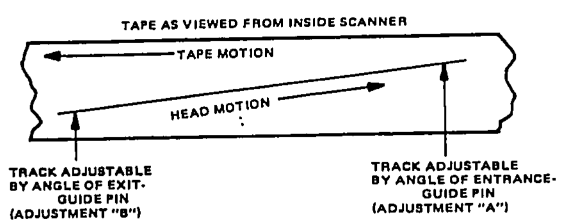
Track straightness is checked by playing back the guide alignment tape and varying MANUAL TRACKING while observing the RF envelope.

1. Connect the oscilloscope:

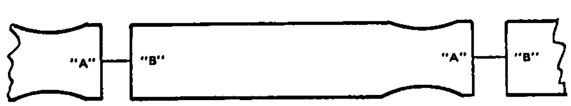
Trigger	P/B SYNC PROC. **PWA 6 TP4**, Reference Vertical. (It is located on the front of PWA 6 near the bottom.)
Channel 1	MOD/DEMOD PWA 1 TP 13 Select RF ENVELOPE on the control panel monitor selector.

2. Play back the Guide Alignment tape. On the Servo Set-up menu, select **Variable Tracking**.
   Tracking is automatically returned to UNITY whenever tape is removed from the Tape-in-Transport-Sensor located on the video erase head assembly.
3. Turn tracking control, while observing the RF envelope. As the tracking control is turned past the point of maximum RF, the envelope should collapse evenly, with no taper around the edges at the dropout area or through the envelope.
4. To adjust for envelope irregularities, when necessary:
   - Loosen the guide adjustment locking screw on the entrance and/or exit guide.
   - Play back the guide alignment tape.
   - Rotate the KNOB tracking control back and forth through the peak RF point, observing the edges of the RF envelope on each side of the format dropout.
   - Adjust screws "A" and/or "B" for maximum output and flatness of the leading and trailing edges of the RF envelope.
   - Tighten the entrance and exit guide block locking screws. Repeat the test and observe that the envelope is still correct
5. The guide heighth adjustment screws are factory set. See Appendix A.

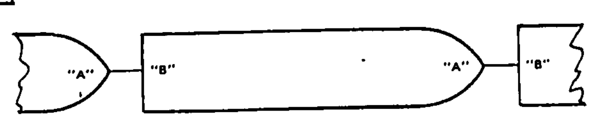




IDEAL RF ENVELOPE—ADJUSTMENTS "A" AND "B" CORRECTLY SET



ADJUSTMENT "A" MISADJUSTED



ADJUSTMENT "A" MISADJUSTED

Scanner tachometer (tach) position determines the heighth of the video tracks on the tape.

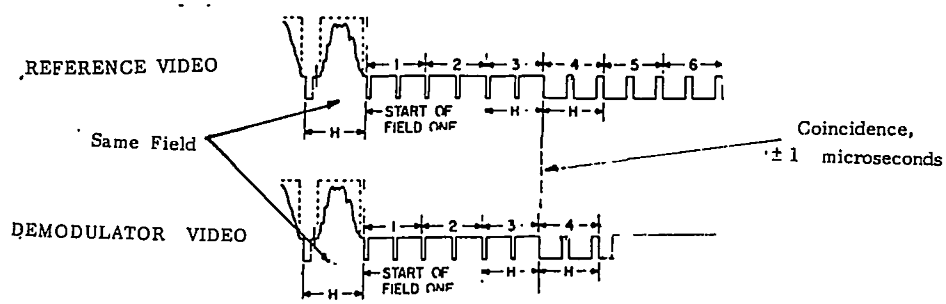
1. Set up the oscilloscope:

Trigger	Waveform Monitor Sync BNC on the back of the VPR-3 (use a "T").
Channel 1 Probe	MODULATOR PWA 1 **TP 13**. Select DEMOD VIDEO on the control panel monitor select switches.

2. VPR 3 Mode:

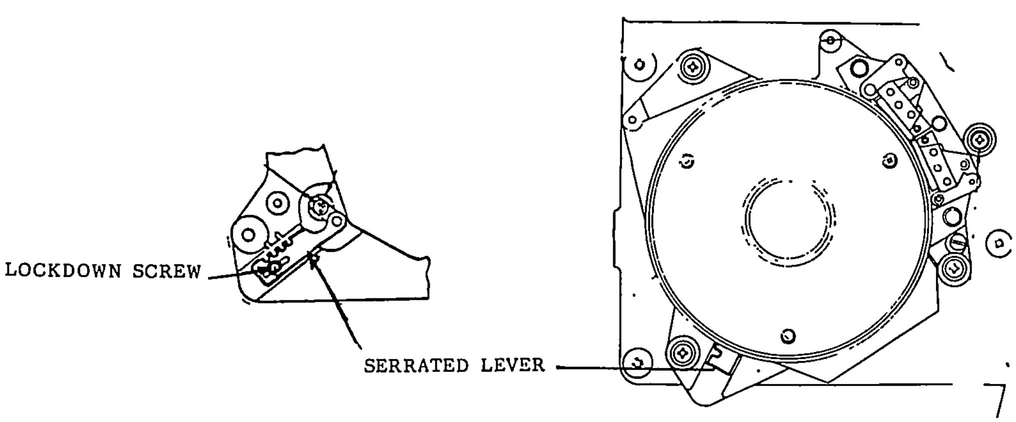
HOME MENU	EDIT ASSEMBLE
VIDEO SET-UP	Record Head Playback

3. Playing back the guide alignment tape, use the KNOB **tracking control** to peak tracking as observed on the control panel VIDEO/RF Meter. Improper adjustment of tracking can introduce errors in excess of tolerances.
4. Momentarily depress the **Tape/EE** switch on the RF EQUALIZER PWA 3 and adjust the oscilloscope to place the start of the EE Vertical broad pulse on a convenient graticule marking. Release the switch.



Observe that the playback Vertical Sync edge is coincident, ± 1 microsecond, with reference vertical.

5. If not, loosen the lever hold down screw and use a screwdriver to move the serrated lever for coincidence of the vertical timing edges, ± 1 microsecond.
6. Observe the horizontal pulses after dropout (approximately line 17 - 20 on NTSC). If necessary, adjust for coincidence, ± 1 microsecond.
7. Tighten the lockdown screw. Observe that there is no change in timing when the screw is tightened.

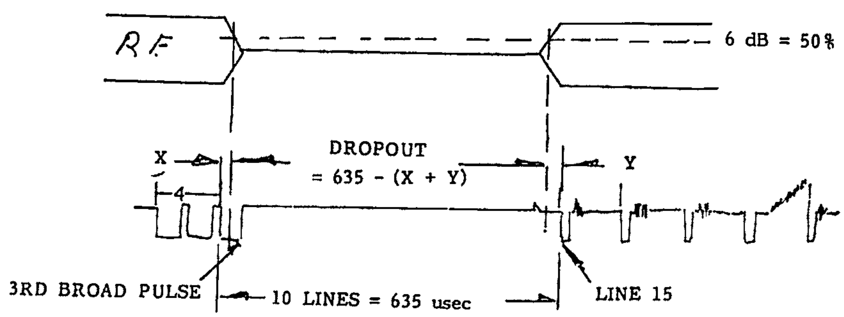


Dropout position and duration are checked by making a new recording on a work tape. Do not use Edit Record mode. The width of the dropout is affected by the tip penetration, which changes as the tip wears down.

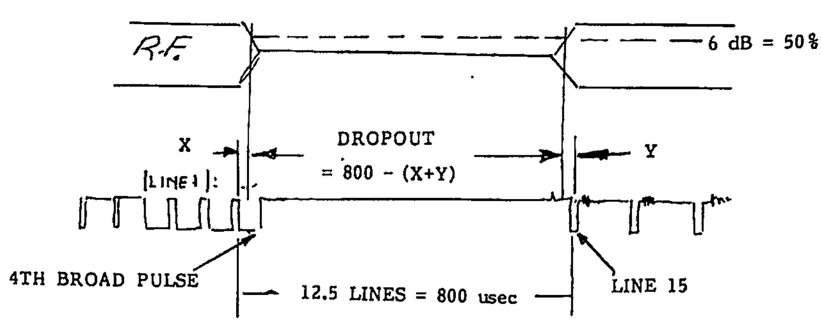
DROPOUT POSITION AND DURATION VERSUS TIP PROJECTION

	525		625	
TIP PROJ (MILS)	D. O. WIDTH ± 10 µs	µs into 3rd Broad Pulse ± 3 µs	D. O. WIDTH ± 10 µs	µs into 4th Broad Pulse ± 3 µs
2.5	632	0.4	758	19.6
2.6	629	1.0	754	20.2
2.7	626	1.5	751	20.8
2.8	623	2.0	747	21.4
2.9	620	2.6	744	22.0
3.0	617	3	740	22.6
3.1	614	3.5	736	23.2
3.2	612	4.0	733	23.8
3.3	609	5.0	730	24.4
3.4	606	5.5	726	25.0
3.5	604	6.0	724	25.6
3.6	601	6.5	721	26.2

525



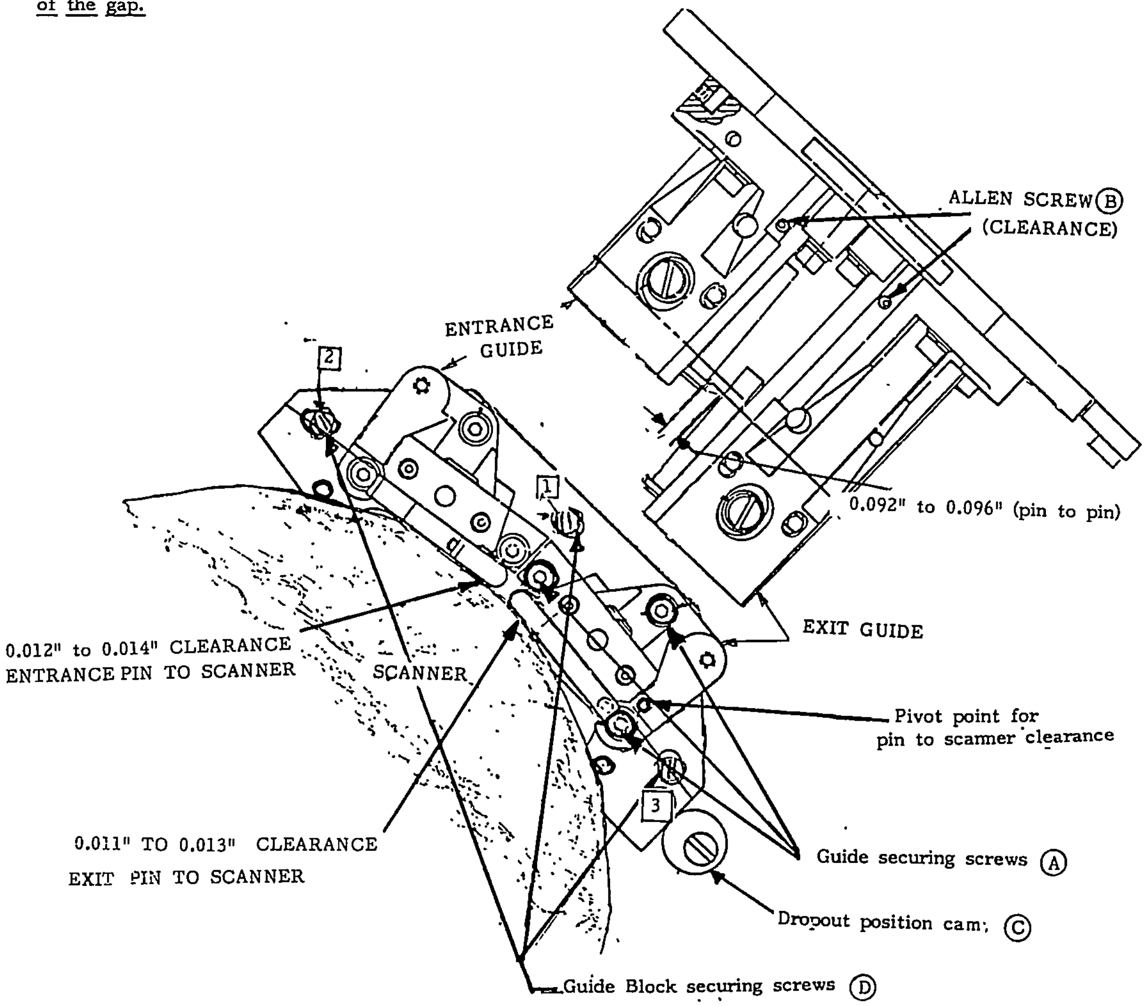
625



After making a new recording, connect the oscilloscope as follows, and measure the dropout duration at the 50% point on the RF envelope as well as its timing with respect to the vertical 3rd (525) or 4th (625) broad pulse.

Trigger	Waveform Monitor Sync BNC on the rear of the VPR-3.
Channel 1	MODULATOR PWA 1 TP 13, selecting RF ENVELOPE on the Control Panel Monitor Select switches.
Tracking	UNITY
Video Head	On video set-up Menu, select RECord Head playback.

Dropout duration is affected by the pin to scanner gap. To measure the clearance, insert a 12 mil precision plastic stock between the scanner and the guide pin at the record head height. Make certain all heads are clear of the gap.



To adjust the clearance:

1. Turn allen screw **B** clockwise until it contacts the scanner.
2. Loosen the three guide securing screws **A**.
3. Turn allen screw **B** clockwise to increase the gap. To decrease the gap, turn **B** counterclockwise while pushing gently on the guide assembly.
4. Snug down the three securing screws **A** going from one to another.
5. Recheck the clearance.
6. Back off allen screw **B** two turns counterclockwise.

Dropout position is adjusted using the dropout position cam. Switch the monitor to DEMOD VIDEO.
Make certain that the SYNC ADD switch on Playback Sync Processor PWA 6 is off

If the dropout is early, loosen the screw that secures the dropout position cam **C** and use a feeler guage to set the spacing in mils between the cam and the guide block. **One mil equals one microsecond.**

1. Loosen the guide block securing screws **D** and slide the guide block until it presses against the cam, and the guide block locating pins are resting against the lower scanner.
2. When moving the guide block, loosen the three guide block screws enough so that the rubber ring under the guide block is not pulled along and deformed when the block is moved.
3. Tighten the three guide block securing screws **D** in the **1, 2, 3** sequence shown, making three passes before full torque is applied.

If the dropout is late, first loosen the three guide block securing screws **D**. Use a feeler guage to set the clearance between the guide block and the dropout position cam. Tighten the three guide block securing screws **D** in the **1, 2, 3** sequence.

- Loosen the cam, rotate it until it snug against the guide block,and retighten.

Make a new recording and verify the dropout position and duration. **Recheck track straightness.**

Control track position is checked using the same procedures as for scanner tachometer position, except that tracking must be in **UNITY**

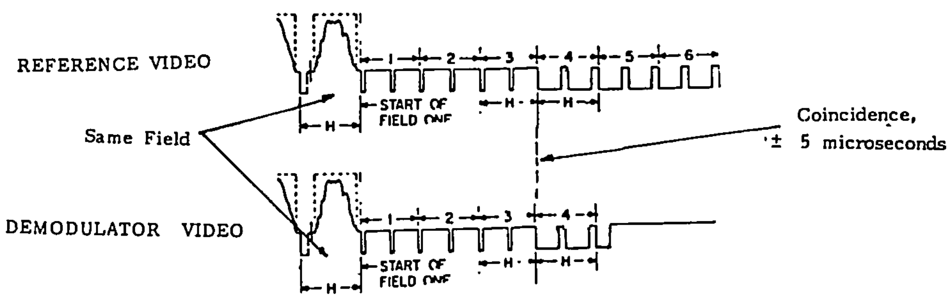
1. Set up the oscilloscope:

Trigger	Waveform Monitor Sync BNC on the back of the VPR-3 (use a ("T").
Channel 1 Probe	MODULATOR PWA 1 **TP** 13. Select DEMOD VIDEO on the Control Panel Monitor Selector.

2. VPR-3 mode

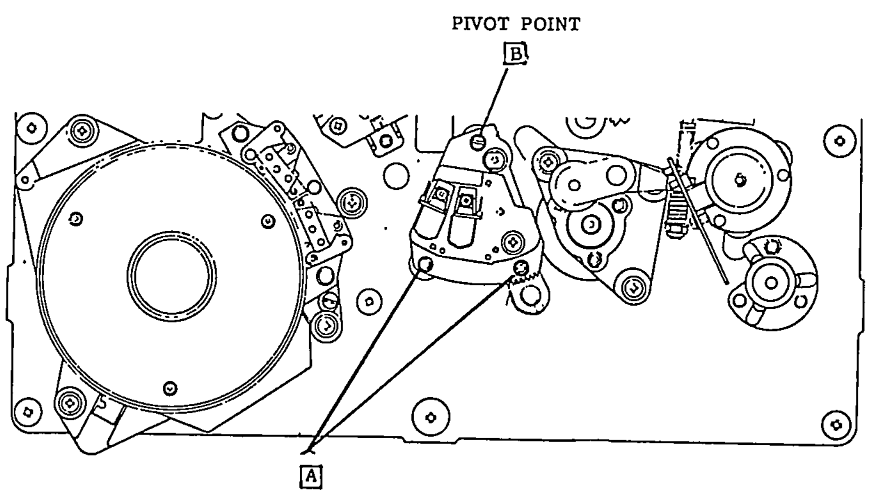
Home Menu	Edit Assemble mode
Servo Set-Up	Tracking to Unity
Video Set-up	Record Head Playback

3. Playback the guide alignment tape with TRACKING in UNITY. Momentarily depress the TAPE/EE switch on RF EQUALIZER PWA 3, and adjust the scope to place the start of the vertical broad pulse on a convenient graticule marking. Observe that the two vertical sync intervals are coincident, ± 5 microseconds, and on the same field.



If the timing is not within ± 5 microsecond, the **audio and control track head assembly** must be moved.

1. Loosen the two screws **A** so that the head assembly can pivot on **B**.
2. Playing back the guide alignment tape, move the head assembly to achieve coincidence between Demod and Reference vertical, ± 5 microsecond. A movement of one sixth of an inch represents a one field displacement!
3. Adjust the oscilloscope to observe horizontal sync after dropout. Adjust, if necessary, for coincidence within ± 1 microsecond. Tighten the screws on the audio head assembly base.



INCHVPA.MSS-01

VPR 3 HELICAL INTERCHANGE
APPENDIX A
GUIDE HEIGHT ADJUSTMENTS

1. Use extreme care in making any guide height adjustments. Guide height and guide angle adjustments are interactive. The two are adjusted together, in small increments, to achieve correct biasing of the tape onto the guide band, and a flat RF envelope, as tracking is varied. Misadjustment can cause serious interchange problems.

2. Set-up:

SCOPE:	Trigger PLAYBACK SYNC PWA TP 4
	Channel 1 to MODULATOR PWA TP 13
	Select RF on the VPR 3 Control Panel Monitor Select.
VPR-3	Loosen the slotted screws on the EXIT and ENTRANCE Guides ½ turn
	Record Lockout, CONTROL PWA 20, ON.
	On the VIDEO SET-UP menu, select RECORD HEAD playback, and Variable Tracking.
	Playback the Guide Alignment Tape.

3. Adjust the entry height adjustment screw C for proper biasing of the tape by the ceramic edge guide - 2 to 3 mils lift off of the guide.

The edge guide should not buckle the tape. A push on the entry keeper should cause a slight (10%) dip in the right edge of the RF envelope.

Be very careful not to push the ceramic guide into the rotating scanner.

A clockwise turn on screw C will increase the bias on the tape, while a counterclockwise turn will raise the edge off of the tape.

Alternate the height adjustment with angle adjustment A to peak up the RF envelope without causing a dip elsewhere.

Vary tracking and observe that the RF envelope on the scope rises and falls evenly.

The proper adjustment of C and A is ¼ turn clockwisefrom the point wherethe ceramic guide just touches the tape.

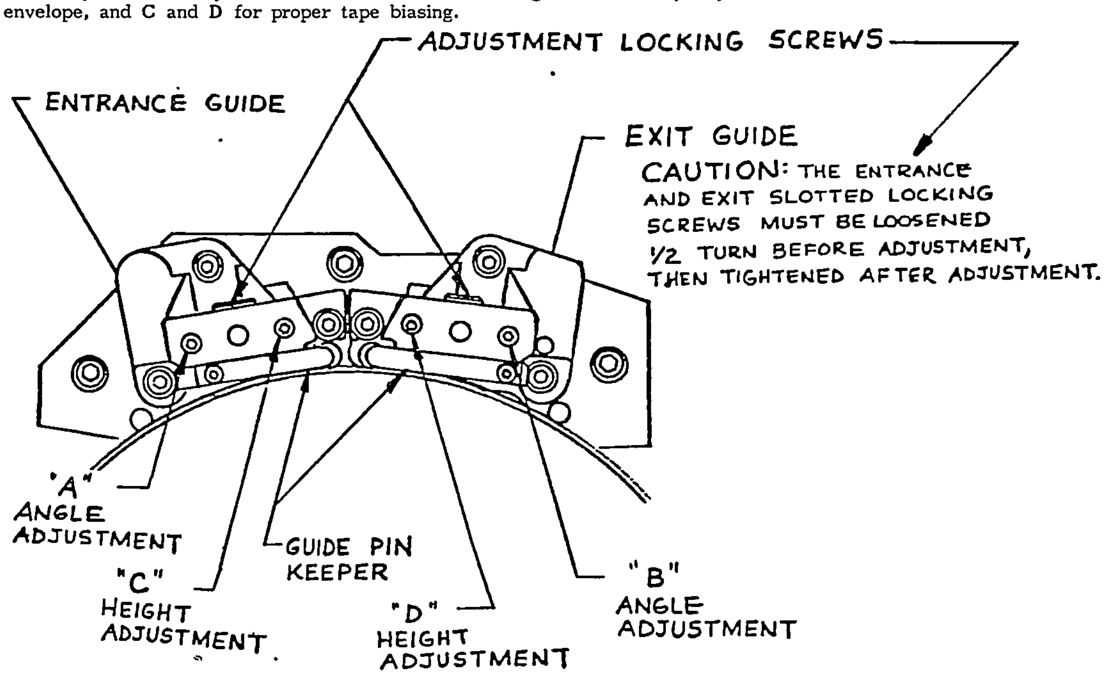
4. Repeat the procedure for screws B (angle) and D (height) on the exit guide..

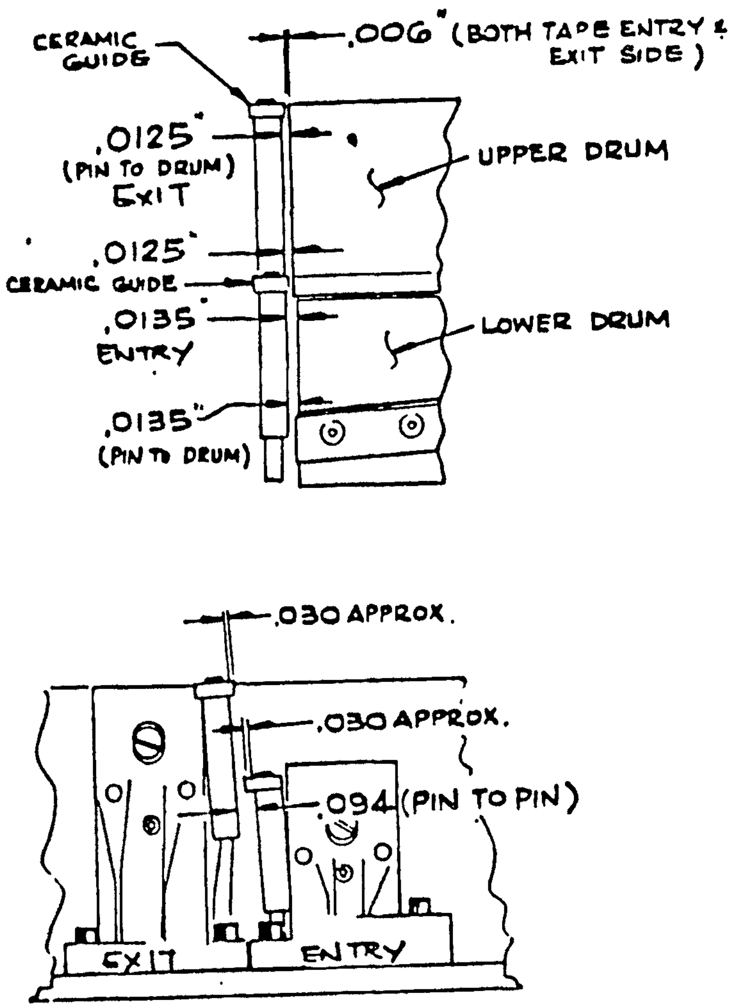
5. Depress STOP, and when the scanner stops, tighten the slotted screws on the Entrance and Exit guides.

6. Playback the guide alignment tape. Vary tracking, and verify that the RF envelope rises and falls uniformly. Leading and trailing edges should rise and fall together. Apush on the guide keeper should cause a slight dip (approximately 10%) on the edge of the RF envelope.

Make sure the tape is not being buckled by the ceramic guide edge guide.

It may be necessary to loosen the slotted screws again, and finely adjust Screws A and B for flat envelope, and C and D for proper tape biasing.





SCANNER GUIDE PIN ADJUSTMENT

FIG 1.A

Verify pin-to-pin spacing is between 0.092 to 0.096 inches. (See Figure 1). (Note: use 0.092, 0.094, 0.096 gauges in "go-no-go" technique).

013

Verify pin-to-drum spacing is 0.012 to 0.014 inches for the entry pin and 0.011 to 0.013 inches for the exit pin. (See Figure 1). Adjust if necessary and repeat step 4.

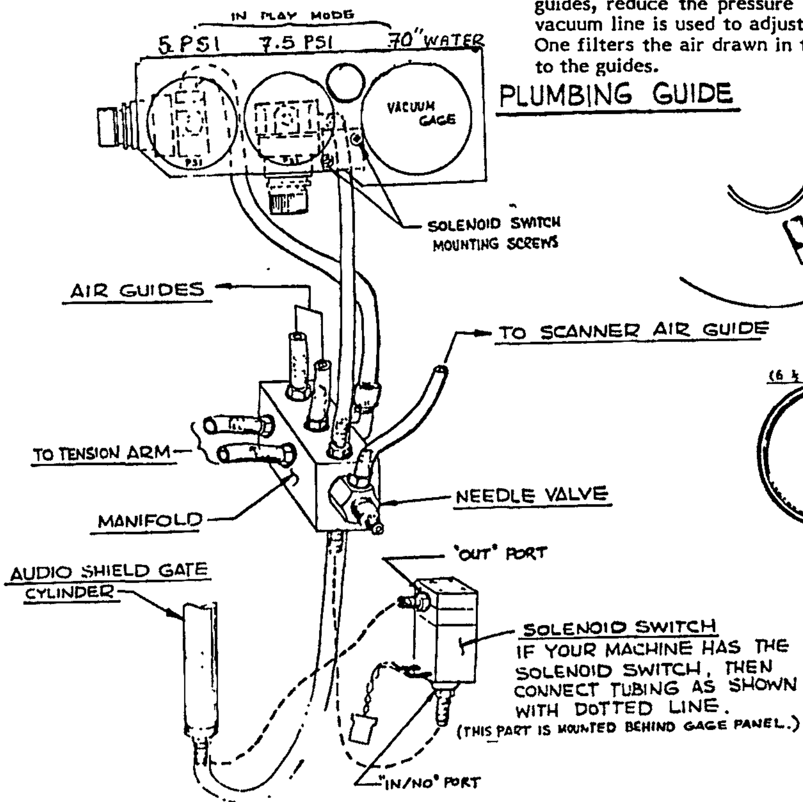
NOTE

THE PINS SHOULD BE PARALLEL TO THE SCANNER WITHIN .5 MILS.

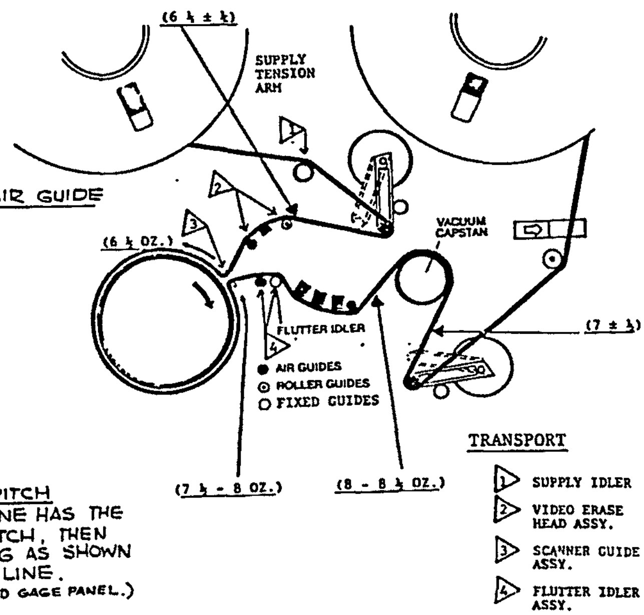
Adjust spacing of the spring loaded ceramic edge guides for .005 to .007 inches spacing from the upper drum (see Figure 1). Verify that the ceramic extends .003 to .005 inches over the front of the pin and lays flat on top of the pin - (push finger forward if necessary). Use gram gauge and measure spring force of 22 to 27 grams. Reform spring as necessary to achieve spring force and flatness.

2-6 AIR SYSTEM CHECKS

The air system is housed in an acoustically shielded enclosure located behind the tape transport. It provides the air used by the air guides on the tape transport and the vacuum required by the capstan. It also supplies air for the air-actuated audio headstack shield that slides into position when VPR-3 power is on and tape is threaded. An ac-powered rotary-vane type compressor produces the pressure. Two pressure regulators, one for the scanner guides and the other for the transport guides, reduce the pressure to the appropriate levels. A pressure regulator in the vacuum line is used to adjust the capstan vacuum. The system uses two air filters. One filters the air drawn in through the capstan and the other filters the air output to the guides.



PLUMBING GUIDE



1. Adjust scanner guide pressure for 7.5 PSI in play mode.
2. Adjust transport guide pressure for 5 PSI in play mode.
3. Adjust vacuum for 70 inches of water in play mode.
4. Repeat step 16, 17 and 18 as necessary.
5. Turn off power and extend PWA A14 (Reel and Scanner Servo). Connect scope to Pin 35 (Capstan MDA Drive). 0.45V equals 1 amp of capstan current.
6. Place machine in stop, then +1 var. play. Rotate the needle valve counter-clockwise to obtain a minimum of capstan current.
7. Adjust the needle valve clockwise until the capstan current is 100 ma above the minimum. (0.045V above min. reading).
8. Adjust take-up tension for equal capstan current in variable play mode for +1x and -1x play speed.
9. Place the machine in stop, then play. If everything is normal the capstan current will run from 0.7 to 1.0 amp depending on altitude, tape, humidity, temp, etc. If the capstan current is high, check the transport guides by raising the pressure to them. If current decreases with an increase in air pressure, then one or more guides are not flowing properly. Isolate defective guide by checking tension build-up through the transport.

COLOR FRAMER ADJUSTMENTS
NTSC

NOTE:- NO ADJUSTMENT OF THE COLOR FRAMER, PWA5, SHOULD BE PERFORMED UNLESS A KNOWN RS170A VIDEO SOURCE OF 0 DEGREES SC/H PHASE IS AVALIABLE. A suitable source is the video output of the ZEUS 1 with SC/H phase set to standard, or using the Advanced Reference output. All adjustments should only be performed if components have been changed, as the unit is Factory calibrated.

1. With power removed from the VPR-3, place PWA 5 COLOR FRAMER, on the extender. Turn on the editor with the [editr] softkey in the Home menu. Unless otherwise stated the **System Unity** button should be in **UNITY**.

REFERENCE COLOR FIELD 1 IDENTIFIER.

2. 3.58MHz Phase Locked Oscillator adjustment.

Scope	5Pin 61 5TP25 5Pin 47 (Trigger) Adjust the scope's timebase in delayed sweep to show the burst on Pin61.
Jumper	5J6 A-C
Adjust	5 C 163 for minimum drift between the two signals.
Jumper	5J6 A-B

3. 90 Degree Phase Shifter adjustment.

Scope	5TP 15 (Trigger) 5TP 24
Adjust	R246 so that the pulses at TP15 are in the center of the high or low portion of the square wave at TP24. NOTE: The pulses could be at either the high or low part of the square wave, and either is correct.

DEMODULATED VIDEO FIELD IDENTIFIER

4. VCO Error Voltage Offset. Either short 5R29 or ground U18-3.

Scope	5TP 5
Adjust	R223 for 0 volts at TP 5. Remove the short.

5. VCO Error Voltage.

Scope	5TP 5
Adjust	L3 for 0 volts at TP 5.

6. Burst Filter Tuning.

Scope	5TP 6 5Pin 47 (Trigger)
Adjust	L2 for maximum amplitude burst at TP 6.

7. Horizontal Subcarrier Delay.

Scope	5TP 2 Burst Sample 5TP 3 H Derived Subcarrier 5Pin 47 (Trigger) Flywheel H
Adjust	L1 so that the pulses at TP2 are in the center of the high or low portion of the square wave at TP3. NOTE: The pulses could be at either the high or low part of the square wave, and either is correct.

8. SC/H Phase Meter Calibration. Adjust 5R 119 so that the SC/H Phase Meter on the Control Panel reads 0 Degrees.

9. SC/H Meter calibration range control. With the system in variable adjust the SC/H meter control CW until the meters reads +40 degrees. Now turn the control an equal distance CCW and ensure that the meter reads -40 degrees. If it does not adjust 5R 263. Repeat until an equal CW, CCW adjustment of the control gives an equal indication on meter. Place the system back into UNITY.

NOTE: The next two steps require a video source that allows the SC/H phase to be adjusted a calibrated amount. If such a source is not avaliable then these steps should NOT be done. If the VPR 3 is connected to a ZEUS 1 then put the system in PREPROC and with the [ZEUS]; [PHASE] menu adust the SC/H phase.

10. **SC/H Phase Meter Linearity** adjustment. On the Video Input source swing the SC/H phase +40 degrees, note the meter reading. Now swing the SC/H phase of the source to -40 degrees and the meter should read the same negative as for the positive swing. If there is any non-linearity adjust **5R 222** for an equal positive and negative deflection for the source SC/H phase.

11. **SC/H Phase Meter gain.** Adjust the source SC/H phase for +70 degrees. If the meter does not read +70 the adjust **5R 27** to achieve this. Ensure that when the source phase is swung to -70 degrees that the meter reads -70.If it does not recheck the adjustment of **R 222.** Repeat steps 10 and 11 as necessary to get correct meter deflection.

12. **Waveform position** adjustment. Play a previously recorded tape and select the RF monitoring on the Video Monitoring selector. Adjust **R 221** so that the RF display is central, showing the two dropouts evenly placed from either edge of the display.

COLOR FRAMER ADJUSTMENTS
PAL

NOTE:- NO ADJUSTMENT OF THE COLOR FRAMER, PWA5, SHOULD BE PERFORMED UNLESS A KNOWN VIDEO SOURCE OF 0 DEGREES SC/H PHASE IS AVALIABLE. A suitable source is the video output of the ZEUS 1 with SC/H phase set to standard, or using the Advanced Reference output. All adjustments should only be performed if components have been changed, as the unit is Factory calibrated.

1. With power removed from the VPR-3, place PWA 5 COLOR FRAMER, on the extender. Turn on the editor with the [editr] softkey in the Home menu. Unless otherwise stated the System Unity button should be in UNITY.

REFERENCE COLOR FIELD 1 IDENTIFIER.

2. 4.43MHz Phase Locked Oscillator adjustment.

Scope	5Pin 61 5U109-8 5Pin 47 (Trigger) Adjust the scope's timebase in delayed sweep to show the burst on Pin61.
Jumper	5J8 A-C
Adjust	5 C 220 for minimum drift between the two signals.
Jumper	5J8 A-B

3. Subcarrier Tuned Amplifier, adjustment.

Scope	U107-3
Adjust	L10 for maximum subcarrier.

4. 25Hz Tuned Amplifier adjustment.

Scope	5TP 3
Adjust	R282 for a 10v p-p 25Hz signal.

5. 90 Degree Phase Shifter adjustment.

Scope	5TP 13 (Trigger) 5TP 30
Adjust	R292 so that the H pulses at TP13 are at the peak or trough of the 25 Hz sine wave at TP230. <u>NOTE:</u> The pulses could be at either the high or low part of the square wave, and either is correct.

DEMODULATED VIDEO FIELD IDENTIFIER

6. Frame Ramp Generator.

Scope	5TP 23
Adjust	5R 46 so that there is no step half way up the 25Hz ramp at TP23.

7. 25Hz Offset.

Scope	5TP 15
Adjust	5R 39 for a minimum 25Hz component in the VCO error signal at TP15.

8. VCO Error Voltage Offset. Either short 5R157 or ground U47-3.

Scope	5TP 15
Adjust	R155 for 0 volts at TP 15. Remove the short.

9. **VCO Error Voltage.**

Scope	5TP 15
Adjust	L3 for 0 volts at TP 15.

10. **Burst Filter Tuning.**

Scope	5TP 1 5Pin 47 (Trigger)
Adjust	L1 for maximum amplitude burst at TP 1.

11. **Horizontal Subcarrier Delay.**

Scope	5TP 2 Burst Sample 5TP 3 H Derived Subcarrier 5Pin 47 (Trigger) Flywheel H
Adjust	L2 so that the pulses at TP2 are in the center of the high or low portion of the square wave at TP3. NOTE: The pulses could be at either the high or low part of the square wave, and either is correct.

12. **SC/H Phase Meter Calibration.** Adjust 5R 177 so that the SC/H Phase Meter on the Control Panel reads 0 Degrees.

13. **SC/H Meter calibration range control.** With the system in variable adjust the SC/H meter control CW until the meters reads +40 degrees. Now turn the control an equal distance CCW and ensure that the meter reads -40 degrees. If it does not adjust 5R 147. Repeat until an equal CW, CCW adjustment of the control gives an equal indication on meter. Place the system back into UNITY.

NOTE: The next two steps require a video source that allows the SC/H phase to be adjusted a calibrated amount. If such a source is not avaliable then these steps should NOT be done. If the VPR 3 is connected to a ZEUS 1 then put the system in PREPROC and with the [ZEUS]; [PHASE] menu adust the SC/H phase.

14. **SC/H Phase Meter Linearity** adjustment. On the Video Input source swing the SC/H phase +40 degrees, note the meter reading. Now swing the SC/H phase of the source to -40 degrees and the meter should read the same negative as for the positive swing. If there is any non-linearity adjust **5R 106** for an equal positive and negative deflection for the source SC/H phase.

15. **SC/H Phase Meter gain.** Adjust the source SC/H phase for +70 degrees. If the meter does not read +70 the adjust **5R 109** to achieve this. Ensure that when the source phase is swung to -70 degrees that the meter reads -70.If it does not recheck the adjustment of **R 106.** Repeat steps 14 and 15 as necessary to get correct meter deflection.

16. **Waveform position** adjustment. Play a previously recorded tape and select the RF monitoring on the Video Monitoring selector. Adjust **R 303** so that the RF display is central, showing the two dropouts evenly placed from either edge of the display.